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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

FSEZ1317
Primary-Side-Regulation PWM with POWER MOSFET Integrated

Features

- Low Standby Power Under 30mW
- High-Voltage Startup
- Fewest External Component Counts
- Constant-Voltage (CV) and Constant-Current (CC) Control without Secondary-Feedback Circuitry
- Green-Mode: Linearly Decreasing PWM Frequency
- Fixed PWM Frequency at 50kHz with Frequency Hopping to Solve EMI Problem
- Cable Compensation in CV Mode
- Peak-Current-Mode Control in CV Mode
- Cycle-by-Cycle Current Limiting
- V_{DD} Over-Voltage Protection with Auto Restart
- V_{DD} Under-Voltage Lockout (UVLO)
- Gate Output Maximum Voltage Clamped at 15V
- Fixed Over-Temperature Protection with Auto Restart
- Available in the 7-Lead SOP and DIP Packages

Applications

- Battery chargers for cellular phones, cordless phones, PDA, digital cameras, power tools, etc.
- Replaces linear transformers and RCC SMPS

Description

This third-generation Primary-Side-Regulation (PSR) and highly integrated PWM controller provides several features to enhance the performance of low-power flyback converters. The proprietary topology, TRUECURRENT™, of FSEZ1317 enables precise CC regulation and simplified circuit design for battery-charger applications. A low-cost, smaller, and lighter charger results, as compared to a conventional design or a linear transformer.

To minimize standby power consumption, the proprietary green mode provides off-time modulation to linearly decrease PWM frequency under light-load conditions. Green mode assists the power supply in meeting power conservation requirements.

By using the FSEZ1317, a charger can be implemented with few external components and minimized cost. A typical output CV/CC characteristic envelope is shown in Figure 1.

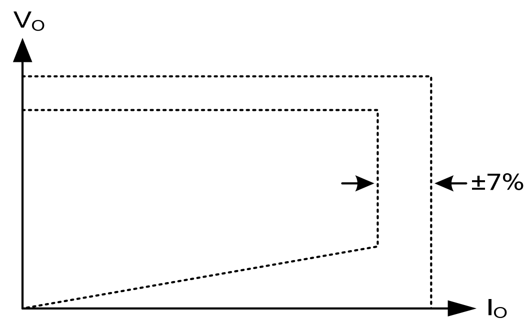


Figure 1. Typical Output V-I Characteristic

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FSEZ1317MY	-40°C to +105°C	7-Lead, Small Outline Package (SOP-7)	Tape & Reel
FSEZ1317NY	-40°C to +105°C	7-Lead, Dual Inline Package (DIP-7)	Tube

Application Diagram

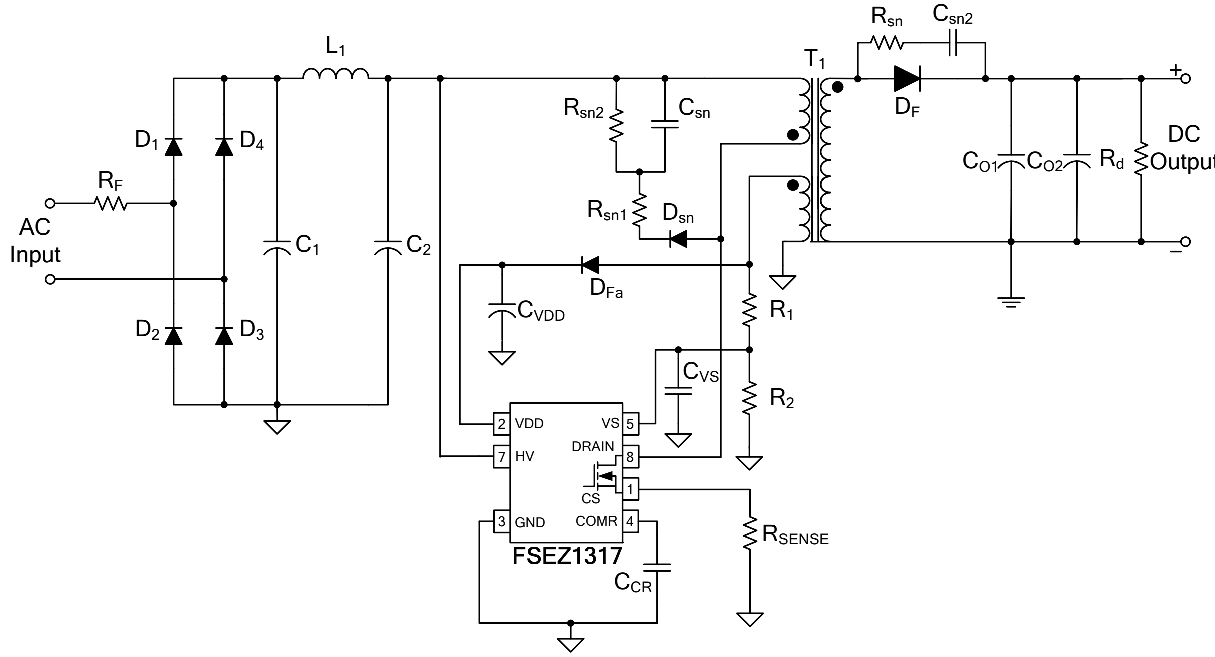


Figure 2. Typical Application

Internal Block Diagram

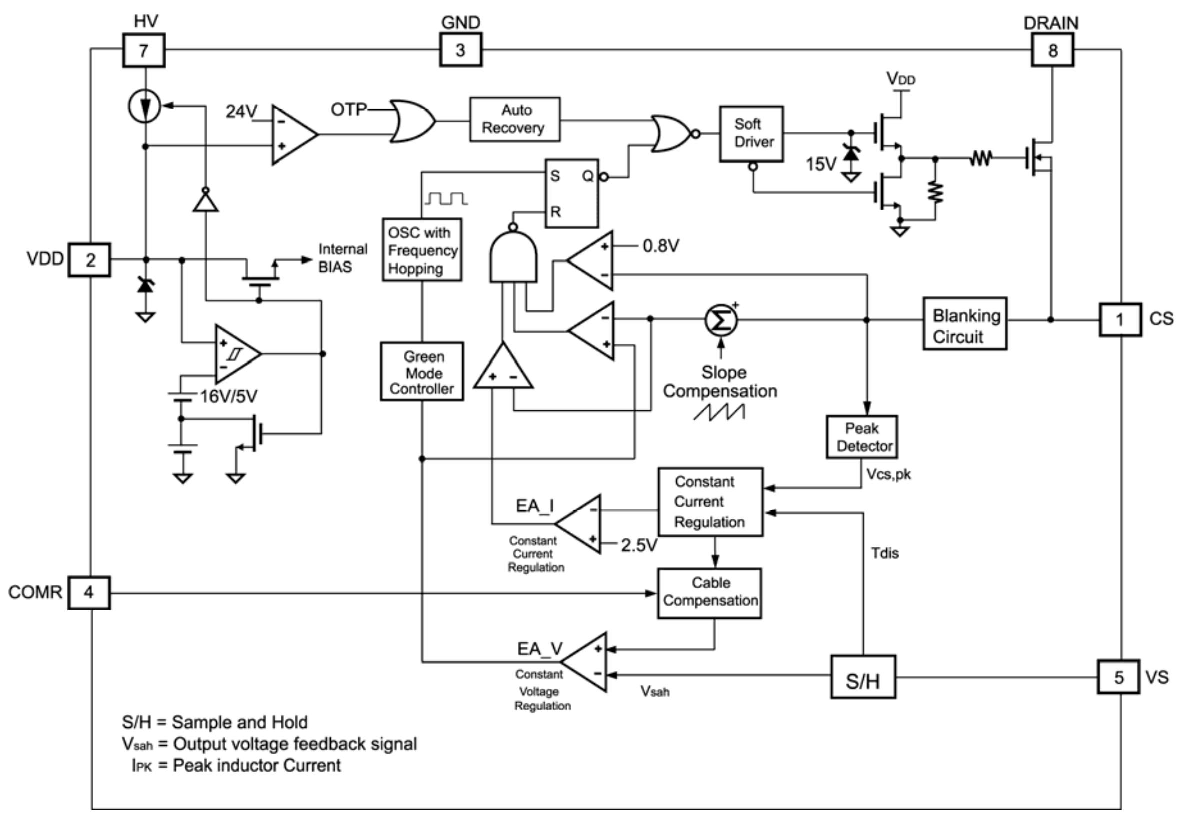
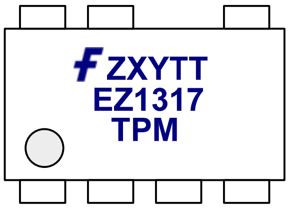


Figure 3. Functional Block Diagram

Marking Information



F: Fairchild Logo
Z: Plant Code
X: 1-Digit Year Code
Y: 1-Digit Week Code
TT: 2-Digit Die Run Code
T: Package Type (M=SOP, N=DIP)
P: Y=Green Package
M: Manufacture Flow Code

Figure 4. Top Mark

Pin Configuration

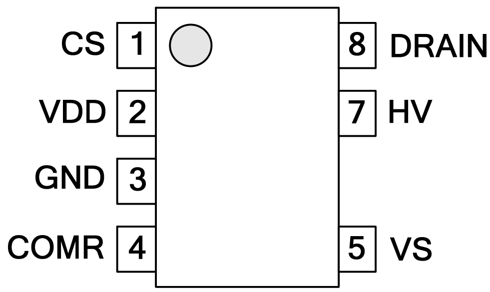


Figure 5. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	CS	**Current Sense**. This pin connects a current-sense resistor, to detect the MOSFET current for peak-current-mode control in CV mode, and provides the output-current regulation in CC mode.
2	VDD	**Power Supply**. IC operating current and MOSFET driving current are supplied using this pin. This pin is connected to an external V_{DD} capacitor of typically 10µF. The threshold voltages for startup and turn-off are 16V and 5V, respectively. The operating current is lower than 5mA.
3	GND	**Ground**
4	COMR	**Cable Compensation**. This pin connects a 1µF capacitor between the COMR and GND pins for compensation voltage drop due to output cable loss in CV mode.
5	VS	**Voltage Sense**. This pin detects the output voltage information and discharge time based on voltage of auxiliary winding.
7	HV	**High Voltage**. This pin connects to bulk capacitor for high-voltage startup.
8	DRAIN	**Driver Output**. Power MOSFET drain. This pin is the high-voltage power MOSFET drain.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
V_{HV}	HV Pin Input Voltage			500	V
V_{VDD}	DC Supply Voltage(1,2)			30	V
V_{VS}	VS Pin Input Voltage		-0.3	7.0	V
V_{CS}	CS Pin Input Voltage		-0.3	7.0	V
V_{COMV}	Voltage Error Amplifier Output Voltage		-0.3	7.0	V
V_{COMI}	Current Error Amplifier Output Voltage		-0.3	7.0	V
V_{DS}	Drain-Source Voltage			700	V
I_D	Continuous Drain Current	T_A=25°C		1	A
		T_A=100°C		0.6	A
I_{DM}	Pulsed Drain Current			4	A
E_{AS}	Single Pulse Avalanche Energy			50	mJ
I_{AR}	Avalanche Current			1	A
P_D	Power Dissipation (T_A < 50°C)			660	mW
θ_{JA}	Thermal Resistance (Junction-to-Air)	SOP		150	°C/W
		DIP		95	°C/W
Ψ_{JT}	Thermal Resistance (Junction-to-Case)	SOP		39	°C/W
		DIP		25	°C/W
T_J	Operating Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Reflow, 3 Cycles)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JEDEC-JESD22_A114 (All Pins Except HV Pin)		5000	V
		Charged Device Model, JEDEC-JESD22_C101 (All Pins Except HV Pin)		2000	

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to the GND pin.
3. ESD ratings including HV pin: HBM=1000V, CDM=1000V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Units
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

Unless otherwise specified, V_{DD}=15V and T_A=25°C.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
V_{DD} Section							
V_{OP}	Continuously Operating Voltage					23	V
V_{DD-ON}	Turn-On Threshold Voltage			15	16	17	V
V_{DD-OFF}	Turn-Off Threshold Voltage			4.5	5.0	5.5	V
I_{DD-OP}	Operating Current				2.5	5.0	mA
$I_{DD-GREEN}$	Green-Mode Operating Supply Current				0.95	1.20	mA
V_{DD-OVP}	V_{DD} Over-Voltage-Protection Level (OVP)			23	24	25	V
$V_{DD-OVP-HYS}$	Hysteresis Voltage for V_{DD} OVP			1.5	2.0	2.5	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage-Protection Debounce Time			50	200	300	μs
HV Startup Current Source Section							
V_{HV-MIN}	Minimum Startup Voltage on HV Pin					50	V
I_{HV}	Supply Current Drawn from HV Pin		V_{DC}=100V		1.5	3.0	mA
I_{HV-LC}	Leakage Current after Startup		HV=500V, V_{DD}= V_{DD-OFF}+1V		0.96	3.00	μA
Oscillator Section							
f_{OSC}	Frequency	Center Frequency		47	50	53	kHz
		Frequency Hopping Range		±1.5	±2.0	±2.5	
$f_{OSC-N-MIN}$	Minimum Frequency at No-Load				370		Hz
$f_{OSC-CM-MIN}$	Minimum Frequency at CCM				13		kHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation		V_{DD}=10~25V,		1	2	%
f_{DT}	Frequency Variation vs. Temperature Deviation		T_A=-40°C to 105°C			15	%
Voltage-Sense Section							
I_{tc}	IC Bias Current				10		μA
$V_{BIAS-COMV}$	Adaptive Bias Voltage Dominated by V_{COMV}		R_{VS}=20kΩ		1.4		V
Current-Sense Section							
t_{PD}	Propagation Delay to GATE Output				90	200	ns
t_{MIN-N}	Minimum On Time at No-Load			700	850	1050	ns
V_{TH}	Threshold Voltage for Current Limit				0.8		V
Voltage-Error-Amplifier Section							
V_{VR}	Reference Voltage			2.475	2.500	2.525	V
V_N	Green-Mode Starting Voltage on EA_V		f_{OSC}-2kHz		2.5		V
V_G	Green-Mode Ending Voltage on EA_V		f_{OSC}=1kHz		0.4		V
Current-Error-Amplifier Section							
V_{IR}	Reference Voltage			2.475	2.500	2.525	V
Cable Compensation Section							
V_{COMR}	COMR Pin for Cable Compensation				0.75		V

Continued on the following page…

Electrical Characteristics (Continued)

Unless otherwise specified, V_{DD}=15V and T_A=25℃.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Internal MOSFET Section(4)						
DCY_{MAX}	Maximum Duty Cycle		70	75	80	%
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	700			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D=250µA, Referenced to T_A=25°C		0.53		V/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	I_D=0.5A, V_{GS}=10V		13	16	Ω
I_S	Maximum Continuous Drain-Source Diode Forward Current				1	A
I_{DSS}	Drain-Source Leakage Current	V_{DS}=700V, T_A=25°C			10	µA
		V_{DS}=560V, T_A=100°C			100	µA
t_{D-ON}	Turn-On Delay Time	V_{DS}=350V, I_D=1A, R_G=25Ω(5)		10	30	ns
t_{D-OFF}	Turn-Off Delay Time			20	50	ns
C_{ISS}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f_S=1MHz		175	200	pF
C_{OSS}	Output Capacitance			23	25	pF
Over-Temperature-Protection Section						
T_{OTP}	Threshold Temperature for OTP(6)		+130	+140	+150	°C

Notes:

4. These parameters, although guaranteed, are not 100% tested in production.
5. Pulse test: pulsewidth ≦ 300µs, duty cycle ≦ 2%.
6. When the Over-temperature protection is activated, the power system enter auto restart mode and output is disabled.

Typical Performance Characteristics

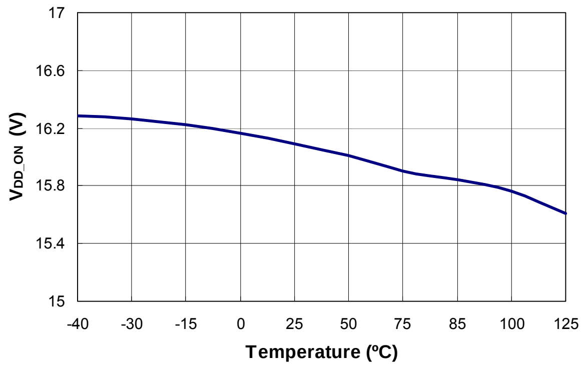


Figure 6. Turn-On Threshold Voltage ($V_{DD\text{-}ON}$) vs. Temperature

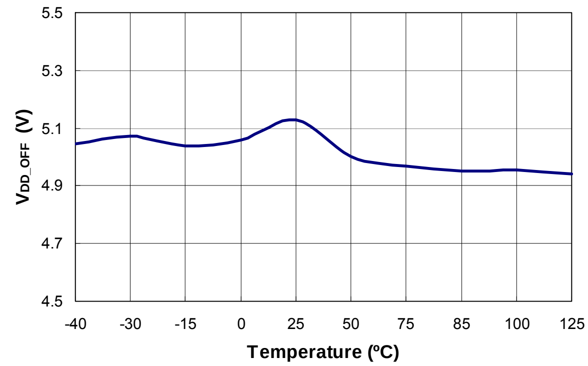


Figure 7. Turn-Off Threshold Voltage ($V_{DD\text{-}OFF}$) vs. Temperature

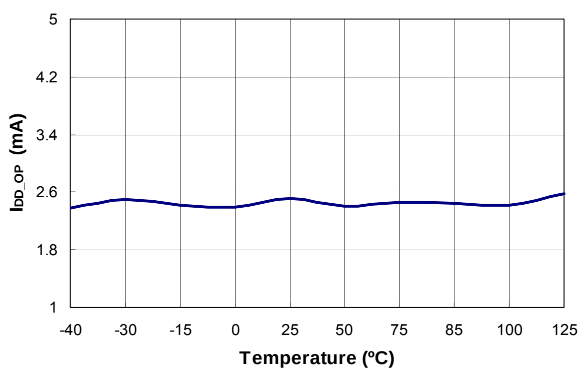


Figure 8. Operating Current ($I_{DD\text{-}OP}$) vs. Temperature

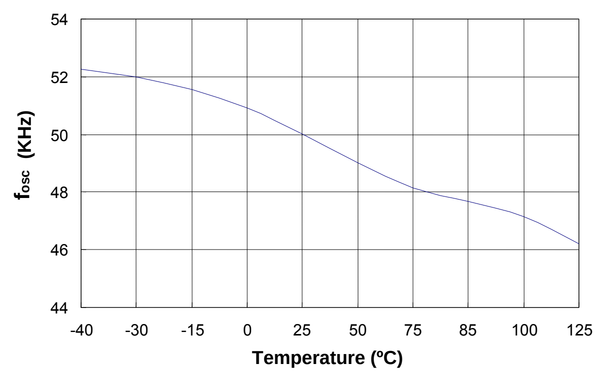


Figure 9. Center Frequency (f_{OSC}) vs. Temperature

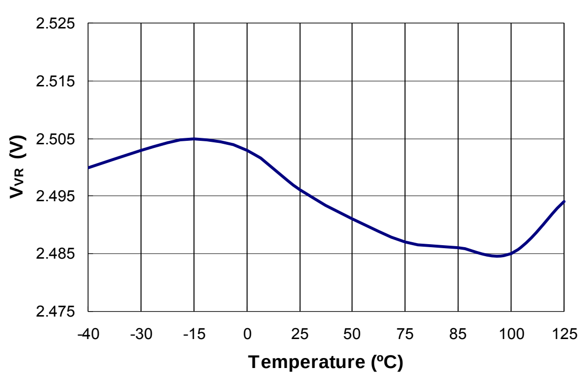


Figure 10. Reference Voltage (V_{VR}) vs. Temperature

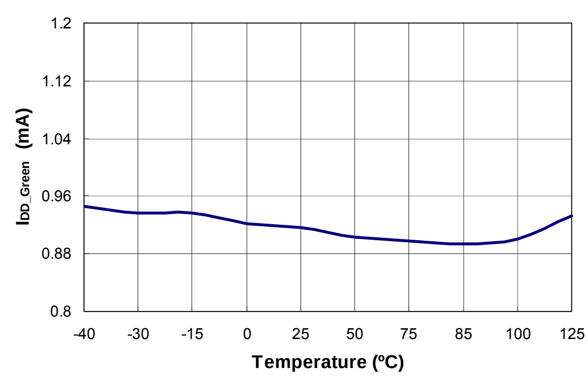


Figure 11. Green Mode Operating Supply Current ($I_{DD\text{-}GREEN}$) vs. Temperature

Typical Performance Characteristics (Continued)

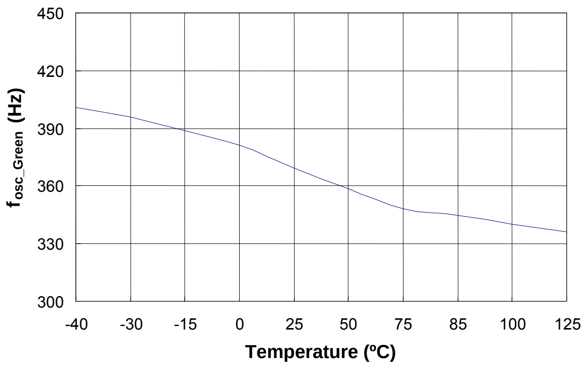


Figure 12. Minimum Frequency at No Load ($f_{OSC-N-MIN}$) vs. Temperature

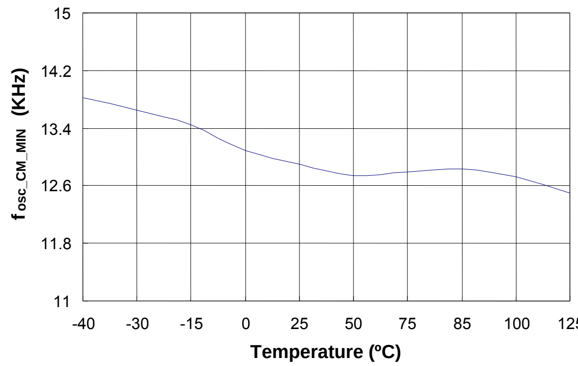


Figure 13. Minimum Frequency at CCM ($f_{OSC-CM-MIN}$) vs. Temperature

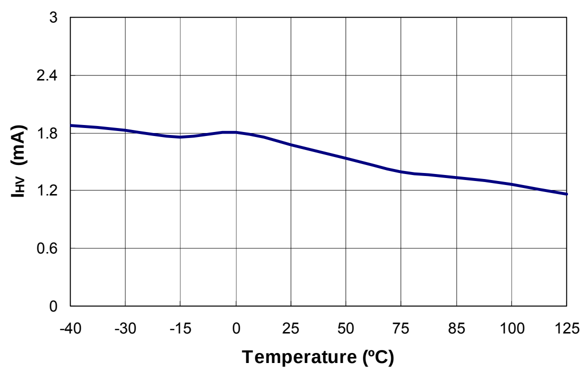


Figure 14. Supply Current Drawn from HV Pin (I_{HV}) vs. Temperature

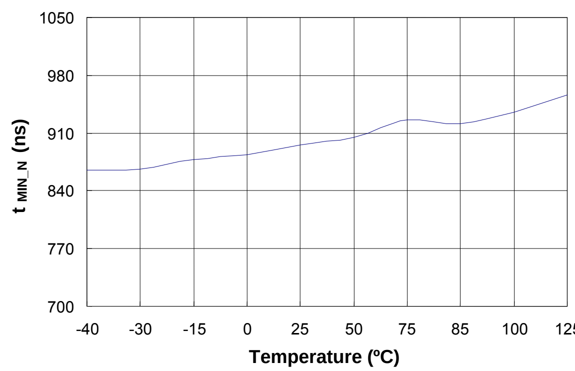


Figure 15. Minimum On Time at No Load (t_{MIN-N}) vs. Temperature

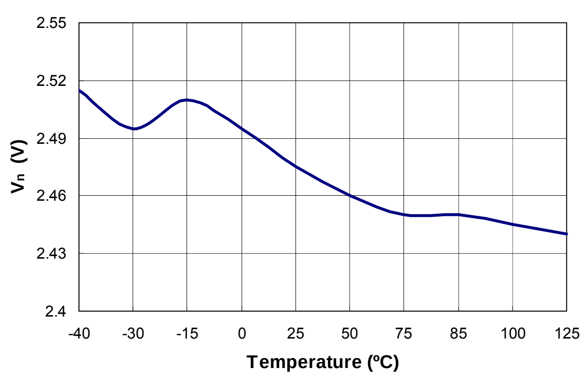


Figure 16. Green Mode Starting Voltage on EA_V (V_N) vs. Temperature

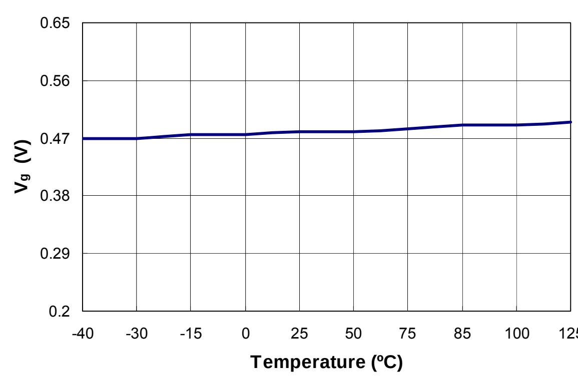


Figure 17. Green Mode Ending Voltage on EA_V (V_G) vs. Temperature

Typical Performance Characteristics (Continued)

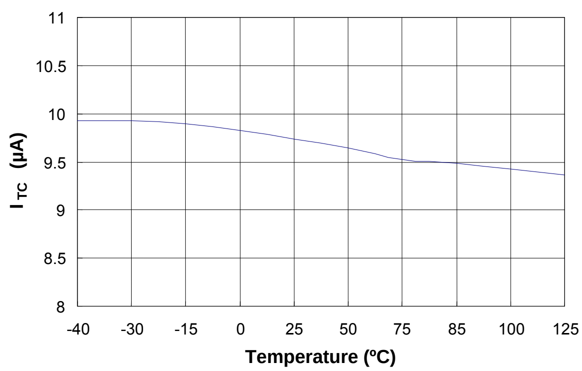


Figure 18. IC Bias Current (I_{tc}) vs. Temperature

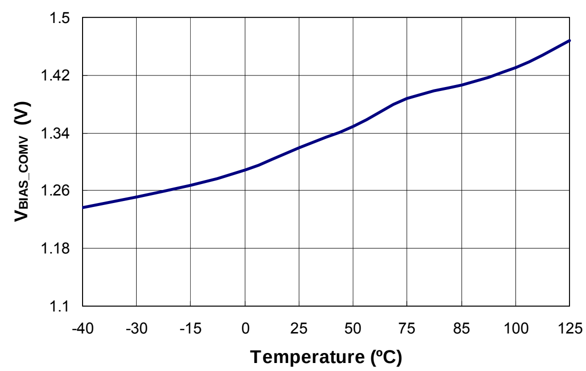


Figure 19. Adaptive Bias Voltage Dominated by V_{COMV} ($V_{BIAS\text{-}COMV}$) vs. Temperature

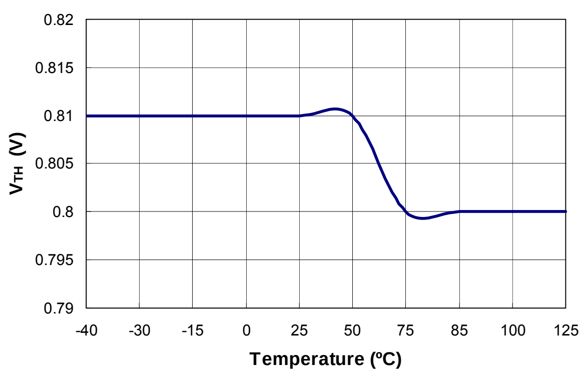


Figure 20. Threshold Voltage for Current Limit (V_{TH}) vs. Temperature

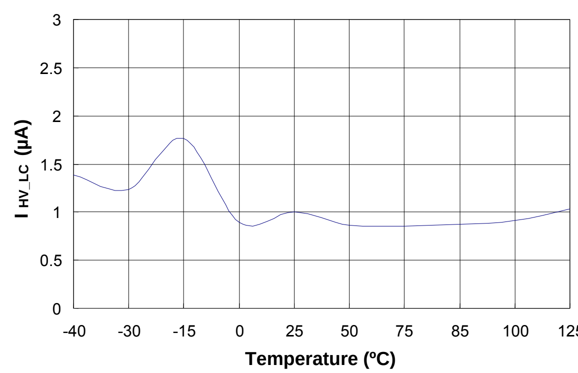


Figure 21. Leakage Current after Startup ($I_{HV\text{-}LC}$) vs. Temperature

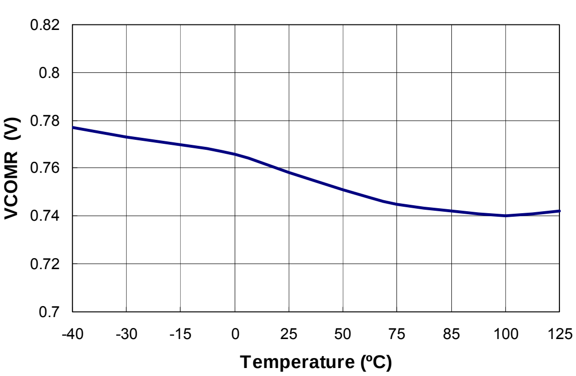


Figure 22. Variation Test Voltage on COMR Pin for Cable Compensation (V_{COMR}) vs. Temperature

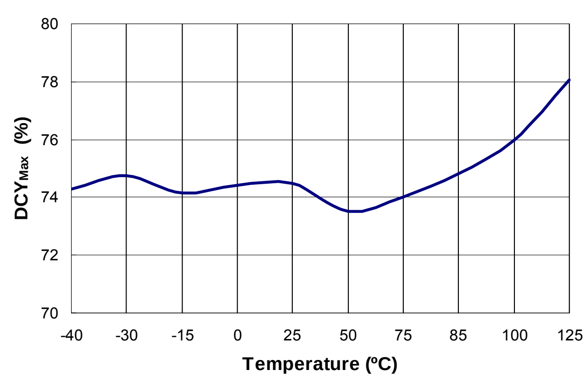


Figure 23. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

Functional Description

Figure 24 shows the basic circuit diagram of primary-side regulated flyback converter, with typical waveforms shown in Figure 25. Generally, discontinuous conduction mode (DCM) operation is preferred for primary-side regulation because it allows better output regulation. The operation principles of DCM flyback converter are as follows:

During the MOSFET on time (t_{ON}), input voltage (V_{DL}) is applied across the primary-side inductor (L_m). Then MOSFET current (I_{ds}) increases linearly from zero to the peak value (I_{pk}). During this time, the energy is drawn from the input and stored in the inductor.

When the MOSFET is turned off, the energy stored in the inductor forces the rectifier diode (D) to be turned on. While the diode is conducting, the output voltage (V_o), together with diode forward-voltage drop (V_F), is applied across the secondary-side inductor ($L_m \times N_s^2/N_p^2$) and the diode current (I_D) decreases linearly from the peak value ($I_{pk} \times N_p/N_s$) to zero. At the end of inductor current discharge time (t_{DIS}), all the energy stored in the inductor has been delivered to the output.

When the diode current reaches zero, the transformer auxiliary winding voltage (V_w) begins to oscillate by the resonance between the primary-side inductor (L_m) and the effective capacitor loaded across the MOSFET.

During the inductor current discharge time, the sum of output voltage and diode forward-voltage drop is reflected to the auxiliary winding side as $(V_o+V_F) \times N_a/N_s$. Since the diode forward-voltage drop decreases as current decreases, the auxiliary winding voltage reflects the output voltage best at the end of diode conduction time where the diode current diminishes to zero. Thus, by sampling the winding voltage at the end of the diode conduction time, the output voltage information can be obtained. The internal error amplifier for output voltage regulation (EA_V) compares the sampled voltage with internal precise reference to generate error voltage (V_{COMV}), which determines the duty cycle of the MOSFET in CV mode.

Meanwhile, the output current can be estimated using the peak drain current and inductor current discharge time because output current is same as the average of the diode current in steady state.

The output current estimator picks up the peak value of the drain current with a peak detection circuit and calculates the output current using the inductor discharge time (t_{DIS}) and switching period (t_s). This output information is compared with internal precise reference to generate error voltage (V_{COMI}), which determines the duty cycle of the MOSFET in CC mode. With Fairchild's innovative technique TRUECURRENT™, constant current (CC) output can be precisely controlled.

Among the two error voltages, V_{COMV} and V_{COMI}, the smaller one determines the duty cycle. Therefore, during constant voltage regulation mode, V_{COMV} determines the duty cycle while V_{COMI} is saturated to HIGH. During constant current regulation mode, V_{COMI} determines the duty cycle while V_{COMV} is saturated to HIGH.

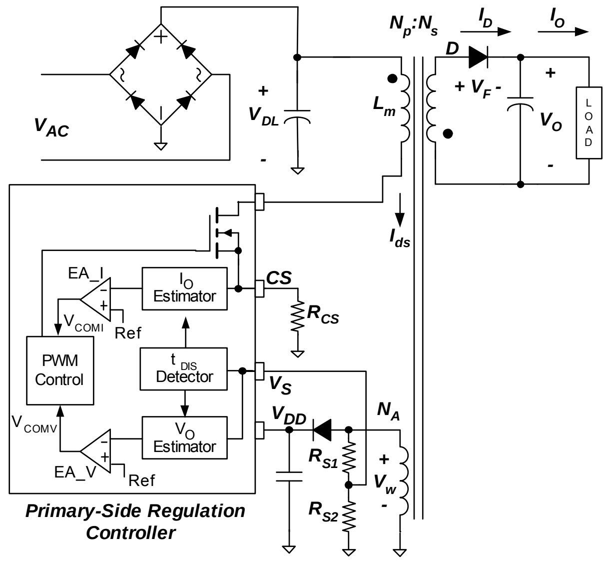


Figure 24. Simplified PSR Flyback Converter Circuit

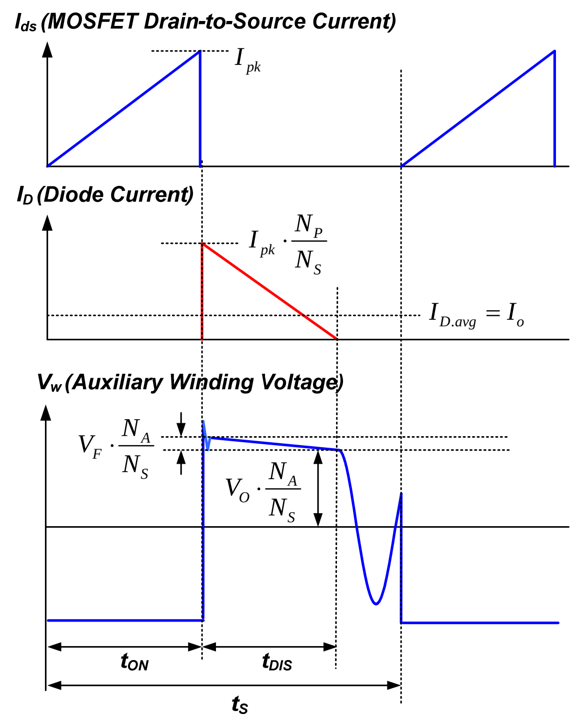


Figure 25. Key Waveforms of DCM Flyback Converter

Cable Voltage Drop Compensation

In cellular phone charger applications, the battery is located at the end of cable, which typically causes several percentage of voltage drop on the battery voltage. FSEZ1317 has a built-in cable voltage drop compensation that provides a constant output voltage at the end of the cable over the entire load range in CV mode. As load increases, the voltage drop across the cable is compensated by increasing the reference voltage of the voltage regulation error amplifier.

Operating Current

The FSEZ1317 operating current is as small as 2.5mA, which results in higher efficiency and reduces the V_{DD} hold-up capacitance requirement. Once FSEZ1317 enters "deep" green mode, the operating current is reduced to 0.95mA, assisting the power supply in meeting power conservation requirements.

Green-Mode Operation

The FSEZ1317 uses voltage regulation error amplifier output (V_{COMV}) as an indicator of the output load and modulates the PWM frequency as shown in Figure 26. The switching frequency decreases as the load decreases. In heavy load conditions, the switching frequency is fixed at 50kHz. Once V_{COMV} decreases below 2.5V, the PWM frequency linearly decreases from 50kHz. When FSEZ1317 enters deep green mode, the PWM frequency is reduced to a minimum frequency of 370Hz, thus gaining power saving to meet international power conservation requirements.

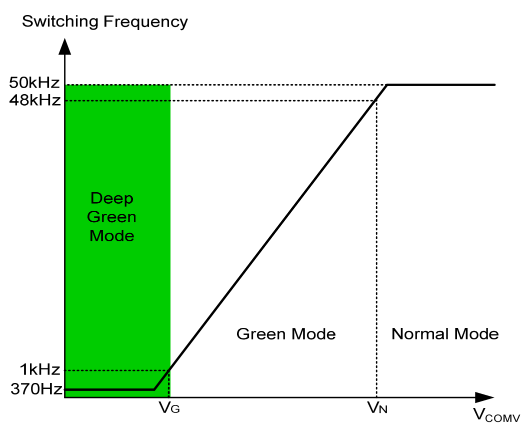


Figure 26. Switching Frequency in Green Mode

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. FSEZ1317 has an internal frequency hopping circuit that changes the switching frequency between 47kHz and 53kHz over the period shown in Figure 27.

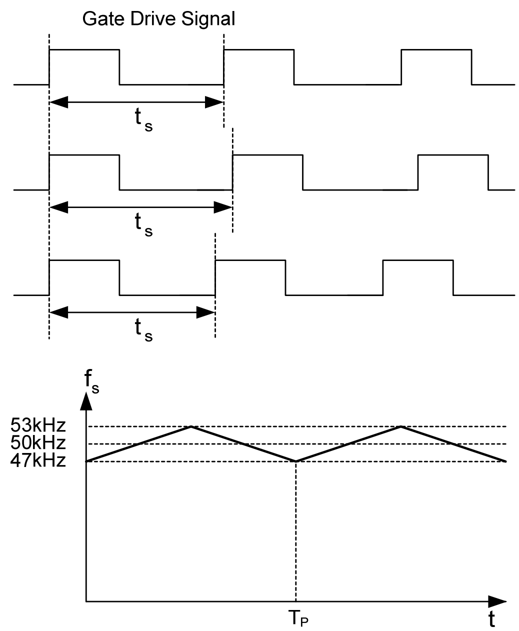


Figure 27. Frequency Hopping

High-Voltage Startup

Figure 28 shows the HV-startup circuit for FSEZ1317 applications. The HV pin is connected to the line input or bulk capacitor through a resistor, R_{START} (100kΩ recommended). During startup status, the internal startup circuit is enabled. Meanwhile, line input supplies the current, $I_{STARTUP}$, to charge the hold-up capacitor, C_{DD}, through R_{START}. When the V_{DD} voltage reaches $V_{DD\text{-}ON}$, the internal startup circuit is disabled, blocking $I_{STARTUP}$ from flowing into the HV pin. Once the IC turns on, C_{DD} is the only energy source to supply the IC consumption current before the PWM starts to switch. Thus, C_{DD} must be large enough to prevent V_{DD} from dropping down to $V_{DD\text{-}OFF}$ before the power can be delivered from the auxiliary winding.

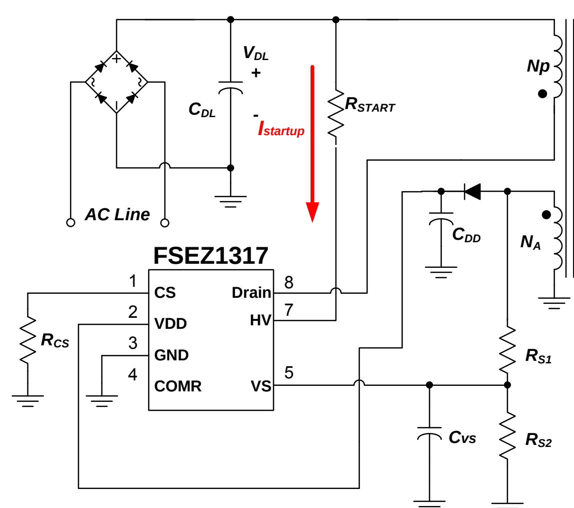


Figure 28. HV Startup Circuit

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16V and 5V, respectively. During startup, the hold-up capacitor must be charged to 16V through the startup resistor to enable the FSEZ1317. The hold-up capacitor continues to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} is not allowed to drop below 5V during this startup process. This UVLO hysteresis window ensures that hold-up capacitor properly supplies V_{DD} during startup.

Protections

The FSEZ1317 has several self-protection functions, such as Over-Voltage Protection (OVP), Over-Temperature Protection (OTP), and pulse-by-pulse current limit. All the protections are implemented as auto-restart mode. Once the abnormal condition occurs, the switching is terminated and the MOSFET remains off, causing V_{DD} to drop. When V_{DD} drops to the V_{DD} turn-off voltage of 5V, internal startup circuit is enabled again and the supply current drawn from the HV pin charges the hold-up capacitor. When V_{DD} reaches the turn-on voltage of 16V, normal operation resumes. In this manner, the auto-restart alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated *(see Figure 29).*

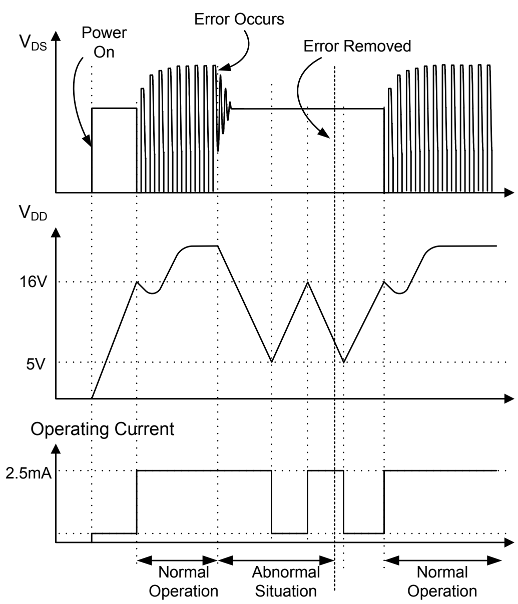


Figure 29. Auto-Restart Operation

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents damage from over-voltage conditions. If the V_{DD} voltage exceeds 24V at open-loop feedback condition, OVP is triggered and the PWM switching is disabled. The OVP has a debounce time (typically 200µs) to prevent false triggering due to switching noises.

Over-Temperature Protection (OTP)

The built-in temperature-sensing circuit shuts down PWM output if the junction temperature exceeds 140°C.

Pulse-by-pulse Current Limit

When the sensing voltage across the current-sense resistor exceeds the internal threshold of 0.8V, the MOSFET is turned off for the remainder of switching cycle. In normal operation, the pulse-by-pulse current limit is not triggered since the peak current is limited by the control loop.

Leading-Edge Blanking (LEB)

Each time the power MOSFET switches on, a turn-on spike occurs at the sense resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver. As a result conventional RC filtering can be omitted.

Gate Output

The FSEZ1317 output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 15V Zener diode to protect the power MOSFET transistors against undesired over-voltage gate signals.

Built-In Slope Compensation

The sensed voltage across the current-sense resistor is used for current mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillations due to peak-current mode control. The FSEZ1317 has a synchronized, positive-slope ramp built-in at each switching cycle.

Noise Immunity

Noise from the current sense or the control signal can cause significant pulsewidth jitter, particularly in continuous-conduction mode. While slope compensation helps alleviate these problems, further precautions should still be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FSEZ1317, and increasing the power MOS gate resistance are advised.

Typical Application Circuit (Primary-Side Regulated Flyback Charger)

Application	Fairchild Devices	Input Voltage Range	Output	Output DC cable
Cell Phone Charger	FSEZ1317 (SOP-7)	90~265V_{AC}	5V/0.7A (3.5W)	AWG26, 1.8 Meter

Features

- High efficiency (>65.5% at full load) meeting EPS 2.0 regulation with enough margin
- Low standby (Pin<30mW at no-load condition)

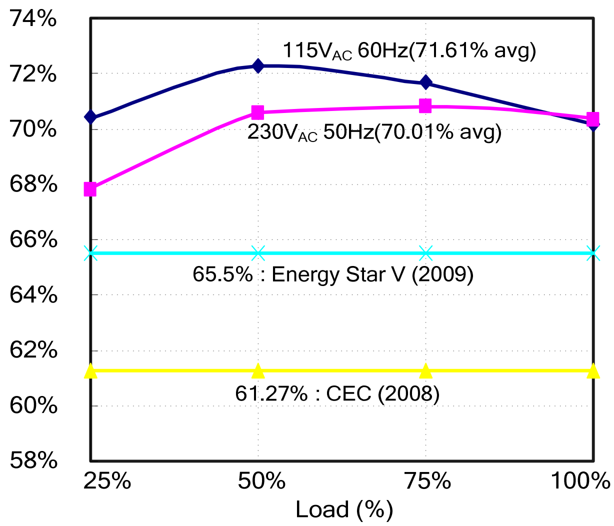


Figure 30. Measured Efficiency

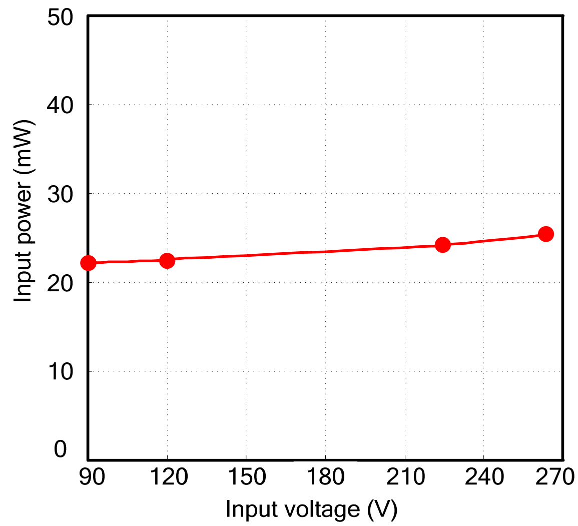


Figure 31. Standby Power

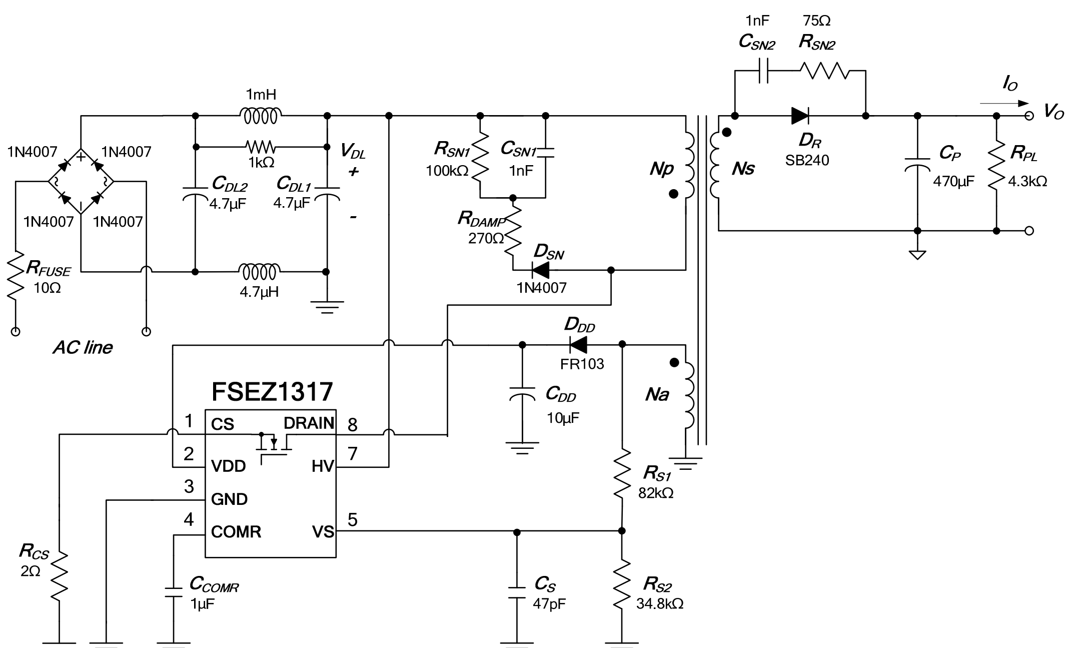


Figure 32. Schematic of Typical Application Circuit

Typical Application Circuit (Continued)

Transformer Specification

- Core: EE16
- Bobbin: EE16

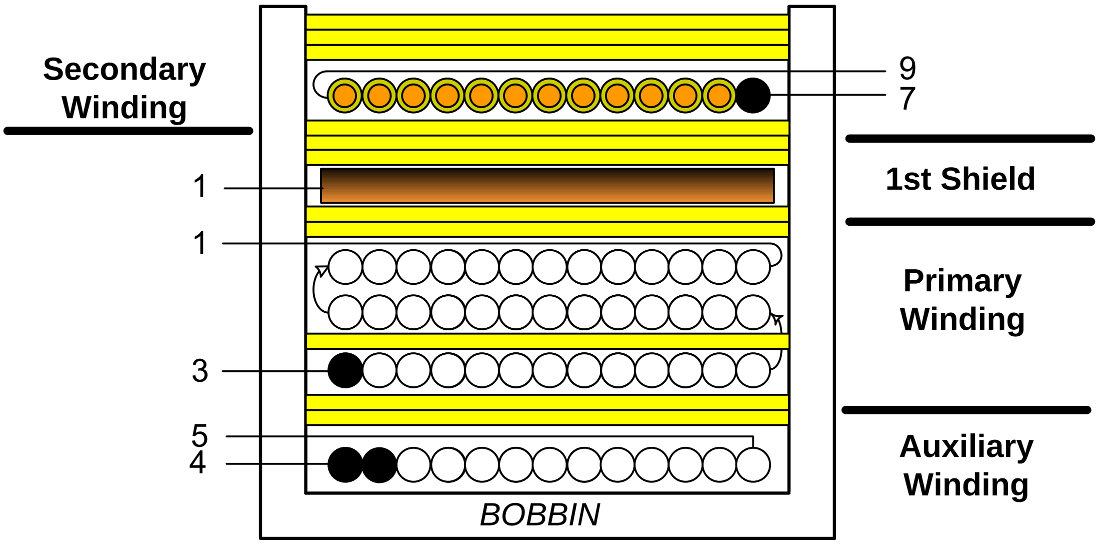


Figure 33. Transformer Specification

Notes:
7. When W4R's winding is reversed winding, it must wind one layer.
8. When W2 is winding, it must wind three layers and put one layer of tape after winding the first layer.

No.	Terminal		Wire	t_s	Insulation	Barrier Tape	
	S	F			t_s	Primary	Seconds
W1	4	5	2UEW 0.23*2	15	2		
W2	3	1	2UEW 0.17*1	41	1		
				39	0		
				37	2		
W3	1	-	COPPER SHIELD	1.2	3		
W4	7	9	TEX-E 0.55*1	9	3		
			CORE ROUNDING TAPE		3		

	Pin	Specification	Remark
Primary-Side Inductance	1 – 3	2.25mH ± 7%	100kHz, 1V
Primary-Side Effective Leakage	1 – 3	80μH ± 5%	Short One of the Secondary Windings

Physical Dimensions

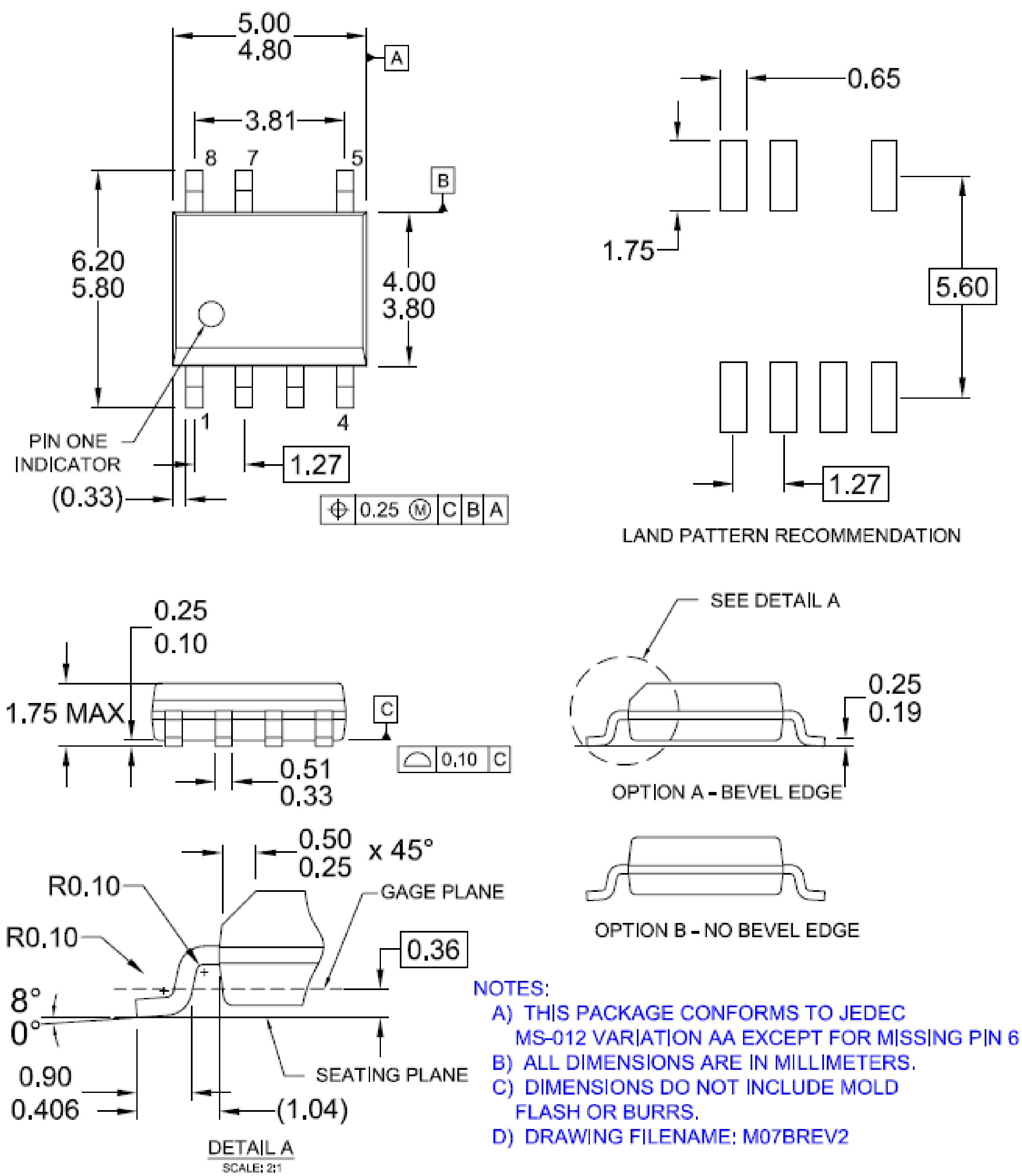


Figure 34. 7-Lead, Small Outline Package (SOP-7)

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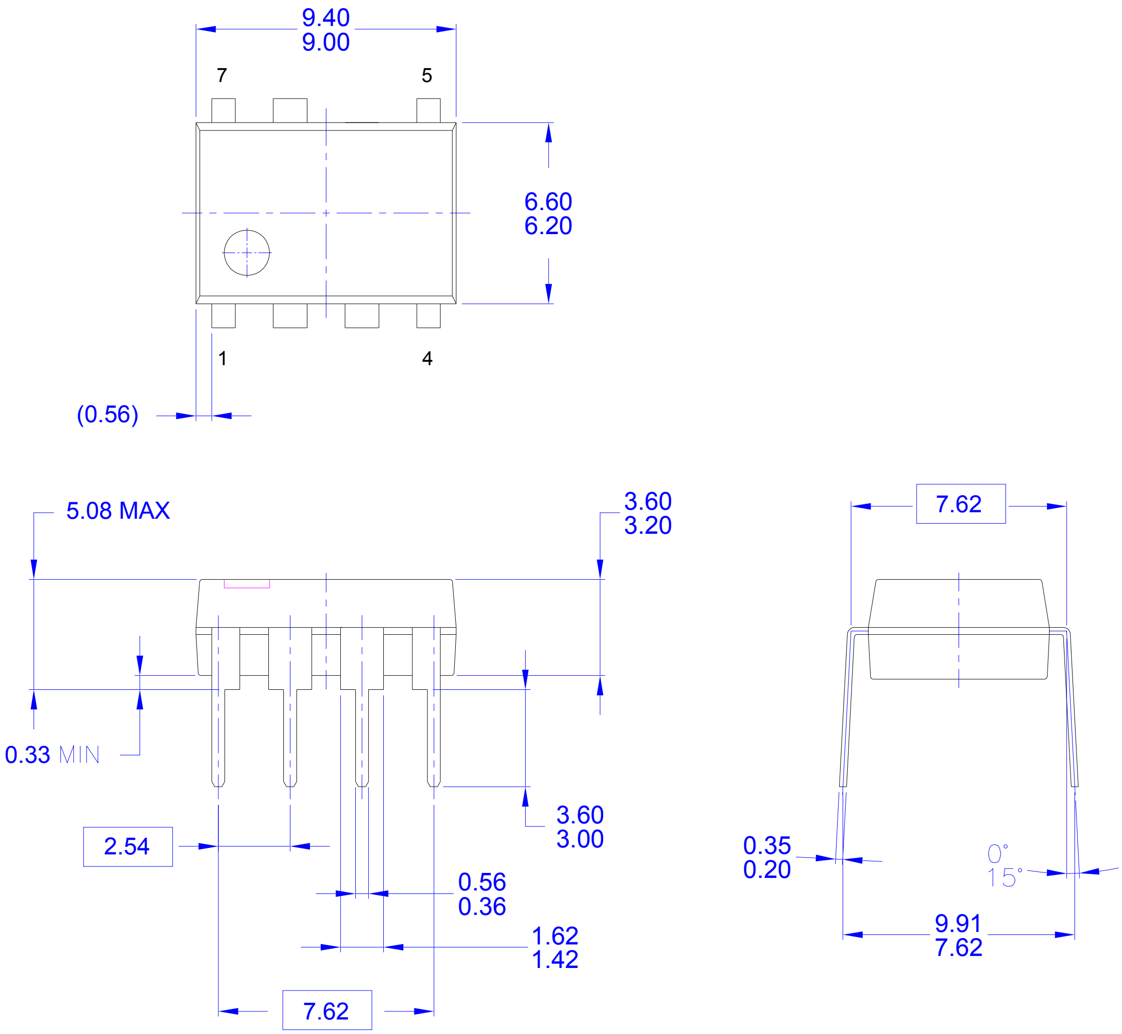
Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE COMPLIES TO JEDEC MS-001, VARIATION BA, EXCEPT FOR TERMINAL COUNT (7 RATHER THAN 8)

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

E) DRAWING FILENAME AND REVISION: MKT-NA07BREV2

Figure 35. 7-Lead, Dual-inline Package (DIP-7)

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