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May 2014

FTL75939
Configurable Reset Timer with Integrated Load Switch

Features

- Factory Programmed Reset Delay: 7.5 s
- Factory Programmed Reset Pulse: 400 ms
- Factory Customized Turn-on Time: 2.3 s
- Factory Customized Turn-off Delay: 7.3 s
- Adjustable Reset Delay Option with External Resistor
- Low I_{CCT} Saves Power Interfacing to Low-Voltage Chips
- Off Pin Turns Off Load Switch to Maintain Battery Charge during Shipment and Inventory. Ready to use Right Out of the Box
- Input Voltage Operating Range: 1.2 V to 5.5 V
- Over-Voltage Protection: Allow Input Pins > V_{BAT}
- Typical R_{ON}: 21 mΩ (Typ.) at V_{BAT}=4.5 V
- Slew Rate / Inrush Control with t_R: 2.7 ms (Typical)
- 3.8 A / 4.5 A Maximum Continuous Current (JEDEC 2S2P, No VIA / with Thermal VIA)
- Output Capacitor Discharge Function
- Zero-Second Test-Mode Enable
- Low < 0.2 µA Typical Shutdown Current
- IEC61000-4-2, , Level 4 compliant SYS_WAKE Pin
- ESD Protected:
  - 8 kV HBM ESD (per JESD22-A114)
  - 10 kV HBM ESD (Pin to Pin, V_{BAT} & V_{OUT})
  - 2 kV CDM (per JESD22-C101)

Applications

- Smart Phones, Tablet PCs
- Storage, DSLR, and Portable Devices

Description

The FTL75939 is both a timer for resetting a mobile device and an advanced load management switch for applications requiring a highly integrated solution.

If the mobile device is off, holding /SR0 LOW (by pressing power-on key) for 2.3 s ±20% turns on the PMIC.

As a reset timer, it has one input and one fixed delay output. It generates a fixed delay of 7.5 s ±20% by disconnecting the PMIC from the battery power supply for 400 ms ±20%. Then the load switch is turned on again to reconnect the battery to the PMIC such that PMIC goes into power-on sequence. The reset delay can be customized by connecting an external resistor to the DELAY_ADJ pin. *Refer to Table 4.*

As an advanced load management switch, the FTL75939 disconnects loads powered from the DC power rail (<6 V) with stringent off-state current targets and high load capacitances (up to 200 µF). The FTL75939 consists of a slew-rate controlled low-impedance MOSFET switch (21 mΩ typical at 4.5 V) that has exceptionally low off-state current drain (<0.2 µA Typical) to facilitate compliance with standby power requirements. The slew-rate-controlled turn-on characteristic prevents inrush current and the resulting excessive voltage drop on power rails.

The low I_{CCT} enables direct interface to lower-voltage chipsets without external translation, while maintaining low power consumption.

The device is packaged in advanced, fully green, 1.31 mm x 1.62 mm, Wafer-Level Chip-Scale Packaging (WLCSP) with backside laminate; providing excellent thermal conductivity, small footprint, and low electrical resistance for a wide application range.

Related Resources

For additional information, please contact:
http://www.fairchildsemi.com/cf/#Regional-Sales

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package	Packing Method
FTL75939UCX	UA	-40 to +85°C	12-Ball WLCSP (with backside laminate), 3x4 Array, 0.4 mm Pitch, 250 µm Ball, Nominal: 1.31 mm x 1.62 mm	3000 Units on Tape and Reel

Application Diagram

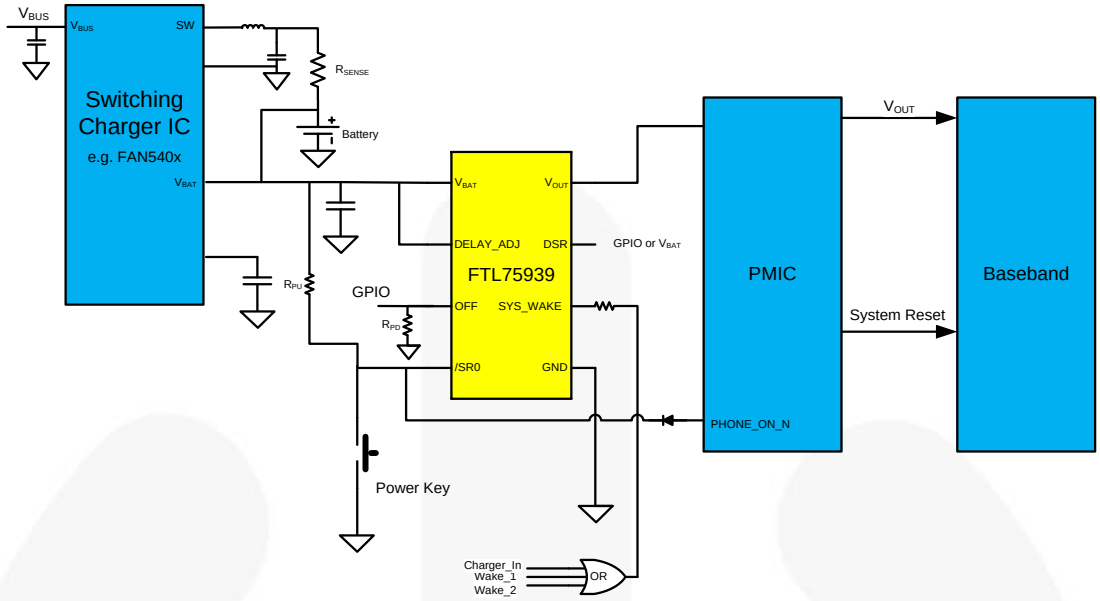


Figure 1. Typical Application with Stand Alone Switching Charger IC

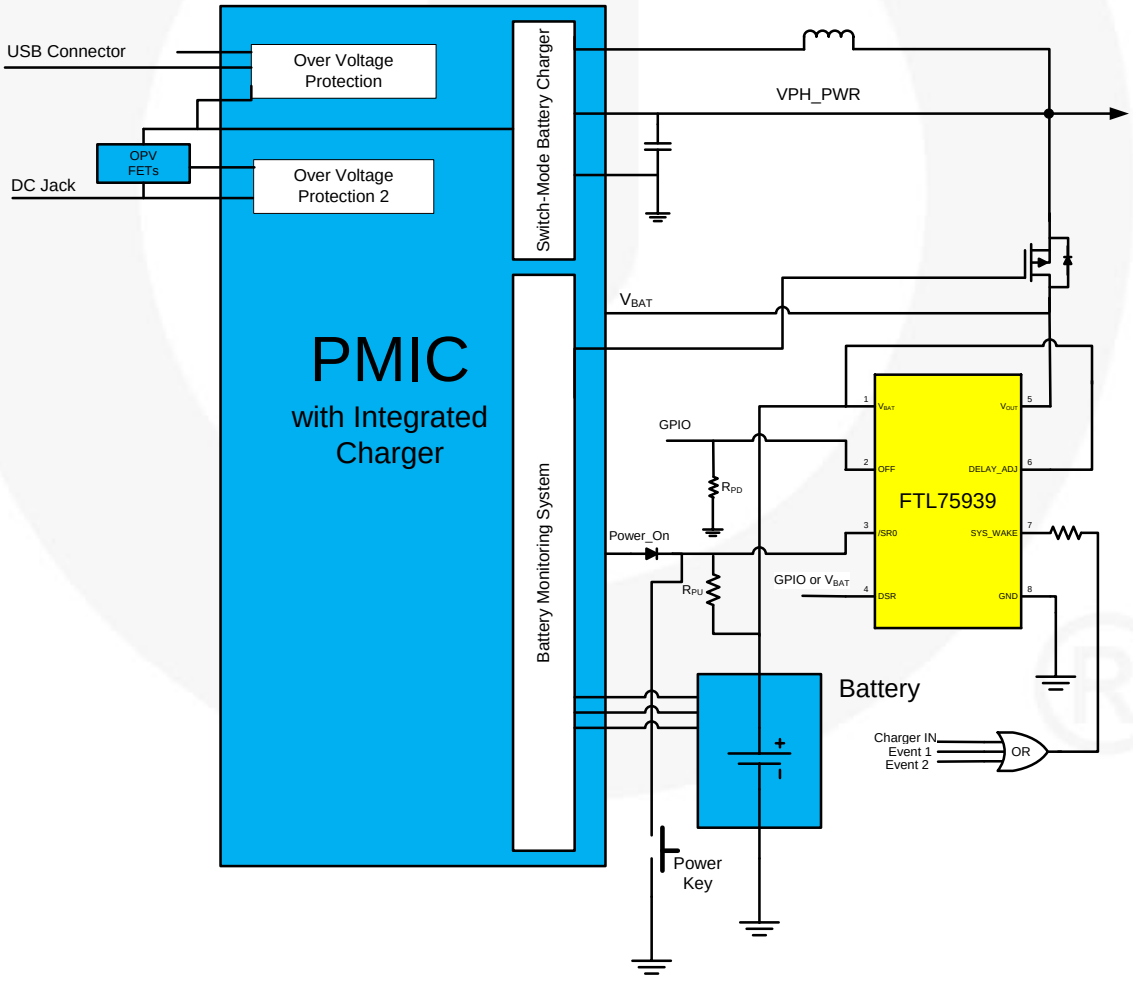


Figure 2. Typical Application PMIC with Integrated Charger

Functional Block Diagram

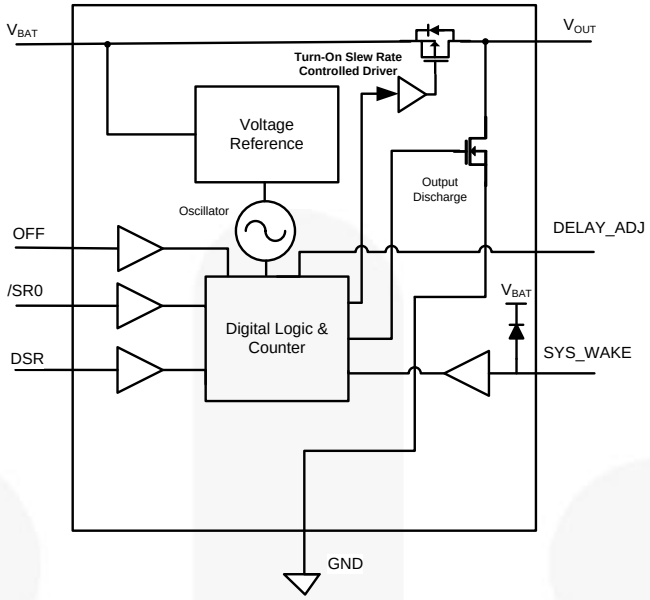


Figure 3. Block Diagram

Pin Configuration

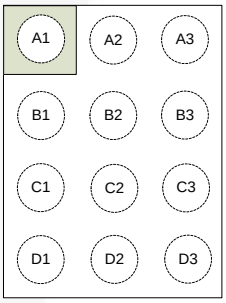


Figure 4. Top View

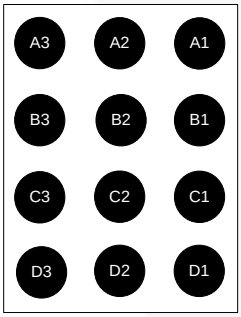


Figure 5. Bottom View

Pin Definitions

Pin #	Name	Description	
		Normal Operation	**0-Second Factory-Test Mode(1)**
A1, A2, A3	V_{OUT}	Switch Output	Switch Output
B1, B2, B3	V_{BAT}	Supply Input	Supply Input
C1	GND	Ground	Ground
C2	DSR	Delay selection input; connected to GPIO with 100 K pull-up or to V_{BAT} directly without pull-up resistor	Logic LOW
C3	/SR0	Power-on or reset input; active LOW.	Logic LOW
D1	DELAY_ADJ	Reset delay adjustment; MUST tie to V_{BAT} directly if not used. To adjust the reset delay, a resistor (R_{ADJ}) is connected between this pin and ground	Connected to V_{BAT} or GND
D2	OFF	Load switch disable; Rising Edge Triggered; changes load switch from ON state to OFF state.	Don't Care
D3	SYS_WAKE	System wake-up input; changes load switch from OFF state to ON state	Don't Care

Note:

1. 0-Second Factory Test Mode is for t_{VON} and t_{PHL1} only.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters	Condition	Min.	Max.	Unit
V_{BAT}	V_{BAT} to GND		-0.3	6.5	V
V_{OUT}	V_{OUT} to GND				
I_{SW}	Maximum Continuous Switch Current	2S2P JEDEC std. PCB		3.8	A
		2S2P + Thermal VIA JEDEC std. PCB		4.5	
P_D	Power Dissipation	I_{OUT}=4.5 A, R_{ON} = 20 mΩ (max)		0.41	W
V_{IN}	DC Input Voltage	/SR0, DSR, OFF, DELAY_ADJ	-0.5	6.5	V
		SYS_WAKE[2]		V_{BAT}+0.3	
I_{IK}	DC Input Diode Current	V_{BAT} < 0 V		-50	mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin			±100	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature, Soldering 10 Seconds			+260	°C
Θ_{JA}	Thermal Resistance, Junction-to-Ambient	2S2P JEDEC std. PCB		86	°C/W
		2S2P + Thermal VIA JEDEC std. PCB		48	
Θ_{JC}	Thermal Resistance, Junction-to-Case[3]			10.9	°C/W
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		8	kV
	Human Body Model, Pin to Pin[4]	V_{BAT}, V_{OUT}		10	
	IEC 61000-2-4, Level 4, for SYS_WAKE[5]	Air		15	
		Contact		8	
	Charged Device Model, JESD22-C101			2	

Notes:

2. SYS_WAKE operates up to 28 V if an external resistor is attached. A value of 100 kΩ is typically recommended.
3. Uniform temperature at bottom solder.
4. Test conditions: V_{BAT} vs. GND and V_{OUT} vs. GND.
5. A 100 kΩ resistor is required between SYS_WAKE and USB Charger In.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameters	Condition	Min.	Max.	Unit
V_{BAT}	Input Voltage[6]	V_{BAT}	1.2	5.5	V
V_{IN}		/SR0, DSR, OFF	0		
		SYS_WAKE	0	V_{BAT}	
V_{OUT}	Output Voltage		0	5.5	V
t_{RFC}	V_{BAT} Recovery Time After Power Down	V_{BAT}=0 V After Power Down, Rising to 0.5 V	5		ms
T_A	Free-Air Operating Temperature		-40	+85	°C

Note:

6. V_{BAT} should never be allowed to float while input pins are driven.

Electrical Characteristics

Unless otherwise noted, V_{BAT}=1.2 to 5.5 V and T_A=-40 to +85°C; typical values are at V_{BAT}=4.5 V and T_A=25°C.

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
Basic Operation						
I_{OFF}	Off Supply Current	V_{BAT}=4.5 V, V_{OUT}=Open, Load Switch=OFF			5.5	µA
I_{SD}	Shutdown Current	V_{BAT}=4.5 V, V_{OUT}=GND, Load Switch=OFF		0.2	5.5	µA
		V_{BAT}=3.8 V, V_{OUT}=GND, Load Switch=OFF		0.1	4.5	
R_{ON}	On Resistance	V_{BAT}=5.5 V, I_{OUT}=1 A(7)		20	24	mΩ
		V_{BAT}=4.5 V, I_{OUT}=1 A, T_A=25°C(7)		21	25	
		V_{BAT}=3.3 V, I_{OUT}=500 mA(7)		24	29	
		V_{BAT}=2.5 V, I_{OUT}=500 mA(7)		28	35	
		V_{BAT}=1.8 V, I_{OUT}=250 mA(7)		37	45	
		V_{BAT}=1.2 V, I_{OUT}=250 mA, T_A=25°C(7)		75	100	
R_{PD}	Output Discharge $R_{PULL\ DOWN}$	V_{BAT}=4.5 V, V_{OUT}= OFF, I_{FORCE}=20 mA, T_A=25°C		65	85	Ω
V_{IH}	Input High Voltage(8)	1.8 V<V_{BAT}≤5.5 V	1.2			V
		1.2 V≤V_{BAT}≤1.8 V	1.0			V
V_{IL}	Input Low Voltage(8)				0.45	V
I_{IN}	Input Leakage Current(8)	0 V ≤ V_{BAT} ≤ 5.5 V			±1.5	µA
I_{CCQ}	Quiescent Current	/SR0=5.5 V, DSR=5.5 V, SYS_WAKE=5.5 V, OFF =GND, I_{OUT}=0 mA, V_{BAT}=5.5 V, Load Switch=ON		5	7	µA
		/SR0=3.8 V, DSR=3.8 V, SYS_WAKE=3.8 V, OFF=GND, I_{OUT}=0 mA, V_{BAT}=3.8 V, Load Switch=ON		4	5.5	
I_{CCT}		/SR0=1.2 V or DSR=1.2 V or OFF=1.2 V, SYS_Wake=1.2 V, V_{BAT}=5.5 V, Load Switch=ON		7	12	µA
I_{CC}	Dynamic Supply Current	/SR0=GND, DSR=5.5 V, V_{BAT}=5.5 V, Load Switch=ON			60	µA

Notes:

7. This parameter is guaranteed by design and characterization; R_{ON} is tested with different voltage and current conditions in production.
8. Input pins are /SR0, OFF, DSR, and SYS_WAKE. Input pins should not be floated when V_{BAT} is connected to the power supply.

AC Electrical Characteristics

Unless otherwise noted, V_{BAT}=1.2 to 5.5 V and T_A=-40 to +85°C; typical values are at V_{BAT}=4.5 V and T_A=25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power-On and Reset Timing						
t_{VON}	Turn-On Time for V_{OUT}	C_L=5 pF, R_L=5 kΩ, DSR=HIGH, Figure 30	1.8	2.3	2.8	s
t_{PHL1}	Timer Delay before Reset	C_L=5 pF, R_L=5 kΩ, DSR=HIGH, Figure 31	6.0	7.5	9.0	s
t_{REC1}	Reset Timeout Delay of V_{OUT}	C_L=5 pF, R_L=5 kΩ, Figure 31	320	400	480	ms
Load Switch Turn-On Timing						
t_{DON}	Turn-On Delay[9]	V_{BAT}=4.5 V, R_L=5 Ω, C_L=100 µF, T_A=25°C, Figure 29		1.7		ms
t_R	V_{OUT} Rise Time[9]			2.7		ms
t_{ON}	Turn-On Time[9], SYS_WAKE to V_{OUT}			4.4		ms
Load Switch Turn-Off with Delay						
t_{SD}	Delay to Turn Off Load Switch	V_{BAT}=4.5 V, R_L=150 Ω, C_L=100 µF, T_A=25°C, DSR=HIGH, Figure 28	5.8	7.3	8.8	s
t_F	V_{OUT} Fall Time[9]			10.0		ms
t_{OFF}	Turn-Off[10,11]			7.3		s
Load Switch Zero-Second Turn-Off						
t_{SD}	Delay to Turn Off Load Switch	V_{BAT}=4.5 V, R_L=150 Ω, C_L=100 µF, T_A=25°C, DSR=LOW, Figure 28		0.6		ms
t_F	V_{OUT} Fall Time[9]			10.0		ms
t_{OFF}	Turn-Off[10,11]			10.6		ms

Notes:

9. $t_{ON}=t_R + t_{DON}$.
10. $t_{OFF}=t_F + t_{SD}$.
11. Output discharge enabled during off-state.

Zero-Second Factory Test Mode

Unless otherwise noted, V_{BAT}=1.2 to 5.5 V and T_A=-40 to +85°C; typical values are at V_{BAT}=4.5 V and T_A=25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{VON}	Turn-On Time for V_{OUT}	C_L=5 pF, R_L=5 kΩ, V_{OUT}=OFF, DSR=LOW, Figure 30		4		ms
t_{PHL1}	Timer Delay before Reset	C_L=5 pF, R_L=5 kΩ, V_{OUT}=ON, DSR=LOW, Figure 31		1		ms

Typical Characteristics

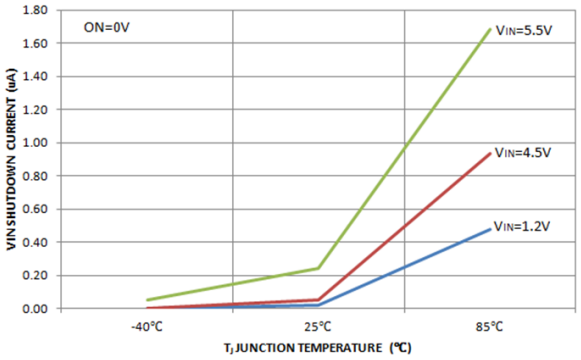


Figure 6. Shutdown Current vs. Temperature

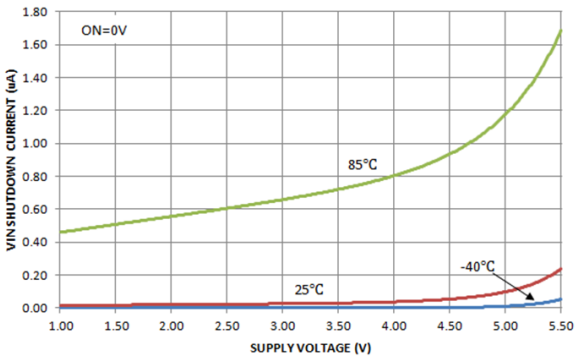


Figure 7. Shutdown Current vs. Supply Voltage

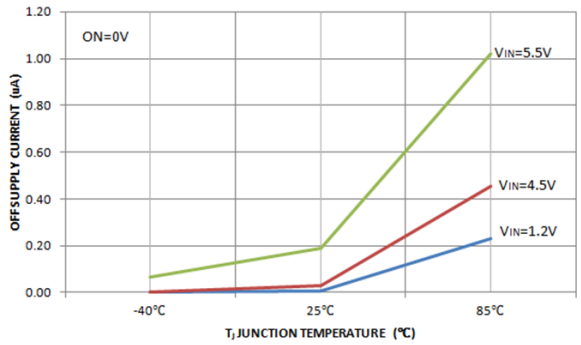


Figure 8. Off Supply Current vs. Temperature (V_{OUT}=0 V)

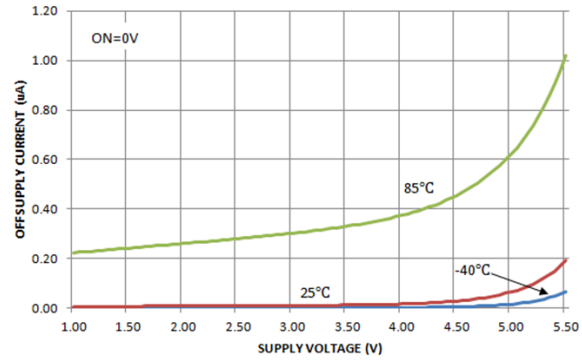


Figure 9. Off Supply Current vs. Supply Voltage (V_{OUT}=0 V)

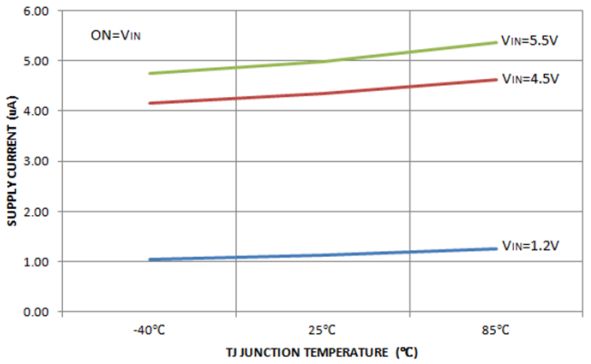


Figure 10. Quiescent Current vs. Temperature

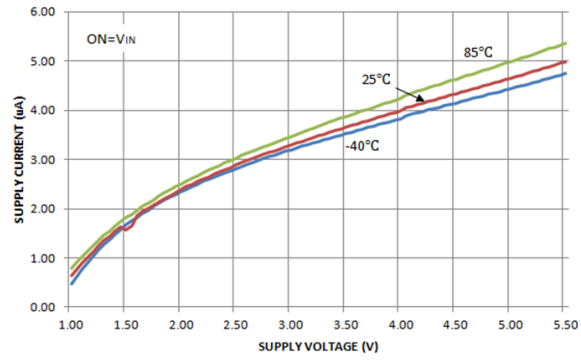


Figure 11. Quiescent Current vs. Supply Voltage

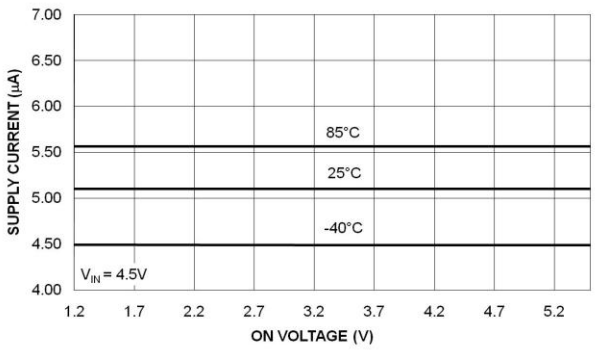


Figure 12. Quiescent Current vs. On Voltage (V_{BAT}=4.5 V)

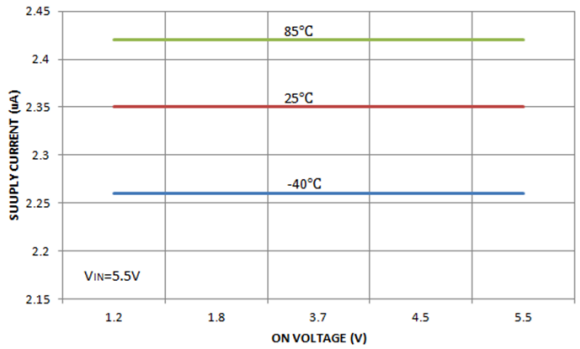


Figure 13. Quiescent Current vs. On Voltage (V_{BAT}=5.5 V)

Typical Characteristics

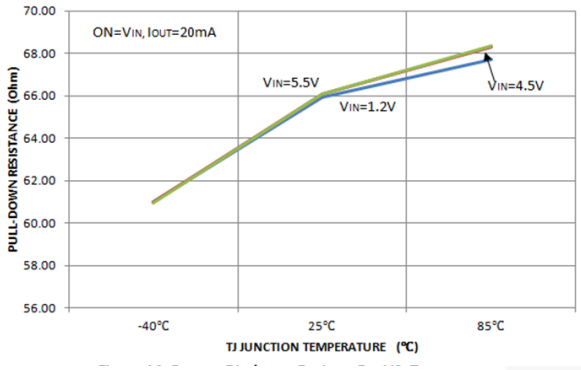


Figure 14. Output Discharge Resistor R_{PD} vs. Temperature

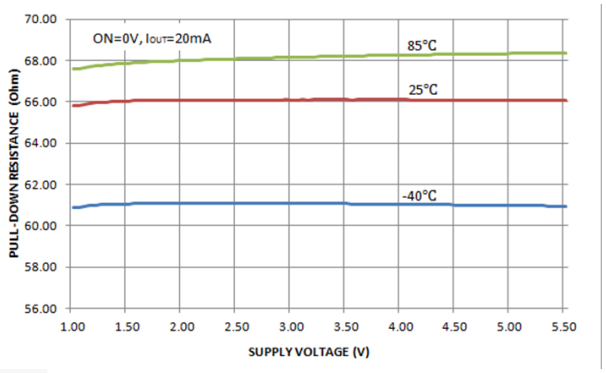


Figure 15. Output Discharge Resistor R_{PD} vs. Supply Voltage

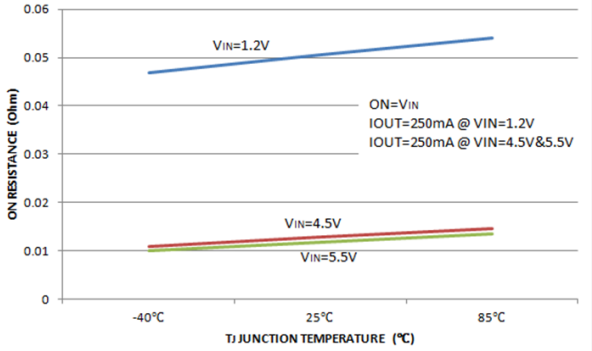


Figure 16. R_{ON} vs. Temperature

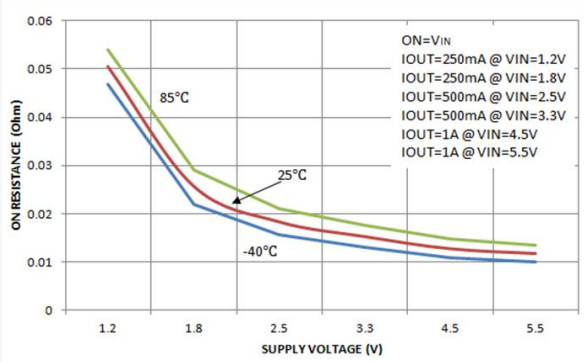


Figure 17. R_{ON} vs. Supply Voltage

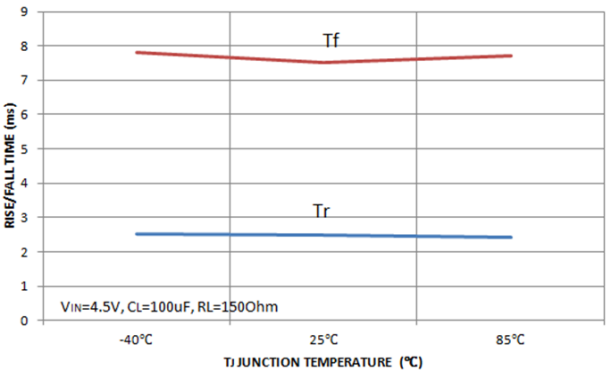


Figure 18. t_R/t_F vs. Temperature

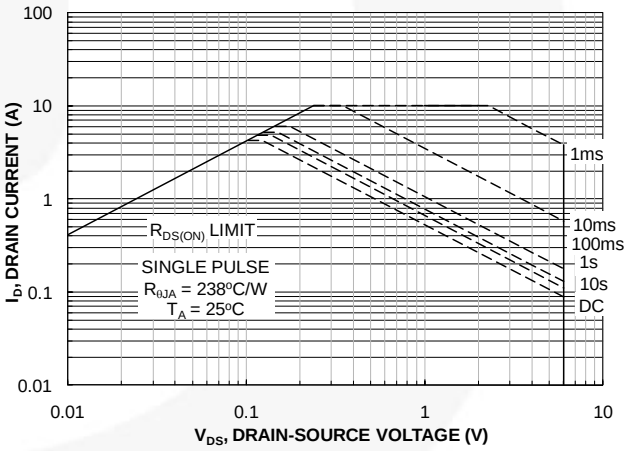


Figure 19. I_{SW} vs. (V_{IBAT}-V_{OUT}) — SOA

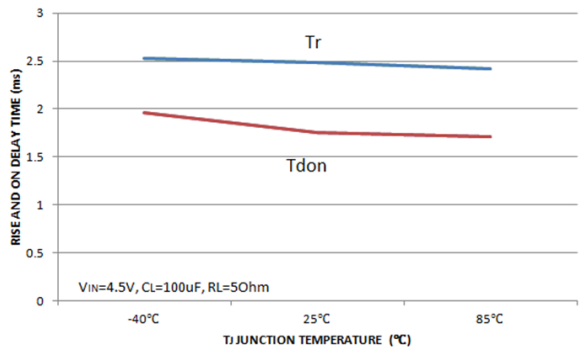


Figure 20. t_R/t_{DON} vs. Temperature

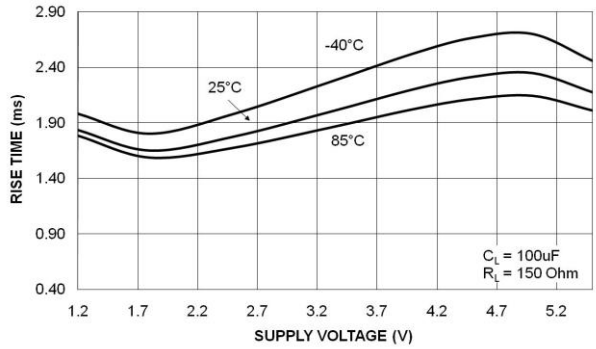


Figure 21. t_R vs. Supply Voltage

Typical Characteristics

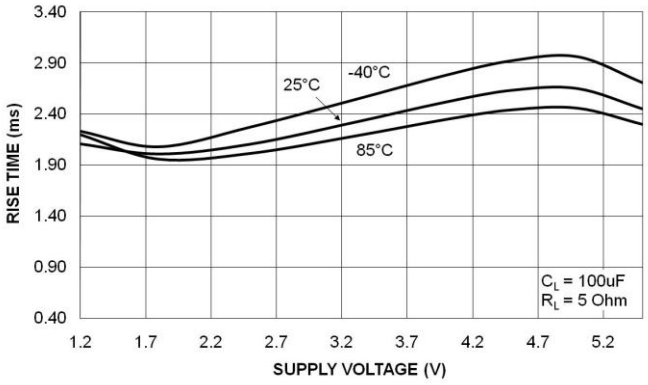


Figure 22. t_R vs. Supply Voltage

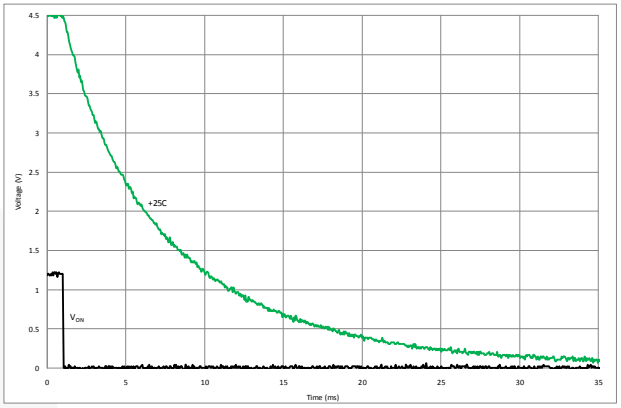


Figure 23. Turn-Off Response (V_{BAT}=4.5 V, C_{IN}=10 µF, C_L=100 µF, without External R_L)

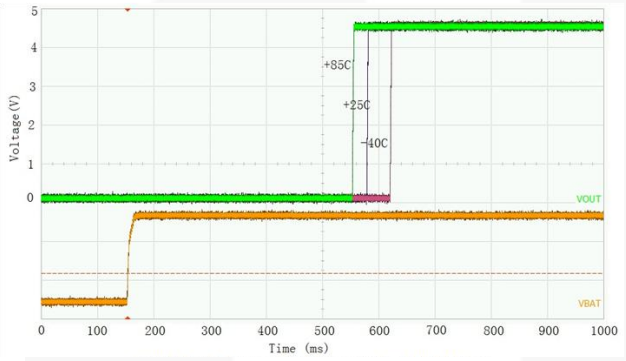


Figure 24. Turn-On Response (V_{BAT}=4.5 V, C_{IN}=10 µF, C_L=1 µF, R_L=50 Ω)

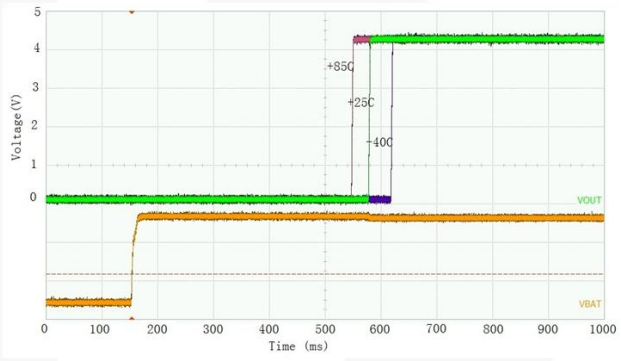


Figure 25. Turn-On Response (V_{BAT}=4.5 V, C_{IN}=10 µF, C_L=100 µF, R_L=5 Ω)

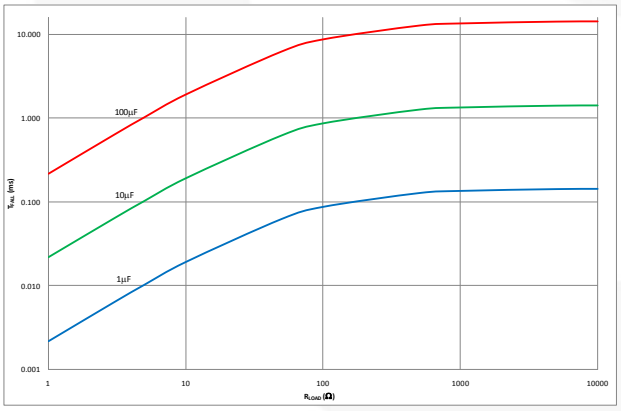


Figure 26. Fall Time as a Function of External Resistive Load (C_L=1 µF, 10 µF, and 100 µF)

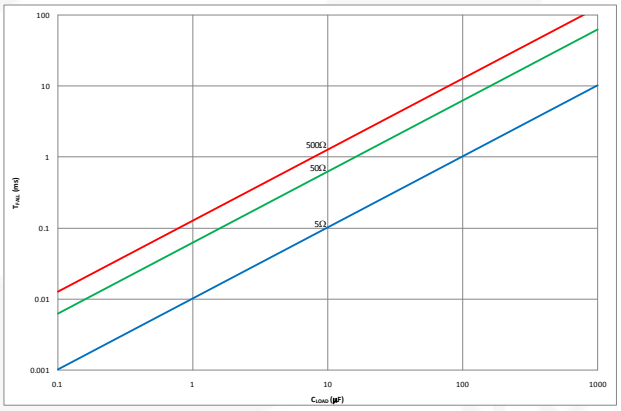


Figure 27. Fall Time as a Function of External Capacitive Load (R_L=5 Ω, 50 Ω, and 500 Ω)

Application Information

Reset Timer and Advanced Load Management

The FTL75939 is both a reset IC and an advanced load management device. A typical application is shown in Figure 1.

Disconnect PMIC from Battery (Turn Off)

After holding the DSR pin HIGH, changing the OFF pin from LOW to HIGH (rising edge triggered) and holding it HIGH for at least 1 ms; the FTL75939 triggers an internal counter to allow a factory-customized 7.3 s delay before turning off internal load switch. The delay is intended to allow the PMIC to complete a power-down sequence before safely disconnecting from the power supply. However, the turn-off sequence is terminated if a higher priority input is detected in t_{SD} period *(see Resolving Input Conflicts)*.

Alternatively, after holding the DSR pin LOW, changing the OFF pin from LOW to HIGH (rising edge triggered) and holding it HIGH for at least 1 ms; the FTL75939 triggers the zero-second turn-off. Delay t_{SD} is significantly reduced to 0.6 ms to avoid the default delay to turn-off load switch (t_{SD}).

With its stringent shutdown current flow, the FTL75939 significantly reduces the current drain on a battery when the PMIC is turned off. This preserves the battery power for a longer period when a mobile device is in Shutdown Mode.

Power On

There are two methods to turn on the load switch to wake up the PMIC. When a HIGH is inserted to the SYS_WAKE pin or when /SR0 is held LOW for > 2.3 s *(see Figure 30)*; the FTL75939 turns on its load switch to allow PMIC to connect to the battery. The reset feature is disabled when V_{OUT} is toggled from OFF to ON. Continuously holding /SR0 LOW does not trigger a reset event.

To enable the reset feature, /SR0 must return to HIGH such that FTL75939 resets its internal counter.

Reset Timer

During normal operation of a mobile device, if a reset operation is needed for mobile equipmen;, holding the power switch, to which /SR0 is connected and is forced LOW, for at least 7.5 s, causes the FTL75939 to cut off the supply power to PMIC for 400 ms by turning off the load switch. The FTL75939 then automatically turns on the load switch to reconnect the PMIC to battery. This forces PMIC to enter a power-on sequence.

If the power switch is released and /SR0 is returned to HIGH within 7.5 s, the FTL75939 resets its counter and V_{OUT} remains in ON state; there is no change on V_{OUT} and a reset does not occur.

Power-On Reset

When FTL75939 is connected to a battery ($V_{BAT} \geq 1.2$ V), the part enters Power-On Reset (POR) Mode. All internal registers are reset and V_{OUT} is ON at the end of POR sequence *(see 0)*.

Zero-Second Factory Test Mode

FTL75939 includes a Zero-Second Factory Test Mode to shorten the turn-on time for V_{OUT} (t_{VON}) and timer delay before reset (t_{PHL1}) for factory testing.

When V_{OUT} is OFF, the default turn-on time (t_{VON}) is 2.3 s. If the DSR pin is LOW prior to /SR0 going LOW, the FTL75939 bypasses the 2.3 s delay and V_{OUT} changes from OFF to ON immediately.

Similiarly, default reset delay (t_{PHL1}) is 7.5 s. If V_{OUT} is ON and the DSR pin is LOW prior to /SR0 going LOW, the FTL75939 enters Zero-Second Factory Test Mode and bypasses the default reset delay of 7.5 s; V_{OUT} is pulled from ON to OFF immediately. The reset pulse (t_{REC1}) remains at 400 ms in Zero-Second Factory Test Mode.

DSR should never be left floating during normal operation.

Table 1. V_{OUT} and Input Conditions

Function	Initial Conditions (t=0 Second)				Associated Delay	V_{OUT}	
	/SR0	SYS_WAKE	OFF	DSR		Before	After
Power-On	LOW	X(12)	X	LOW	t_{VON} < 4 ms	OFF	ON
	LOW	X	X	HIGH	t_{VON}=2.3 s	OFF	ON
	HIGH	HIGH	X	X	t_{ON}=4.4 ms	OFF	ON
Reset Function	LOW	X	X	LOW	t_{PHL1} < 1 ms t_{REC1}=400 ms	ON	⊓ (12)
	LOW	X	X	HIGH	t_{PHL1}=7.5 s(13) t_{REC1}=400 ms	ON	⊓
Turn Off	HIGH	LOW	⌐ (12)	LOW	t_{SD} < 1 ms	ON	OFF
	HIGH	LOW	⌐	HIGH	t_{SD}=7.3 s	ON	OFF

Notes:

12. X=Don't Care, ⌐ = Rising Edge, ⊓ =HIGH to LOW to HIGH.
13. Reset delay (t_{PHL1}) is adjustable *(seeTable 4)*.

Table 2. Pin Condition after POR

Pin Name	/SR0	DSR	SYS_WAKE	OFF	VOUT
Default State (after POR)	1	1	0	0	ON

Note:
14. 1=Input Logic HIGH, 0=Input Logic LOW, ON=load switch is ON state.

Timing Diagrams

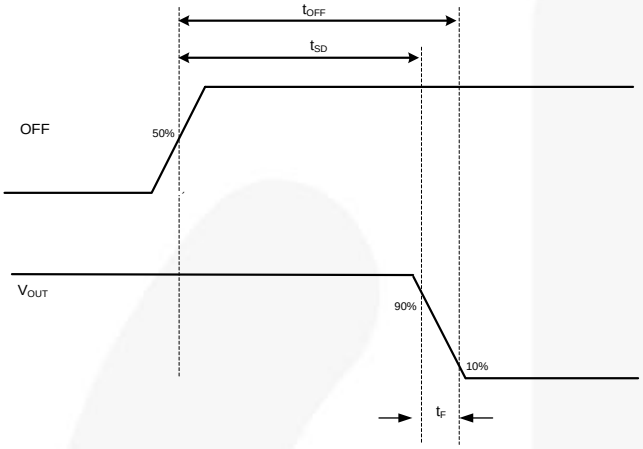


Figure 28. Timing Diagram (OFF vs. V_{OUT})

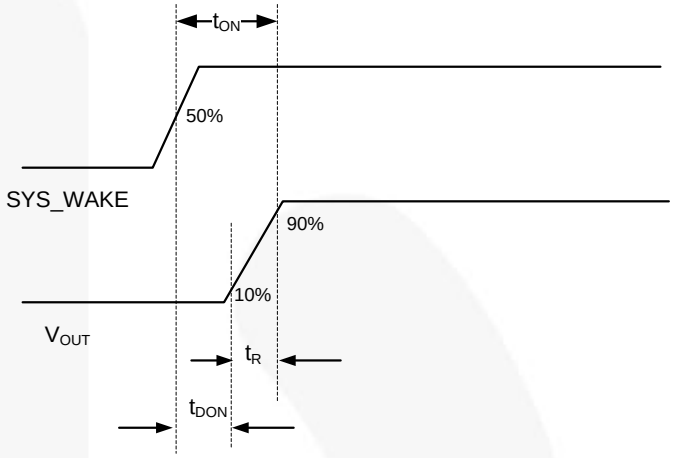


Figure 29. Timing Diagram (SYS_WAKE vs. V_{OUT})

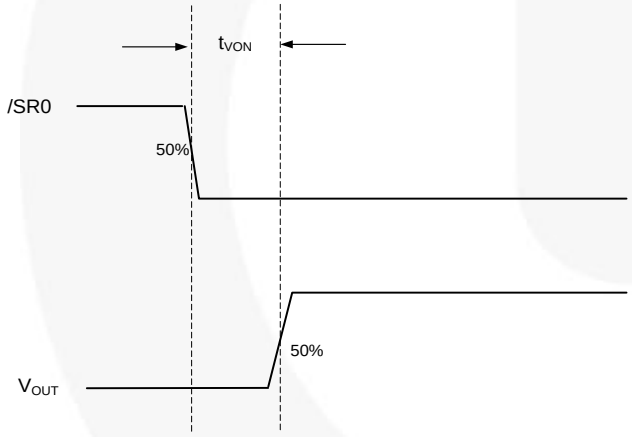


Figure 30. Power On with /SR0

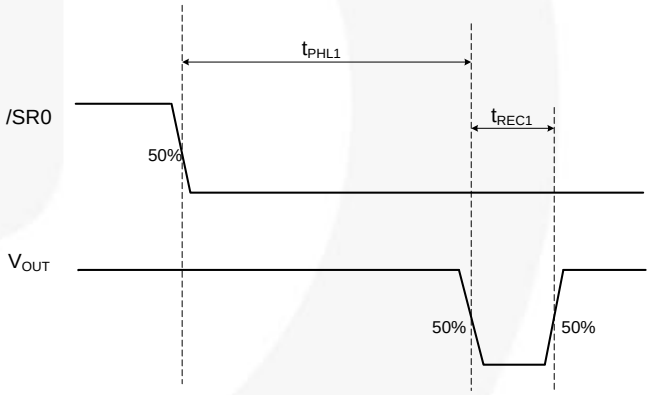


Figure 31. Reset Timing

Resolving Input Conflicts

The FTL75939 allows multiple simultaneous inputs and can resolve conflicts based on priority level *(see Table 3)*. When two input pins are triggered at the same time, only the higher priority input is served and the lower priority input is ignored. The lower-priority signal must be repeated to be serviced.

Table 3. Input Priority

Input	Priority (1=Highest)
/SR0	1
SYS_WAKE	2
OFF	3

Special Note on OFF Pin

In the t_{SD} period (DSR=HIGH only, *see Figure 28*); if /SR0 or SYS_WAKE is triggered when $0 < t < t_{SD}$, the FTL75939 exits the turn-off sequence and V_{OUT} remains in ON state. The higher priority input is served regardless of the condition of OFF pin.

To re-initiate the turn-off sequence, the OFF pins must return to LOW, then toggle from LOW to HIGH again. The same input priority applies (*Table 3*) if DSR = HIGH.

Special Note on SYS_WAKE Pin

The SYS_WAKE pin is designed and characterized to handle high voltage input: at least 20 V. Therefore, in application, a current-limiting resistor (i.e 100 kΩ) is required between SYS_WAKE and the input signal regardless of input voltage.

Adjustable Reset Delay with an External Resistor and DSR

The reset delay is adjustable by connecting a commonly available, low-power, ±5%, RoHS-compliant resistor between the DELAY_ADJ pin and the GND pin *(see Table 4)*. To disable the adjustable delay feature, DELAY_ADJ should be tied to V_{BAT} directly.

The reset delay is factory programmed at 7.5 s.

The additional power consumption caused by using an external resistor is negligible. The external resistor is normally disconnected and is enabled for milliseconds when /SR0 is pulled LOW.

This external adjustment feature provides a simple alternate method for controlling delay time for engineering and production at customer's location.

Fairchild can also factory program a wide range of turn-on times for V_{OUT} (t_{VON}), timer delay before reset (t_{PHL1}), reset timeout delay for V_{OUT} (t_{REC1}), and load switch turn-off time (t_{OFF}) to match customer applications. In this case, the external resistor (R_{ADJ}) can be eliminated.

For more details, contact an authorized sales representative: *http://www.fairchildsemi.com/cf/#Regional-Sales*.

Table 4. Delay Adjustment vs. External Resistor

External Resistor R_{ADJ} (kΩ)	Delay Multiplier	Adjusted Reset Delay t_{PHL1_ADJ}, (Seconds) ±20%
Tie to GND (No Resistor)	0.50 x t_{PHL1}	3.8
3.9	0.75 x t_{PHL1}	5.6
10	1.25 x t_{PHL1}	9.4
22	1.50 x t_{PHL1}	11.3
47	1.75 x t_{PHL1}	13.1
120	2.00 x t_{PHL1}	15.0
Tie to V_{BAT} (No Resistor)	1.00 x t_{PHL1}	7.5

IntelliMAX™ Switch Inside the FTL75939

Input Capacitor

The IntelliMAX™ switch inside the reset timer doesn't require an input capacitor. To reduce device inrush current, a 0.1 µF ceramic capacitor, C_{IN}, is recommended close to the V_{BAT} pin. A higher value of C_{IN} can be used to reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

Output Capacitor

While the load switch works without an output capacitor; if parasitic board inductance forces V_{OUT} below GND when switching off, a 0.1 µF capacitor, C_{OUT}, should be placed between V_{OUT} and GND.

Fall Time

Device output fall time can be calculated based on the RC constant of the external components, as follows:

$$t_F = R_L \times C_L \times 2.2 \quad (1)$$

where t_F is 90% to 10% fall time; R_L is output load; and C_L is output capacitor.

The same equation works for a device with a pull-down output resistor. R_L is replaced by a parallel connected pull-down and an external output resistor combination, calculated as:

$$t_F = \frac{R_L \times R_{PD}}{R_L + R_{PD}} \times C_L \times 2.2 \quad (2)$$

where t_F is 90% to 10% fall time; R_L is output load; R_{PD}=65 Ω is output pull-down resistor; and C_L is the output capacitor.

Resistive Output Load

If resistive output load is missing, the IntelliMAX switch without a pull-down output resistor does not discharge the output voltage. Output voltage drop depends, in that case, mainly on external device leaks.

Application Specifics

At maximum operational voltage (V_{BAT}=5.5 V), device inrush current might be higher than expected. Spike current should be taken into account if V_{BAT}>5 V and the output capacitor is much larger than the input capacitor. Input current I_{BAT} can be calculated as:

$$I_{BAT}(t) \approx \frac{V_{OUT}(t)}{R_{LOAD}} + (C_{LOAD} - C_{IN})\frac{dV_{OUT}(t)}{dt} \quad (3)$$

where switch and wire resistances are neglected and capacitors are assumed ideal.

Estimating $V_{OUT}(t)=V_{BAT}/10$ and using experimental formula for slew rate ($dV_{OUT}(t)/dt$), spike current can be written as:

$$\max(I_{BAT}) = \frac{V_{BAT}}{10R_{LOAD}} + (C_{LOAD} - C_{IN})(0.05V_{BAT} - 0.255) \quad (4)$$

where supply voltage V_{BAT} is in volts; capacitances are in micro farads; and resistance is in ohms.

Example: If V_{BAT}=5.5 V, C_{LOAD}=100 µF, C_{IN}=10 µF, and R_{LOAD}=50 Ω; calculate the spike current by:

$$\max(I_{BAT}) = \frac{5.5}{10 \times 50} + (100 - 10)(0.05 \times 5.5 - 0.255)A = 1.8A$$

Maximum spike current is 1.8 A, while average ramp-up current is:

$$I_{BAT}(t) \approx \frac{V_{OUT}(t)}{R_{LOAD}} + (C_{LOAD} - C_{IN})\frac{dV_{BAT}(t)}{dt}$$
$$\approx 2.75/50 + 100 \times 0.0022 = 0.275A$$

Output Discharge

The device contains a R_{PD}=65 Ω on-chip pull-down resistor for quick output discharge. The resistor is activated when the switch is turned off.

Recommended Layout

For best thermal performance and minimal inductance and parasitic effects, keeping the input and output traces short and capacitors as close to the device as possible is recommended. Additional recommended layout considerations include:

- A1, A2, and A3 are interconnected at PCB, as close to the landing pad as possible.
- B1, B2, and B3 are interconnected at PCB, as close to the landing pad as possible.
- C1 (GND) is connected to GND plane of PCB.
- Reserve a pad for capacitor connection (C1) between V_{BAT} and GND, if no input capacitor is planned.
- Reserve a pad for capacitor connection (C2) between V_{OUT} and GND, if no output capacitor is planned.
- Use a dedicated V_{OUT} or V_{BAT} plane to improve thermal dissipation.

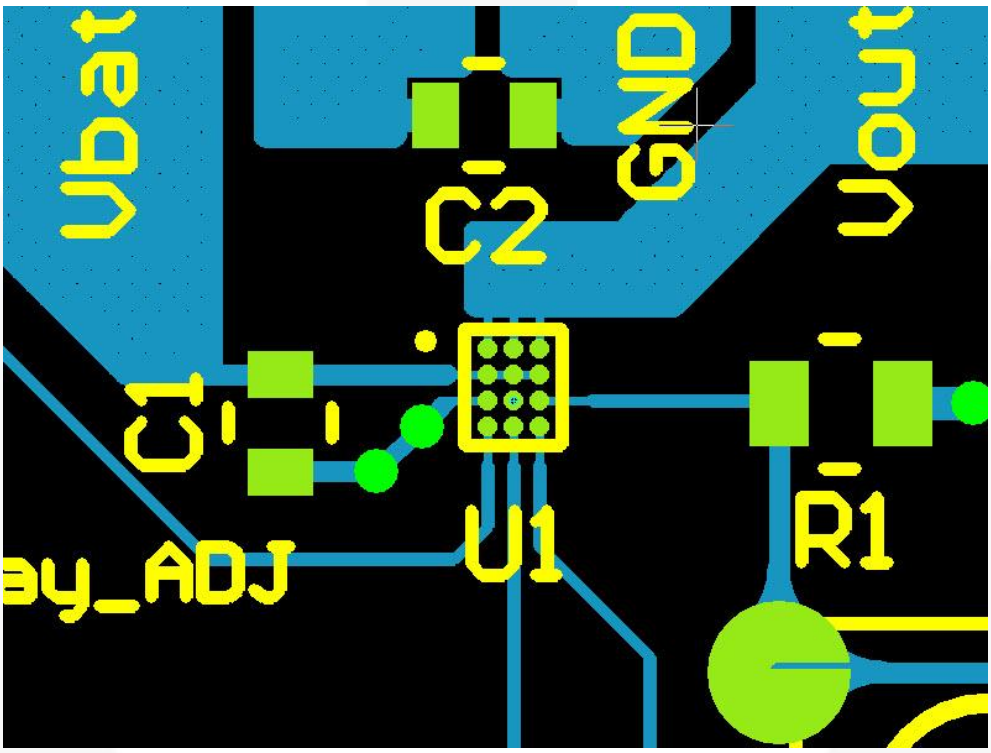
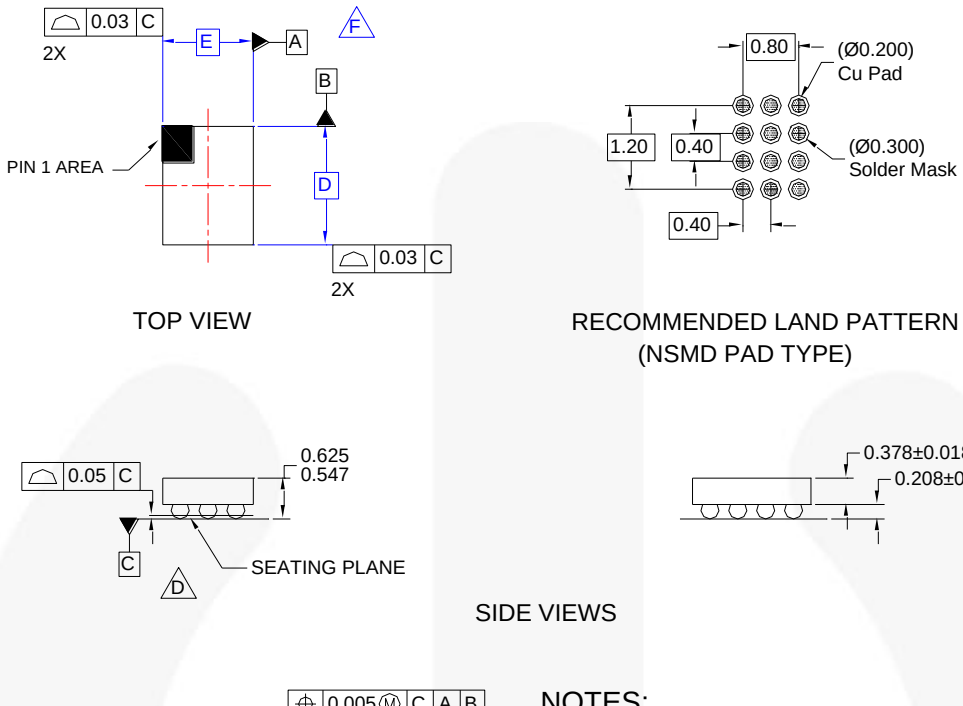


Figure 32. Sample Layout

Physical Dimensions



NOTES:

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B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: MKT-UC012ACrev1.

Figure 33. 12-Ball, Wafer-Level Chip-Scale Packaging (WLCSP) 3x4 Array, 0.4 mm Pitch, 250 µm Ball

D	E	X	Y
1.615 ±0.030	1.310 ±0.030	0.255	0.208

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