SMPS Series N-Channel IGBT

600 V

HGTG40N60A4

ON Semiconductor®

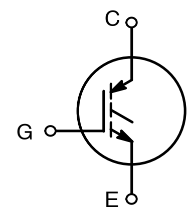
www.onsemi.com

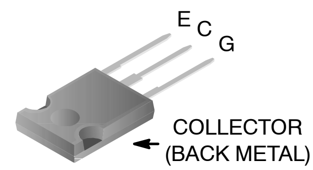
The HGTG40N60A4 is a MOS gated high voltage switching device combining the best features of a MOSFET and a bipolar transistor. This device has the high input impedance of a MOSFET and the low on−state conduction loss of a bipolar transistor. The much lower on−state voltage drop varies only moderately between 25°C and 150°C. This IGBT is ideal for many high voltage switching applications operating at high frequencies where low conduction losses are essential. This device has been optimized for high frequency switch mode power supplies

Formerly Developmental Type TA49347.

Features

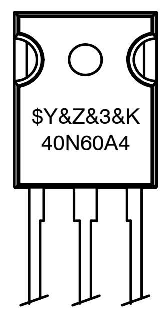
- 100 kHz Operation at 390 V, 40 A
- 200 kHz Operation at 390 V, 20 A
- 600 V Switching SOA Capability
- Typical Fall Time 55 ns at T_J = 125°C
- Low Conduction Loss
- This is a Pb−Free Device





TO−247−3LD SHORT LEAD
CASE 340CK
JEDEC STYLE

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
40N60A4	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

April, 2020 − Rev. 2

Publication Order Number:
HGTG40N60A4/D

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

Parameter	Symbol	HGTG40N60A4	Unit
Collector to Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous At T_C = 25°C At T_C = 110°C	 I_{C25} I_{C110}	 75 63	 A A
Collector Current Pulsed (Note 1)	I_{CM}	300	A
Gate to Emitter Voltage Continuous	V_{GES}	±20	V
Gate to Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at T_J = 150°C, Figure 2	SSOA	200 A at 600 V	
Power Dissipation Total at T_C = 25°C	P_D	625	W
Power Dissipation Derating T_C > 25°C		5	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	−55 to 150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Collector to Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA, V_{GE} = 0 V		600	–	–	V
Emitter to Collector Breakdown Voltage	BV_{ECS}	I_C = −10 mA, V_{GE} = 0 V		20	–	–	V
Collector to Emitter Leakage Current	I_{CES}	V_{CE} = BV_{CES}	T_J = 25°C	–	–	250	μA
			T_J = 125°C	–	–	3.0	mA
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 40 A, V_{GE} = 15 V	T_J = 25°C	–	1.7	2.7	V
			T_J = 125°C	–	1.5	2.0	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 250 μA, V_{CE} = V_{GE}		4.5	5.6	7	V
Gate to Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V		–	–	±250	nA
Switching SOA	SSOA	T_J = 150°C, R_G = 2.2 Ω, V_{GE} = 15 V, L = 100 μH, V_{CE} = 600 V		200	–	–	A
Gate to Emitter Plateau Voltage	V_{GEP}	I_C = 40 A, V_{CE} = 0.5 BV_{CES}		–	8.5	–	V
On−State Gate Charge	$Q_{g(ON)}$	I_C = 40 A, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15 V	–	350	405	nC
			V_{GE} = 20 V	–	450	520	nC
Current Turn−On Delay Time	$t_{d(ON)I}$	IGBT and Diode at T_J = 25°C, I_{CE} = 40 A, V_{CE} = 0.65 BV_{CES}, V_{GE} = 15 V, R_G = 2.2 Ω, L = 200 μH, Test Circuit (Figure 20)		–	25	–	ns
Current Rise Time	t_{rI}			–	18	–	ns
Current Turn−Off Delay Time	$t_{d(OFF)I}$			–	145	–	ns
Current Fall Time	t_{fI}			–	35	–	ns
Turn−On Energy (Note 3)	E_{ON1}			–	400	–	μJ
Turn−On Energy (Note 3)	E_{ON2}			–	850	–	μJ
Turn−Off Energy (Note 2)	E_{OFF}			–	370	–	μJ

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current Turn−On Delay Time	$t_{d(ON)I}$	IGBT and Diode at T_J = 125°C, I_{CE} = 40 A, V_{CE} = 0.65 BV_{CES}, V_{GE} = 15 V, R_G = 2.2 Ω, L = 200 μH, Test Circuit (Figure 20)	−	27	−	ns
Current Rise Time	t_{rI}		−	20	−	ns
Current Turn−Off Delay Time	$t_{d(OFF)I}$		−	185	225	ns
Current Fall Time	t_{fI}		−	55	95	ns
Turn−On Energy (Note 3)	E_{ON1}		−	400	−	μJ
Turn−On Energy (Note 3)	E_{ON2}		−	1220	1400	μJ
Turn−Off Energy (Note 2)	E_{OFF}		−	700	800	μJ
Thermal Resistance Junction To Case	$R_{\theta JC}$		−	−	0.2	°C/W

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Turn−Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0 A). All devices were tested per JEDEC Standard No. 24−1 Method for Measurement of Power Device Turn−Off Switching Loss. This test method produces the true total Turn−Off Energy Loss.
3. Values for two Turn−On loss conditions are shown for the convenience of the circuit designer. E_{ON1} is the turn−on loss of the IGBT only. E_{ON2} is the turn−on loss when a typical diode is used in the test circuit and the diode is at the same T_J as the IGBT. The diode type is specified in Figure 20.

TYPICAL PERFORMANCE CURVES (unless otherwise specified)

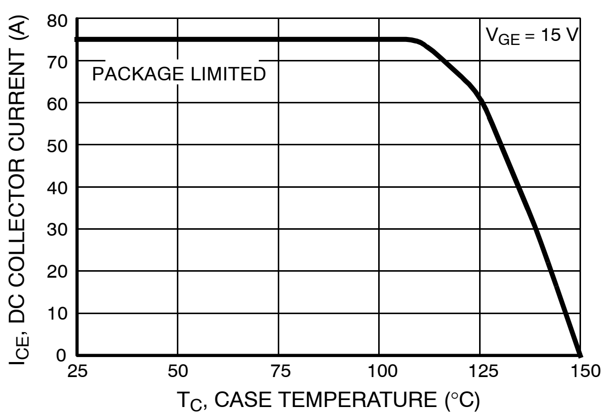


Figure 1. DC COLLECTOR CURRENT vs. CASE TEMPERATURE

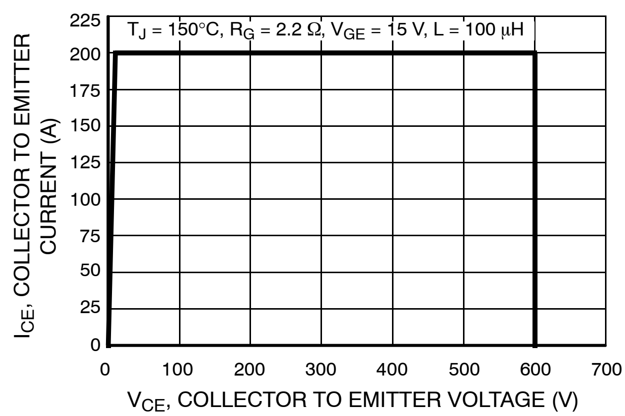


Figure 2. MINIMUM SWITCHING SAFE OPERATING AREA

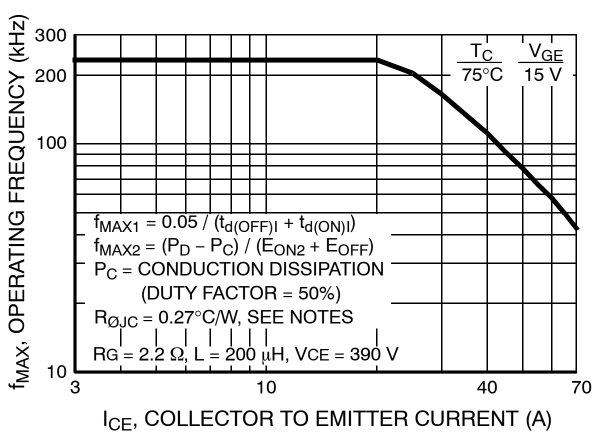


Figure 3. OPERATING FREQUENCY vs. COLLECTOR TO EMITTER CURRENT

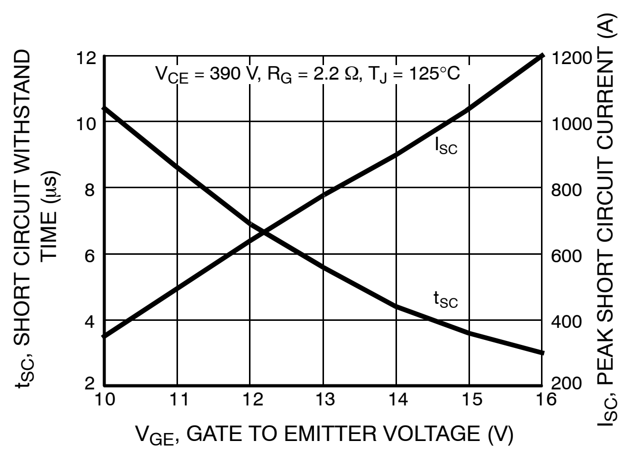


Figure 4. SHORT CIRCUIT WITHSTAND TIME

TYPICAL PERFORMANCE CURVES (unless otherwise specified) (continued)

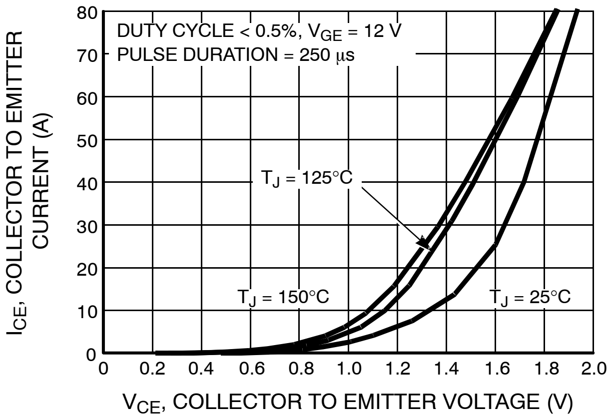


Figure 5. COLLECTOR TO EMITTER ON−STATE VOLTAGE

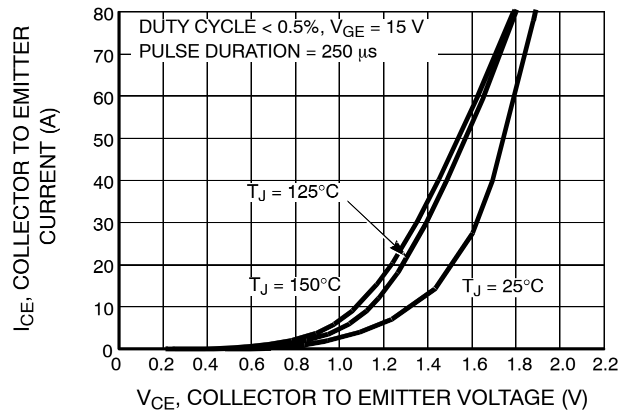


Figure 6. COLLECTOR TO EMITTER ON−STATE VOLTAGE

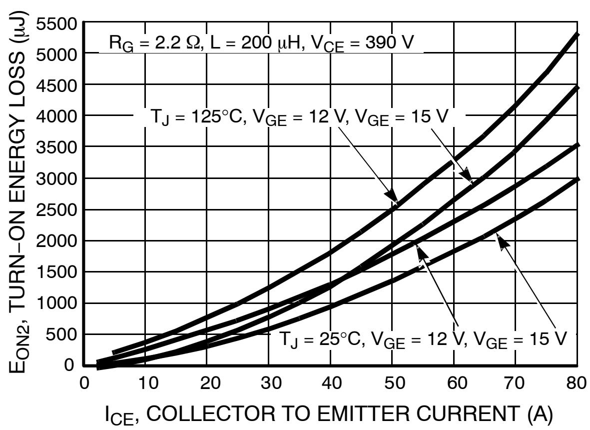


Figure 7. TURN−ON ENERGY LOSS vs. COLLECTOR TO EMITTER CURRENT

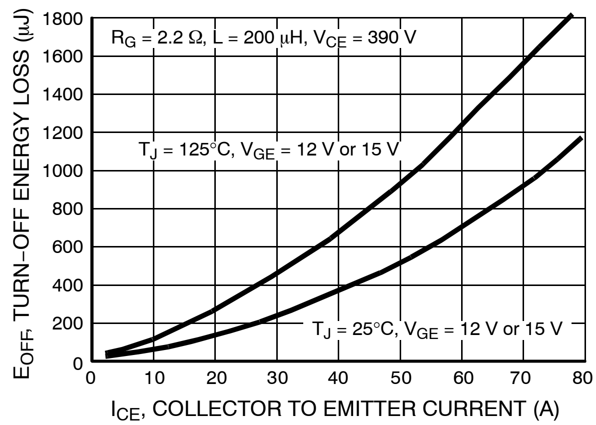


Figure 8. TURN−OFF ENERGY LOSS vs. COLLECTOR TO EMITTER CURRENT

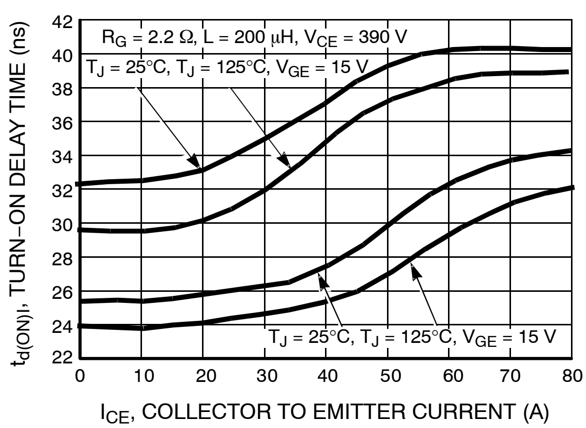


Figure 9. TURN−ON DELAY TIME vs. COLLECTOR TO EMITTER CURRENT

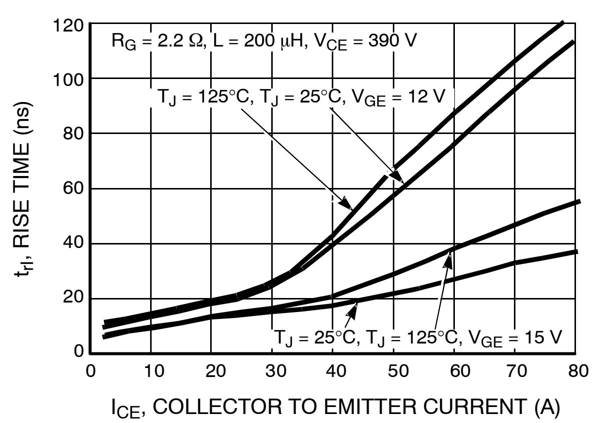


Figure 10. TURN−ON RISE TIME vs. COLLECTOR TO EMITTER CURRENT

TYPICAL PERFORMANCE CURVES (unless otherwise specified) (continued)

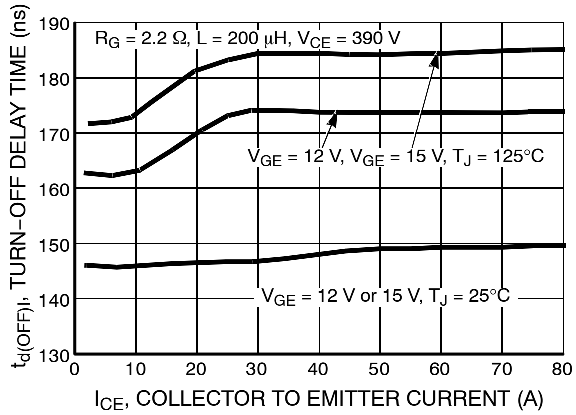


Figure 11. TURN−OFF DELAY TIME vs. COLLECTOR TO EMITTER CURRENT

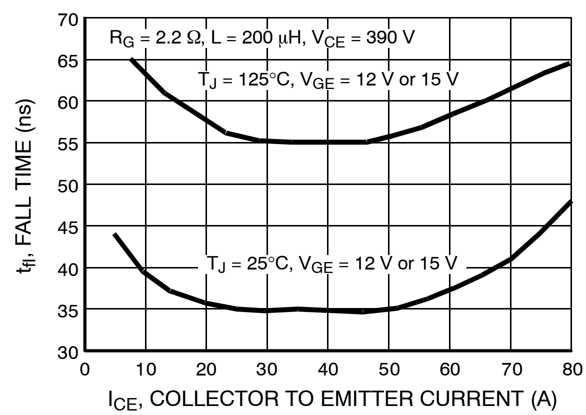


Figure 12. FALL TIME vs. COLLECTOR TO EMITTER CURRENT

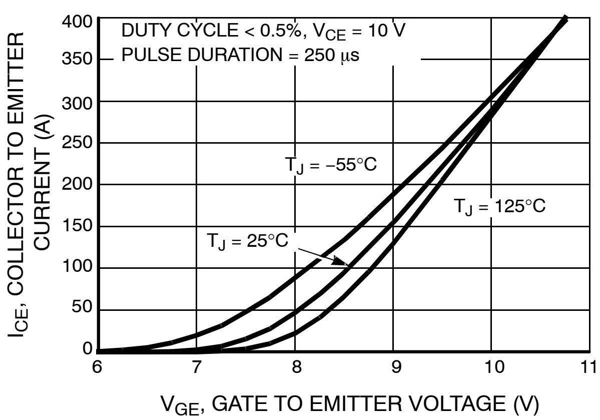


Figure 13. TRANSFER CHARACTERISTIC

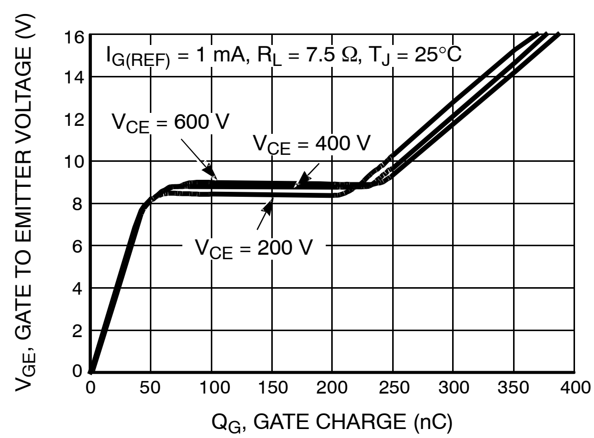


Figure 14. GATE CHARGE WAVEFORMS

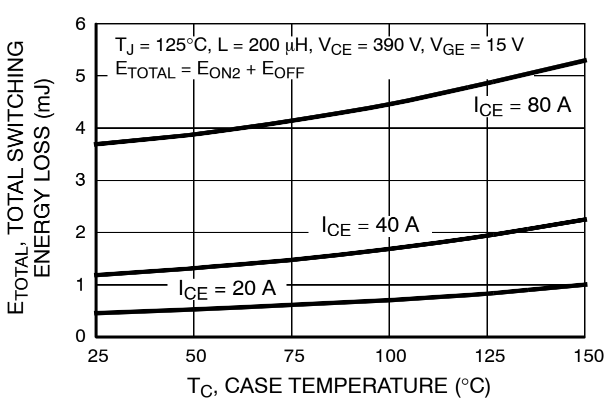


Figure 15. TOTAL SWITCHING LOSS vs. CASE TEMPERATURE

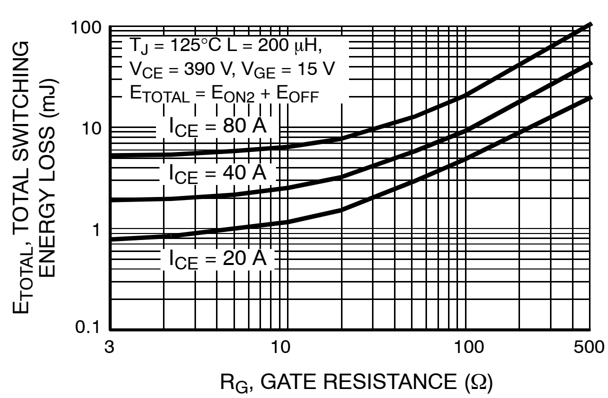


Figure 16. TOTAL SWITCHING LOSS vs. GATE RESISTANCE

TYPICAL PERFORMANCE CURVES (unless otherwise specified) (continued)

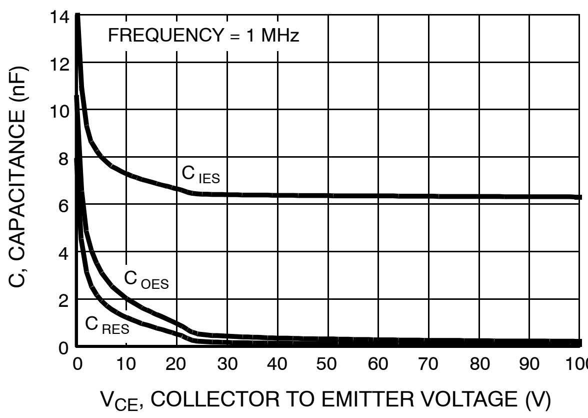


Figure 17. CAPACITANCE vs. COLLECTOR TO EMITTER VOLTAGE

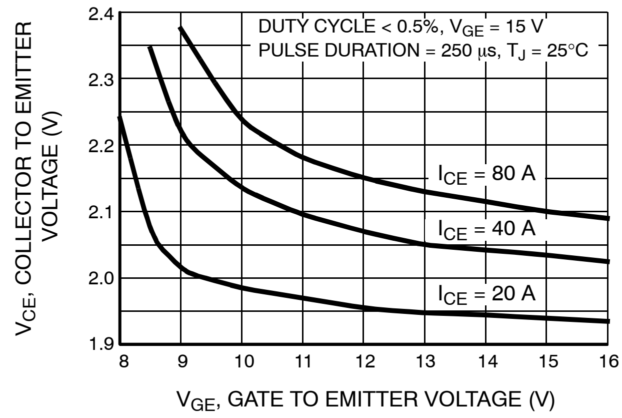


Figure 18. COLLECTOR TO EMITTER ON−STATE VOLTAGE vs. GATE TO EMITTER VOLTAGE

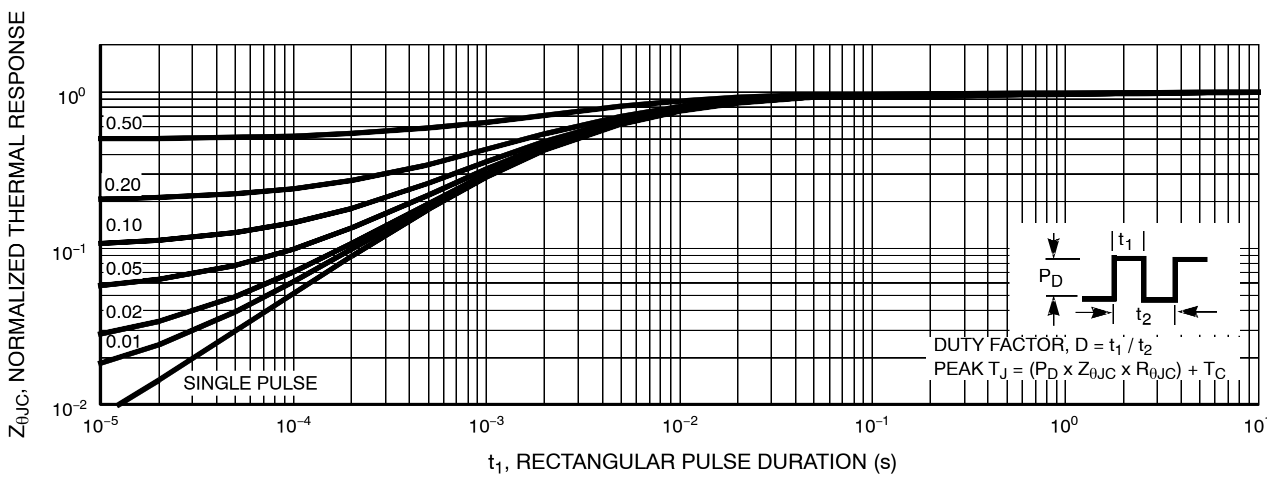


Figure 19. NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

TEST CIRCUIT AND WAVEFORMS

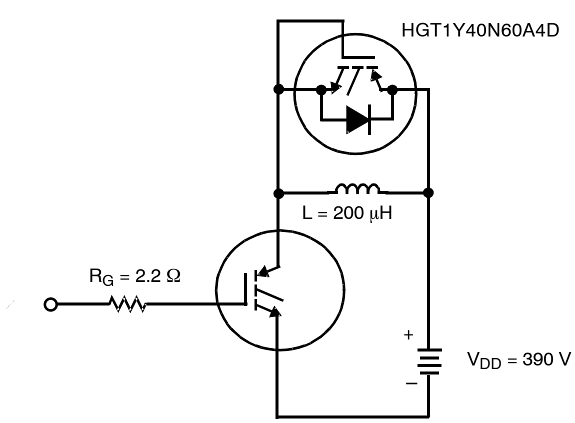


Figure 20. INDUCTIVE SWITCHING TEST CIRCUIT

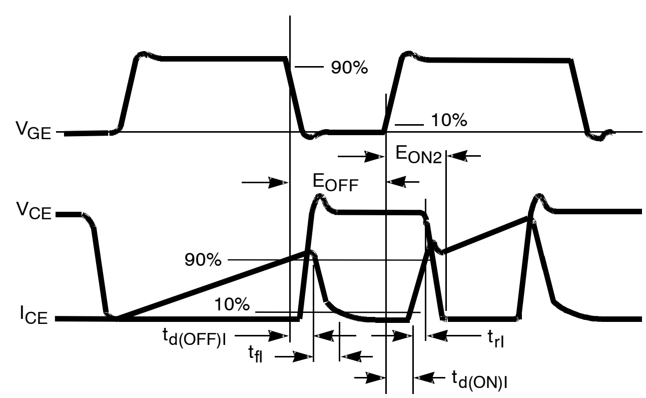


Figure 21. SWITCHING TEST WAVEFORMS

HANDLING PRECAUTIONS FOR IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate−insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means − for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. *Gate Voltage Rating* − Never exceed the gate−voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. *Gate Termination* − The gates of these devices are essentially capacitors. Circuits that leave the gate open− circuited or floating should be avoided. These conditions can result in turn−on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. *Gate Protection* - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

OPERATING FREQUENCY INFORMATION

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows f_{MAX1} or f_{MAX2}; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05 / (t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on−state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 21. Device turn−off delay can establish an additional frequency limiting condition for an application other than T_{JM}. $t_{d(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C) / (E_{OFF} + E_{ON2})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JM} - T_C) / R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 21) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE}) / 2$.

E_{ON2} and E_{OFF} are defined in the switching waveforms shown in Figure 25. E_{ON2} is the integral of the instantaneous power loss (I_{CE} x V_{CE}) during turn−on and E_{OFF} is the integral of the instantaneous power loss (I_{CE} x V_{CE}) during turn−off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$).

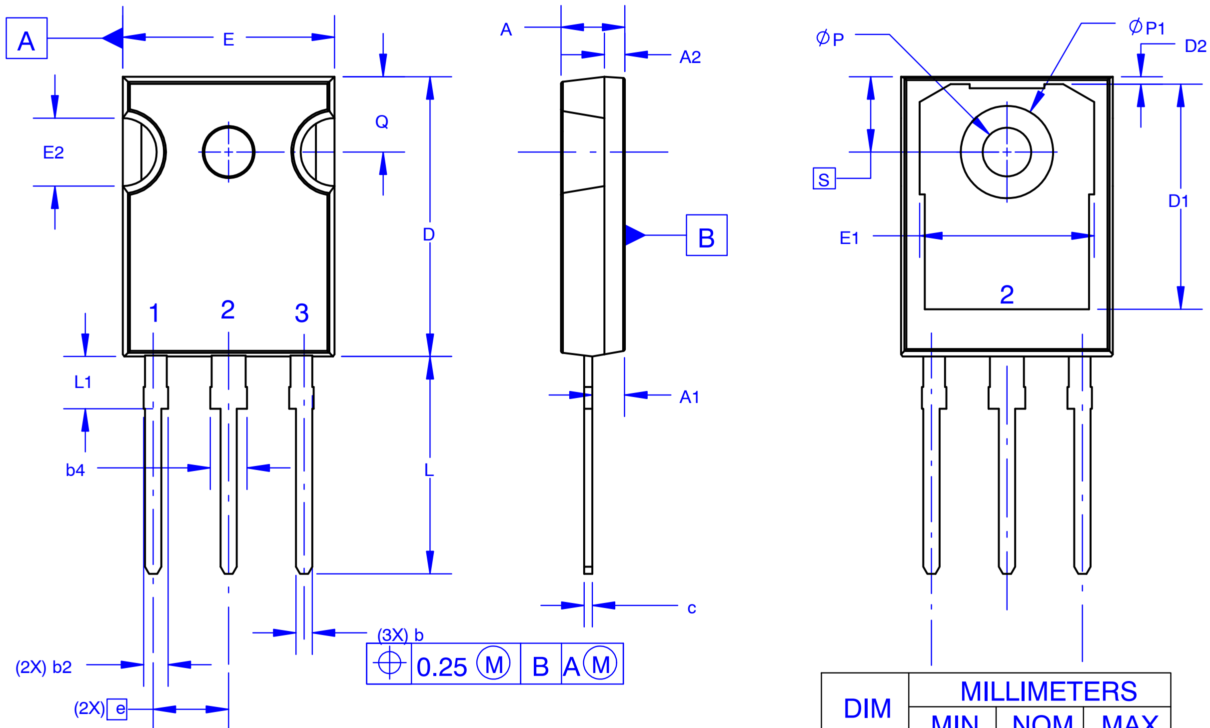
ORDERING INFORMATION

Part Number	Package	Brand	Shipping
HGTG40N60A4	TO−247	40N60A4	450 Units / Tube

NOTE: When ordering, use the entire part number.

TO−247−3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

GENERIC
MARKING DIAGRAM*

AYWWZZ
XXXXXXX
XXXXXXX
∘

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON13851G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TO−247−3LD SHORT LEAD	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊