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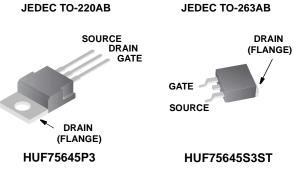
HUF75645P3, HUF75645S3S

Data Sheet

October 2013

N-Channel UltraFET Power MOSFET 100 V, 75 A, 14 mΩ

Packaging



Symbol



Features

- Ultra Low On-Resistance
- $r_{DS(ON)} = 0.014\Omega, V_{GS} = 10V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER™ Electrical Models
 - Spice and Saber Thermal Impedance Models
 - www.onsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75645P3	TO-220AB	75645P
HUF75645S3ST	TO-263AB	75645S

Absolute Maximum Ratings $T_C = 25^{\circ}C$, Unless Otherwise Specified

	HUF75645P3, HUF75645S3ST	UNITS
Drain to Source Voltage (Note 1) V _{DSS}	100	V
Drain to Gate Voltage (R _{GS} = 20kΩ) (Note 1)	100	V
Gate to Source Voltage	±20	V
Drain Current		
Continuous (T _C = 25° C, V _{GS} = 10V) (Figure 2) I _D	75	А
Continuous (T _C = 100 ^o C, V _{GS} = 10V) (Figure 2) I _D	65	А
Pulsed Drain Current	Figure 4	
Pulsed Avalanche Rating UIS	Figures 6, 14, 15	
Power Dissipation	310	W
Derate Above 25°C	2.07	W/ ^o C
Operating and Storage Temperature	-55 to 175	°C
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	300	°C
Package Body for 10s, See Techbrief TB334	260	°C
NOTES:		

1. $T_{.1} = 25^{\circ}C$ to $150^{\circ}C$.

CAUTION: Stresses above those listed in "Absol24ute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

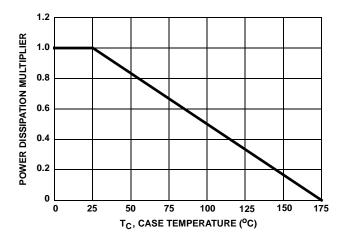
PARAMETER	SYMBOL	TEST	CONDITIONS	MIN	ТҮР	MAX	UNITS
OFF STATE SPECIFICATIONS				1	1	1	
Drain to Source Breakdown Voltage	BV _{DSS}	$I_{D} = 250\mu A, V_{GS} = 0V$ (Figure 11)		100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 95V, V_{GS} = 0^{10}$	V	-	-	1	μΑ
		$V_{DS} = 90V, V_{GS} = 0$	V, T _C = 150 ^o C	-	-	250	μΑ
Gate to Source Leakage Current	I _{GSS}	$V_{GS} = \pm 20V$		-	-	±100	nA
ON STATE SPECIFICATIONS	1						
Gate to Source Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D} = 250$	0μA (Figure 10)	2	-	4	V
Drain to Source On Resistance	rDS(ON)	I _D = 75A, V _{GS} = 10V (Figure 9)		-	0.0115	0.014	Ω
THERMAL SPECIFICATIONS	I					I	1
Thermal Resistance Junction to Case	R _{θJC}	TO-220 and TO-263		-	-	0.48	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}			-	-	62	°C/W
SWITCHING SPECIFICATIONS (V _{GS} =	= 10V)					I	
Turn-On Time	ton	$V_{DD} = 50V, I_D = 75A$ $V_{GS} = 10V,$ $R_{GS} = 2.5\Omega$		-	-	197	ns
Turn-On Delay Time	t _{d(ON)}			-	14	-	ns
Rise Time	tr	(Figures 18, 19)			117	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	41	-	ns
Fall Time	t _f	_	-		97	-	ns
Turn-Off Time	tOFF	1		-	-	207	ns
GATE CHARGE SPECIFICATIONS	I					1	I
Total Gate Charge	Q _{g(TOT)}	$V_{GS} = 0V$ to 20V	$V_{DD} = 50V,$ $I_{D} = 75A,$ $I_{g(REF)} = 1.0mA$ (Figures 13, 16, 17)	-	198	238	nC
Gate Charge at 10V	Q _{g(10)}	$V_{GS} = 0V$ to 10V		-	106	127	nC
Threshold Gate Charge	Q _{g(TH)}	$V_{GS} = 0V$ to 2V		-	6.8	8.2	nC
Gate to Source Gate Charge	Q _{gs}			-	14	-	nC
Gate to Drain "Miller" Charge	Q _{gd}			-	41	-	nC
CAPACITANCE SPECIFICATIONS			-	J.	-1	ı	1
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 12)		-	3790	-	pF
Output Capacitance	C _{OSS}			-	810	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	230	-	pF
	1	_1		I	1	1	1

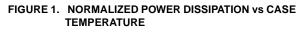
Electrical Specifications $T_C = 25^{\circ}C$, Unless Otherwise Specified

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V _{SD}	I _{SD} = 75A	-	-	1.25	V
		I _{SD} = 35A	-	-	1.00	V
Reverse Recovery Time	t _{rr}	I _{SD} = 75A, dI _{SD} /dt = 100A/μs	-	-	145	ns
Reverse Recovered Charge	Q _{RR}	I _{SD} = 75A, dI _{SD} /dt = 100A/μs	-	-	360	nC

Typical Performance Curves





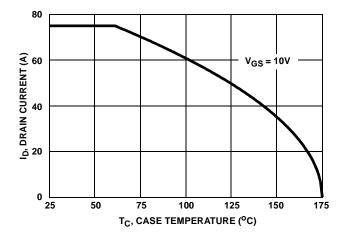
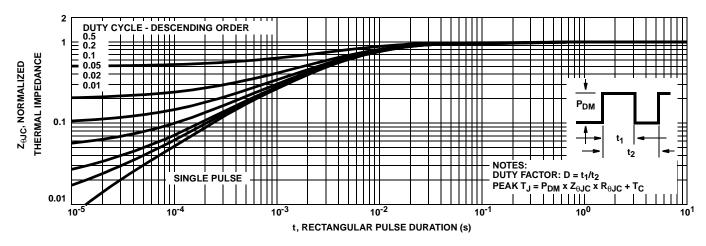
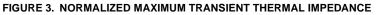


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE





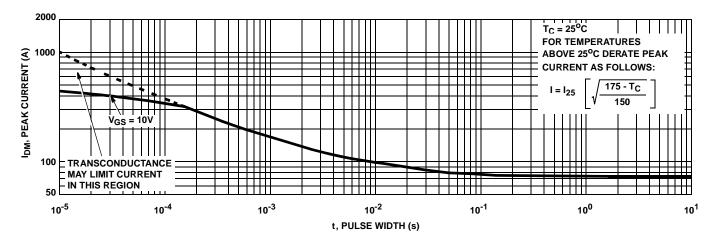


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

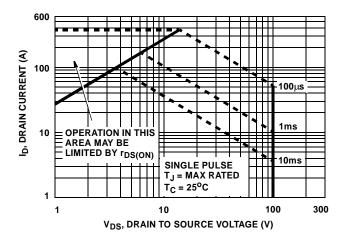


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

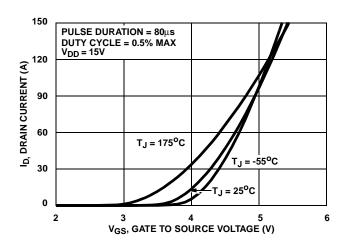


FIGURE 7. TRANSFER CHARACTERISTICS

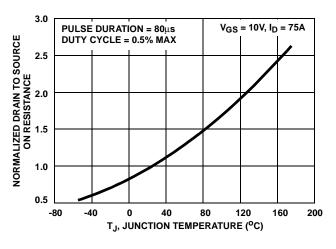
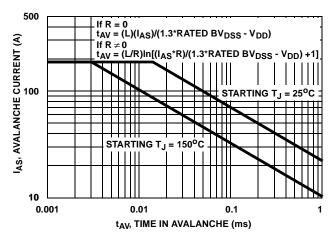


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON **RESISTANCE vs JUNCTION TEMPERATURE**



NOTE: Refer to ON Semiconductor Application Notes AN9321 and AN9322.



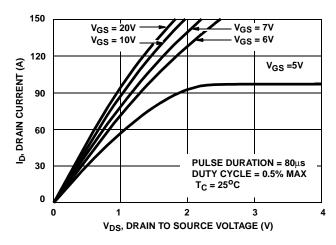
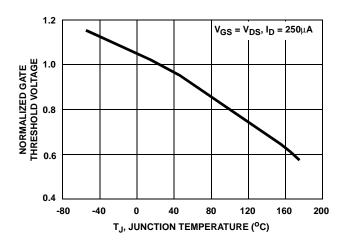
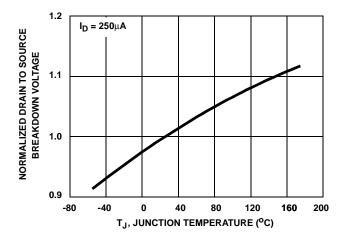


FIGURE 8. SATURATION CHARACTERISTICS





Typical Performance Curves (Continued)





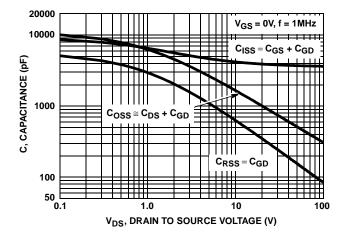
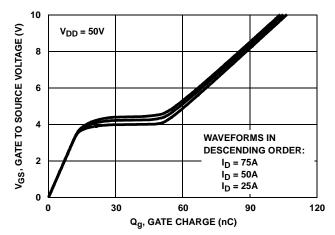


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE





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Test Circuits and Waveforms

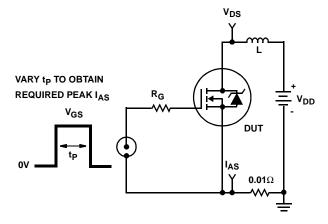


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

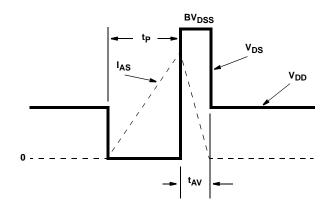


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

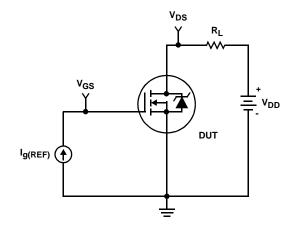


FIGURE 16. GATE CHARGE TEST CIRCUIT

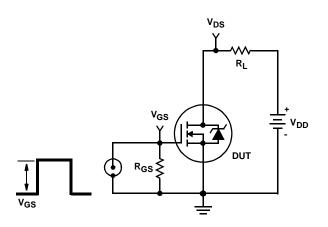
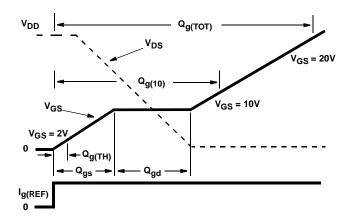


FIGURE 18. SWITCHING TIME TEST CIRCUIT





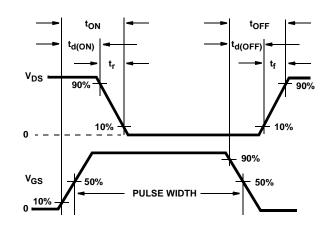
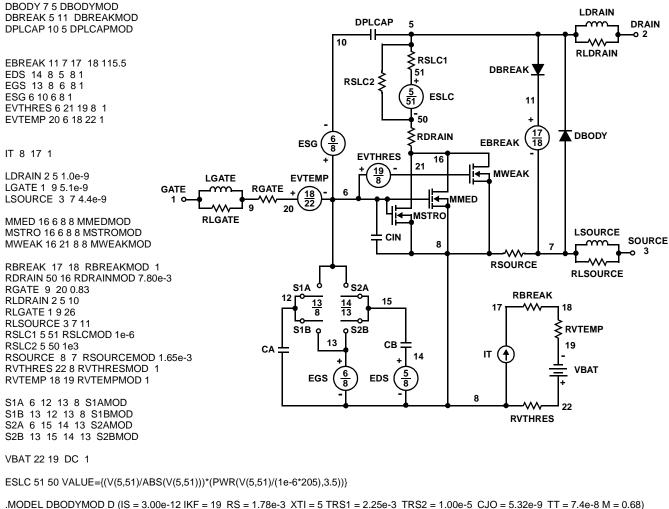


FIGURE 19. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

.SUBCKT HUF75645 2 1 3 ; rev 21 May 1999

CA 12 8 5.31e-9 CB 15 14 5.31e-9 CIN 6 8 3.56e-9



 $\begin{array}{l} \text{MODEL DBODTMOD D (IS = 3.000e+12 IKF = 1 9 KS = 1.78e- XTI = 5 TKS1 = 2.23e-3 TKS2 = 1.00e-3 CJO = 3.32e-3 TT = 7.4e-3 \\ \text{MODEL DBREAKMOD D (RS = 2.15e- 1IKF = 1 TRS1 = 8e- 4TRS2 = 3e-6) \\ \text{MODEL DPLCAPMOD D (CJO = 5.55e- 9IS = 1e-3 0M = 0.98) \\ \text{MODEL MMEDMOD NMOS (VTO = 3.13 KP = 10 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.83) \\ \text{MODEL MSTROMOD NMOS (VTO = 3.51 KP = 93 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.83) \\ \text{MODEL MWEAKMOD NMOS (VTO = 2.65 KP = 0.11 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 8.33) \\ \text{MODEL MWEAKMOD RMOS (VTO = 2.65 KP = 0.11 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 8.33) \\ \text{MODEL RBREAKMOD RES (TC1 = 9.9e- 4TC2 = -1.3e-6) \\ \text{MODEL RBREAKMOD RES (TC1 = 2.63e-3 TC2 = 2.93e-5) \\ \text{MODEL RSLCMOD RES (TC1 = 2.63e-3 TC2 = 1.05e-6) \\ \text{MODEL RSURCEMOD RES (TC1 = 2.63e-3 TC2 = 1.05e-6) \\ \text{MODEL RSURCEMOD RES (TC1 = -2.57e-3 TC2 = -7.05e-6) \\ \text{MODEL RVTHRESMOD RES (TC1 = -2.87e- 3TC2 = -2.21e-6) \\ \end{array}$

.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.4 VOFF = -6.2) .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.8 VOFF = 0.5) .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -1.8)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV 21 May 1999 template ta75645 n2,n1,n3 electrical n2,n1,n3 var i iscl d..model dbodymod = (is = 3.00e-12, cjo = 5.32e-9, tt = 7.4e-8, xti = 5, m = 0.68) d..model dbreakmod = () d..model dplcapmod = (cjo = 5.55e-9, is = 1e-30, vj=1.0, m = 0.8) m..model mmedmod = (type=_n, vto = 3.13, kp = 10, is = 1e-30, tox = 1) m..model mstrongmod = (type=_n, vto = 3.51, kp = 93, is = 1e-30, tox = 1) m..model mweakmod = (type=_n, vto = 2.65, kp = 0.11, is = 1e-30, tox = 1) LDRAIN sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -6.2, voff = -2.4) DPLCAP 5 DRAIN sw_vcsp..model s1bmod = (ron =1e-5, roff = 0.1, von = -2.4, voff = -6.2) o 2 10 $sw_vcsp...model s2amod = (ron = 1e-5, roff = 0.1, von = -1.8, voff = 0.5)$ RLDRAIN sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.5, voff = -1.8) RSLC1 RDBREAK 51 c.ca n12 n8 = 5.31e-9 RSLC2 ₹ 72 c.cb n15 n14 = 5.31e-9 RDBODY ISCL c.cin n6 n8 = 3.56e-9 DBREAK 50 d.dbody n7 n71 = model=dbodymod 71 RDRAIN d.dbreak n72 n11 = model=dbreakmod 6 8 ESG 11 d.dplcap n10 n5 = model=dplcapmod EVTHRES 16 21 19 8 MWEAK i.it n8 n17 = 1 i∙ LGATE EVTEMP DBODY RGATE GATE 6 18 22 EBREAK I.Idrain n2 n5 = 1e-9 MMED i∙ 1 C 9 \sim 20 1.0ate n1 n9 = 5.1e-9MSTR RLGATE l.lsource n3 n7 = 4.4e-9 LSOURCE CIN SOURCE 8 m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u 3 m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u RSOURCE m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u RLSOURCE S1A os2A res.rbreak n17 n18 = 1, tc1 = 9.9e-4, tc2 = -1.3e-6 RBREAK <u>13</u> 8 <u>14</u> 13 15 res.rdbody n71 n5 = 1.78e-3, tc1 = 2.25e-3, tc2 = 1.e-5 17 18 res.rdbreak n72 n5 = 2.15e-1, tc1 = 8e-4, tc2 = 3e-6 RVTEMP res.rdrain n50 n16 = 7.8e-3, tc1 = 9.4e-3, tc2 = 2.93e-5 o S2B S1B res.rgate n9 n20 = 0.83 13 СВ 19 CA res.rldrain n2 n5 = 10 IT (♠ 14 res.rlgate n1 n9 = 26 VBAT <u>6</u> 8 res.rlsource n3 n7 = 11 5 EGS EDS res.rslc1 n5 n51 = 1e-6, tc1 = 2.63e-3, tc2 = 1.05e-6 8 res.rslc2 n5 n50 = 1e3 22 res.rsource n8 n7 = 1.65e-3, tc1 = 1e-3, tc2 = 1e-6 RVTHRES res.rvtemp n18 n19 = 1, tc1 = -2.87e-3, tc2 = -2.21e-6 res.rvthres n22 n8 = 1, tc1 = -2.57e-3, tc2 = -7.05e-6 spe.ebreak n11 n7 n17 n18 = 115.5 spe.eds n14 n8 n5 n8 = 1 spe.egs n13 n8 n6 n8 = 1 spe.esg n6 n10 n6 n8 = 1 spe.evtemp n20 n6 n18 n22 = 1 spe.evthres n6 n21 n19 n8 = 1 sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod v.vbat n22 n19 = dc=1

equations {

i (n51->n50) +=iscl iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/205))** 3.5)) }

SPICE Thermal Model

REV 28 July 1999

HUF75645T

CTHERM1 th 6 8.80e-3 CTHERM2 6 5 2.50e-2 CTHERM3 5 4 2.70e-2 CTHERM4 4 3 3.70e-2 CTHERM5 3 2 4.40e-2 CTHERM6 2 tl 3.40e-1

RTHERM1 th 6 1.20e-2 RTHERM2 6 5 3.00e-2 RTHERM3 5 4 4.30e-2 RTHERM4 4 3 8.80e-2 RTHERM5 3 2 9.90e-2 RTHERM6 2 tl 1.10e-1

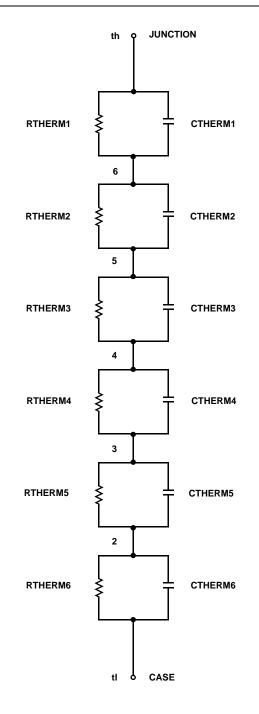
SABER Thermal Model

SABER thermal model HUF75645T

template thermal_model th tl thermal_c th, tl {

ctherm.ctherm1 th 6 = 8.80e-3ctherm.ctherm2 6 5 = 2.50e-2ctherm.ctherm3 5 4 = 2.70e-2ctherm.ctherm4 4 3 = 3.70e-2ctherm.ctherm5 3 2 = 4.40e-2ctherm.ctherm6 2 tl = 3.40e-1

rtherm.rtherm1 th 6 = 1.20e-2 rtherm.rtherm2 6 5 = 3.00e-2 rtherm.rtherm3 5 4 = 4.30e-2 rtherm.rtherm4 4 3 = 8.80e-2 rtherm.rtherm5 3 2 = 9.90e-2 rtherm.rtherm6 2 tl = 1.10e-1 }



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