

# ON Semiconductor

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The logo for onsemi, featuring the word "onsemi" in a dark teal, lowercase, sans-serif font. The letter "i" is stylized with a white dot and a teal vertical bar. A small orange triangle is positioned above the top right of the "i". A trademark symbol (TM) is located to the right of the logo.

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# HUFA75639S3ST-F085A

## 56A, 100V, 0.025 Ohm, N-Channel UltraFET Power MOSFETs



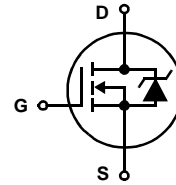
These N-Channel power MOSFETs are manufactured using the innovative UltraFET® process. This advanced process technology

achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

### Features

- 56A, 100V
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

### Symbol

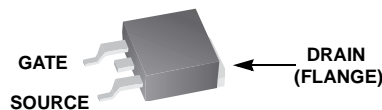


### Ordering Information

PART NUMBER	PACKAGE	BRAND
HUFA75639S3ST-F085A	TO263AB	75639S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUFA75639S3ST.

### Packaging



JEDEC TO-263AB

# HUFA75639S3ST-F085A

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DSS}$	100	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	100	V
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 20$	V
Drain Current			
Continuous (Figure 2) . . . . .	$I_D$	56	A
Pulsed Drain Current . . . . .	$I_{DM}$	Figure 4	
Pulsed Avalanche Rating . . . . .	$E_{AS}$	Figures 6, 14, 15	
Power Dissipation . . . . .	$P_D$	200	W
Derate Above $25^\circ\text{C}$ . . . . .		1.35	W/ $^\circ\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	$T_L$	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
<b>OFF STATE SPECIFICATIONS</b>							
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ (Figure 11)	100	-	-	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 95\text{V}, V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$	
		$V_{DS} = 90\text{V}, V_{GS} = 0\text{V}, T_C = 150^\circ\text{C}$	-	-	250	$\mu\text{A}$	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA	
<b>ON STATE SPECIFICATIONS</b>							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ (Figure 10)	2	-	4	V	
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 56\text{A}, V_{GS} = 10\text{V}$ (Figure 9)	-	0.021	0.025	$\Omega$	
<b>THERMAL SPECIFICATIONS</b>							
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	0.74	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247	-	-	30	$^\circ\text{C/W}$	
		TO-220, TO-263	-	-	62	$^\circ\text{C/W}$	
<b>SWITCHING SPECIFICATIONS (<math>V_{GS} = 10\text{V}</math>)</b>							
Turn-On Time	$t_{ON}$	$V_{DD} = 50\text{V}, I_D \cong 56\text{A},$ $R_L = 0.89\Omega, V_{GS} = 10\text{V},$ $R_{GS} = 5.1\Omega$	-	-	110	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	15	-	ns	
Rise Time	$t_r$		-	60	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	20	-	ns	
Fall Time	$t_f$		-	25	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	70	ns	
<b>GATE CHARGE SPECIFICATIONS</b>							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V}$ to $20\text{V}$	$V_{DD} = 50\text{V},$ $I_D \cong 56\text{A},$ $R_L = 0.89\Omega$ $I_{g(REF)} = 1.0\text{mA}$ (Figure 13)	-	110	130	nC
Gate Charge at 10V	$Q_{g(10)}$	$V_{GS} = 0\text{V}$ to $10\text{V}$		-	57	75	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V}$ to $2\text{V}$		-	3.7	4.5	nC
Gate to Source Gate Charge	$Q_{gs}$			-	9.8	-	nC
Gate to Drain "Miller" Charge	$Q_{gd}$			-	24	-	nC

# HUFA75639S3ST-F085A

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>CAPACITANCE SPECIFICATIONS</b>						
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$ (Figure 12)	-	2000	-	pF
Output Capacitance	$C_{OSS}$		-	500	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	65	-	pF

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 56\text{A}$	-	-	1.25	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 56\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	110	ns
Reverse Recovered Charge	$Q_{RR}$	$I_{SD} = 56\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	320	nC

## Typical Performance Curves

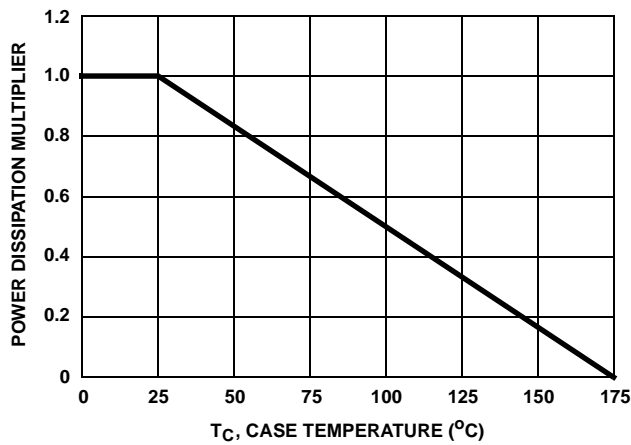


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

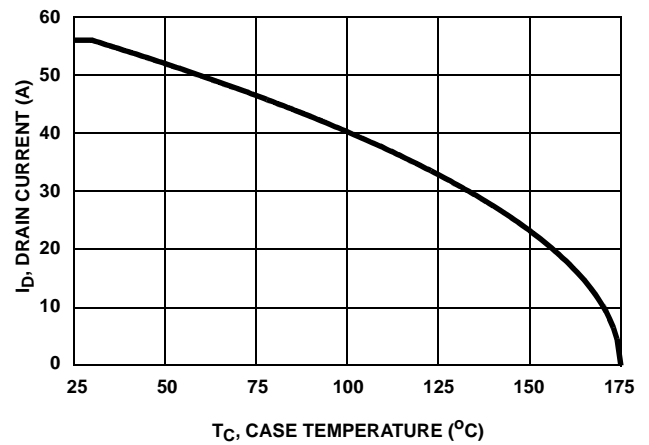


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

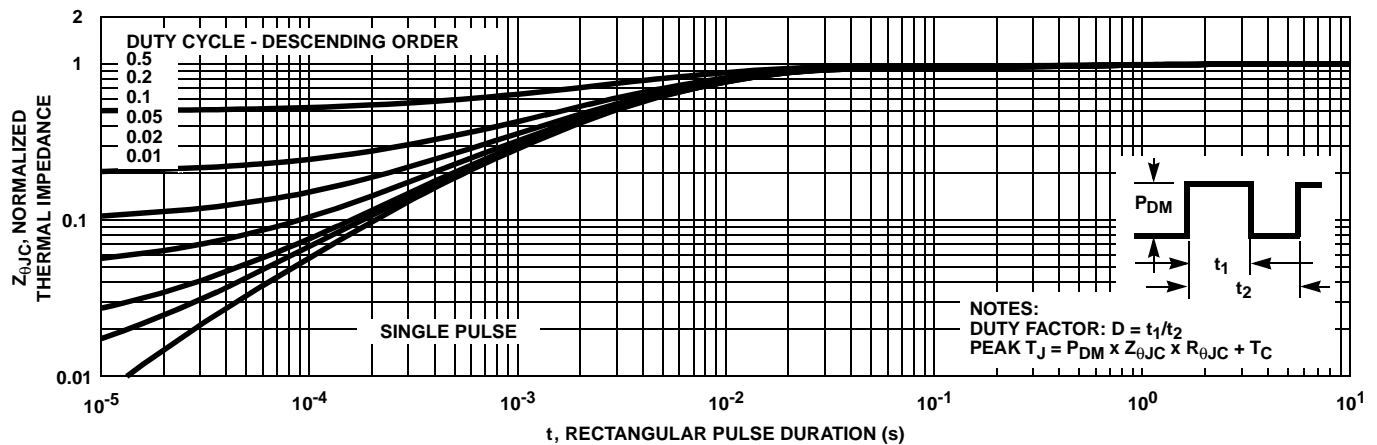


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves (Continued)

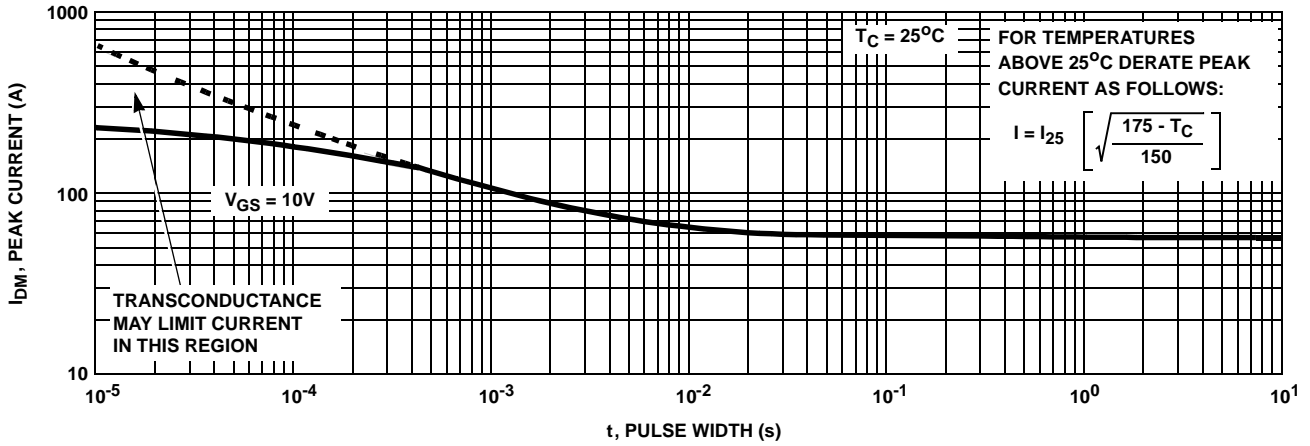


FIGURE 4. PEAK CURRENT CAPABILITY

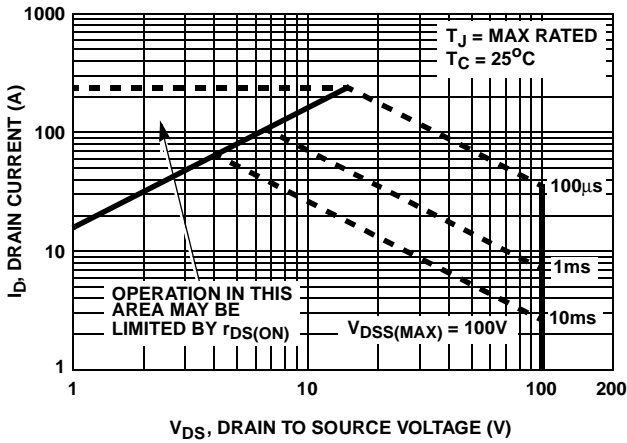
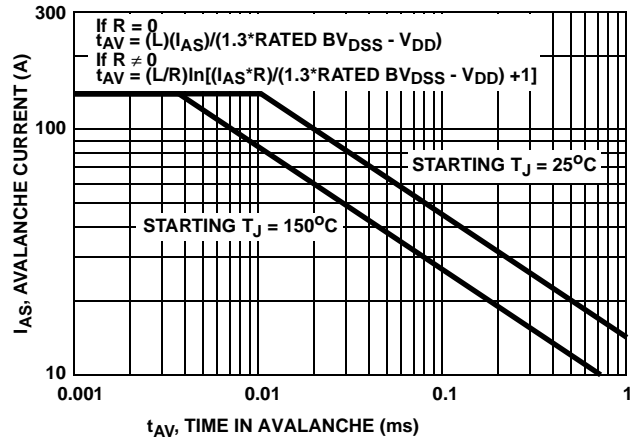


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to ON Semiconductor Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

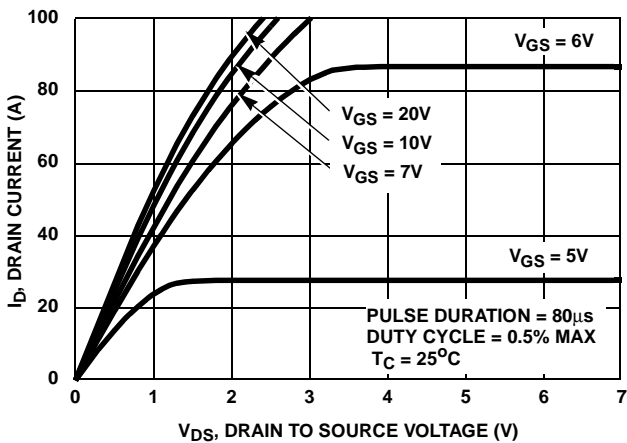


FIGURE 7. SATURATION CHARACTERISTICS

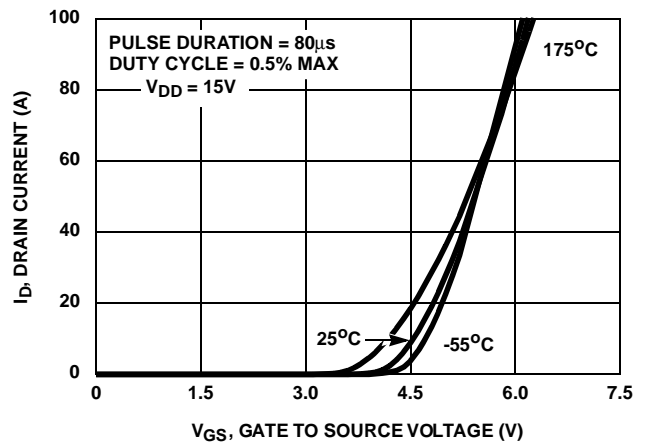


FIGURE 8. TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

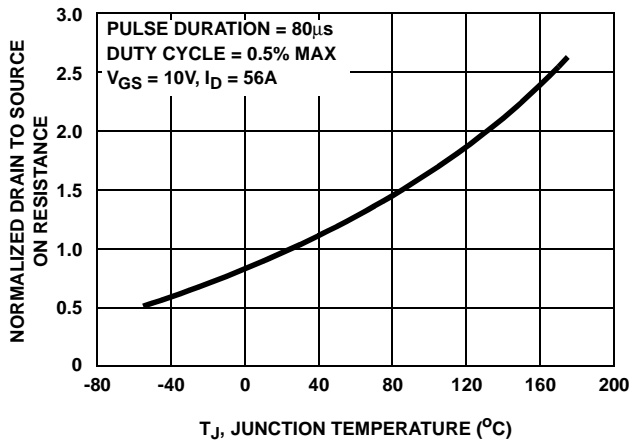


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

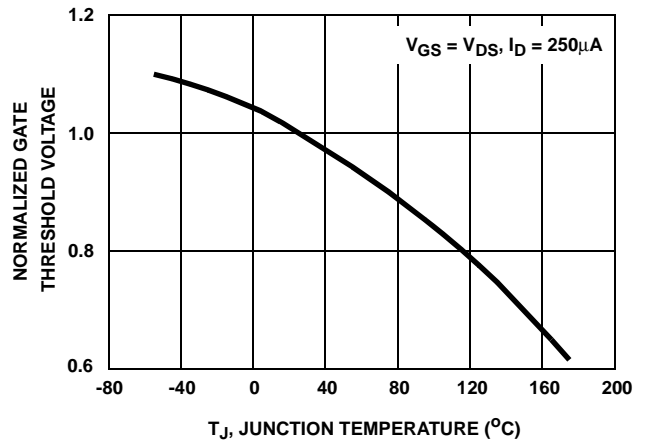


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

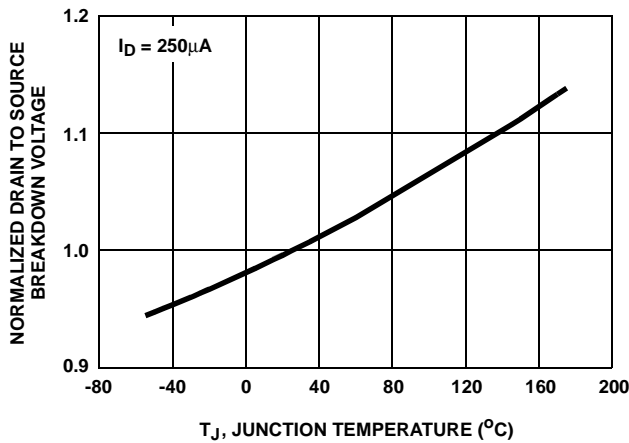


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

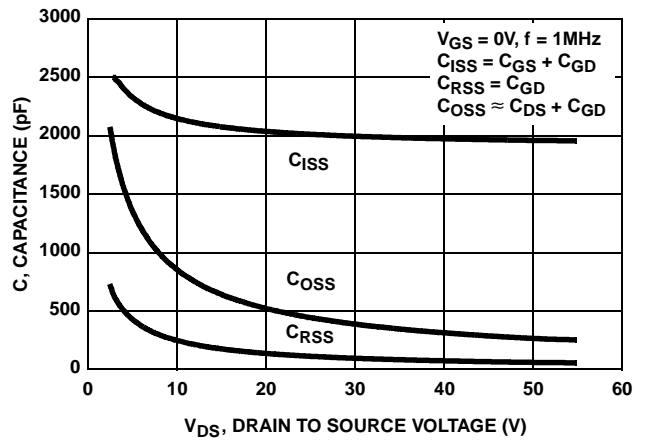
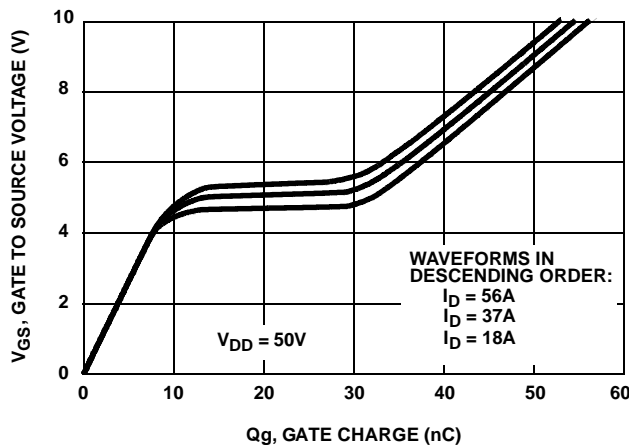


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to ON Semiconductor Application Notes AN7254 and AN7260.  
FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

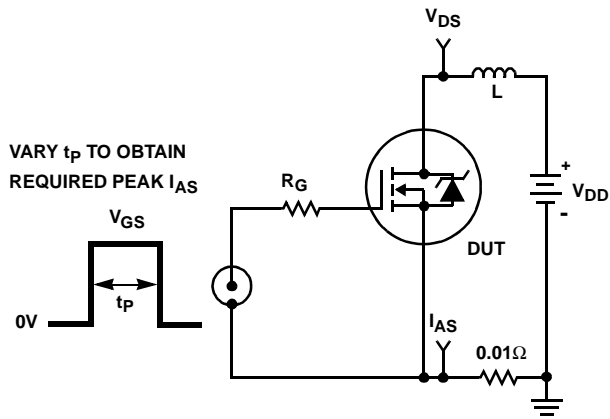


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

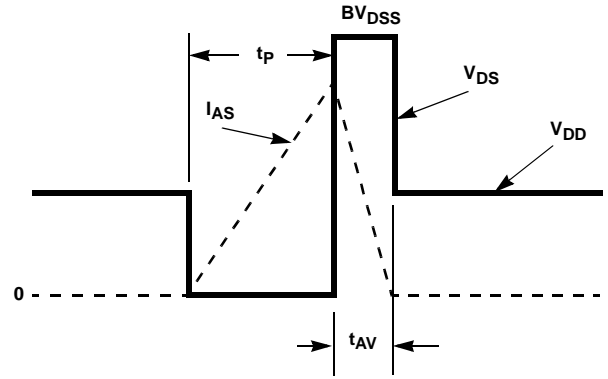


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

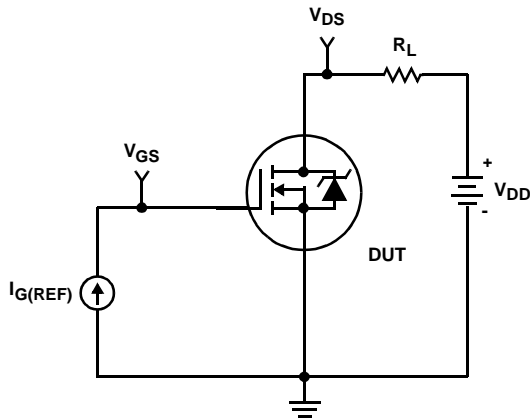


FIGURE 16. GATE CHARGE TEST CIRCUIT

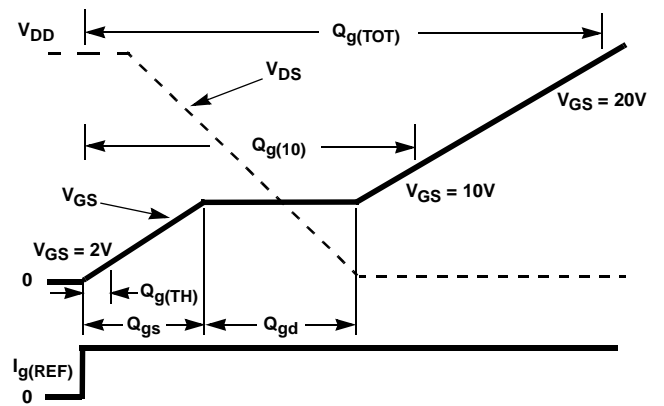


FIGURE 17. GATE CHARGE WAVEFORM

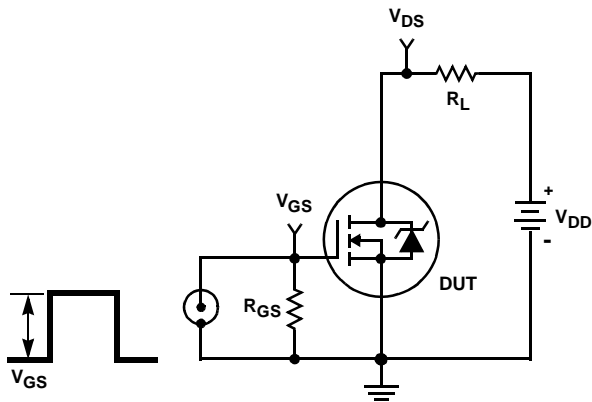


FIGURE 18. SWITCHING TIME TEST CIRCUIT

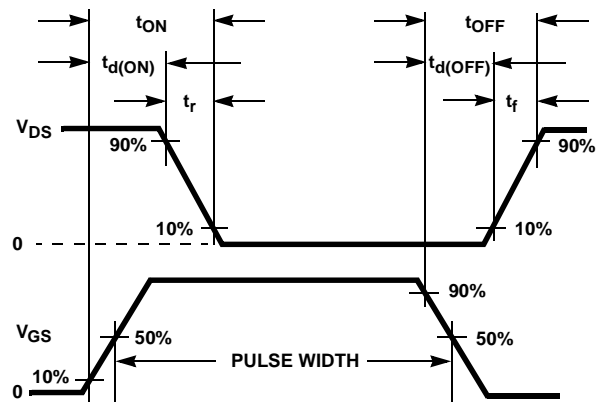



FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

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