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December 2013

## IRL640A

# N-Channel Logic Level A-FET 200 V, 18 A, 180 m $\Omega$

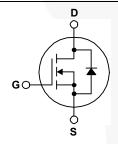
#### **Description**

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supplies, DC-AC converters for uninterrupted power supply and motor control.

#### **Features**

- 18 A, 200 V,  $R_{DS(on)}$  = 180 m $\Omega$  @  $V_{GS}$  = 5 V
- Low Gate Charge (Typ. 40 nC)
- Low Crss (Typ. 95 pF)
- · Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- · Logic-Level Gate Drive





#### **Absolute Maximum Ratings**

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	200	V
	Continuous Drain Current (T <sub>C</sub> =25°C)	18	
I <sub>D</sub>	Continuous Drain Current (T <sub>C</sub> =100°C)	11.4	A
I <sub>DM</sub>	Drain Current-Pulsed (1)	63	Α
$V_{GS}$	Gate-to-Source Voltage	±20	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (2)	64	mJ
I <sub>AR</sub>	Avalanche Current (1)	18	Α
E <sub>AR</sub>	Repetitive Avalanche Energy (1)	11	mJ
dv/dt	Peak Diode Recovery dv/dt (3)	5	V/ns
	Total Power Dissipation (T <sub>C</sub> =25°C)	110	W
$P_{D}$	Linear Derating Factor	0.88	W/°C
	Operating Junction and	55 ( 450	
$T_J$ , $T_STG$	Storage Temperature Range	- 55 to +150	
<b>-</b>	Maximum Lead Temp. for Soldering	000	°C
$T_L$	Purposes, 1/8. from case for 5-seconds	300	

#### Thermal Resistance

Symbol	Characteristic	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-Case		1.14	
$R_{\theta CS}$	Case-to-Sink	0.5		°C/W
$R_{\theta JA}$	Junction-to-Ambient		62.5	

### **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
IRL640A	IRL640A	TO-220	Tube	N/A	N/A	50 units

## **Electrical Characteristics** ( $T_{\rm C}$ =25 $^{\circ}{\rm C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Тур.	Max.	Units	Test Condition	
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	200			V	$V_{GS} = 0V, I_{D} = 250 \mu A$	
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.		0.17		V/°C	I <sub>D</sub> =250μA	
$V_{GS(th)}$	Gate Threshold Voltage	1.0		2.0	V	$V_{DS} = 5V, I_{D} = 250 \mu A$	
ı	Gate-Source Leakage, Forward			100	nA	V <sub>GS</sub> =20V	
I <sub>GSS</sub>	Gate-Source Leakage, Reverse			-100	ПА	V <sub>GS</sub> =-20V	
	Dunin to Course I column Cumant			10		V <sub>DS</sub> =200V	
I <sub>DSS</sub>	Drain-to-Source Leakage Current		-	100	μΑ	V <sub>DS</sub> =160V,T <sub>C</sub> =125°C	
	Static Drain-Source					V 5VI 0A (4)	
R <sub>DS(on)</sub>	On-State Resistance	0.1		0.18	Ω	$V_{GS}=5V,I_{D}=9A \qquad (4)$	
$g_{fs}$	Forward Transconductance		13.3		Ω	$V_{DS} = 40V, I_{D} = 9A$ (4)	
C <sub>iss</sub>	Input Capacitance		1310	1705		\\ 0\\\\ 25\\\$ 4MH=	
C <sub>oss</sub>	Output Capacitance		200	250	рF	$V_{GS}=0V, V_{DS}=25V, f=1MHz$	
C <sub>rss</sub>	Reverse Transfer Capacitance		95	120		See Fig 5	
t <sub>d(on)</sub>	Turn-On Delay Time		11	30		V 400VI 40A	
t <sub>r</sub>	Rise Time		8	25	20	$V_{DD} = 100 V, I_{D} = 18 A,$	
t <sub>d(off)</sub>	Turn-Off Delay Time		46	100	ns $R_G=4.6\Omega$		
t <sub>f</sub>	Fall Time		15	40		<b>See Fig 13</b> (4) (5)	
$Q_g$	Total Gate Charge		40	56		V <sub>DS</sub> =160V,V <sub>GS</sub> =5V,	
$Q_gs$	Gate-Source Charge		6.8		nC	I <sub>D</sub> =18A	
$Q_{gd}$	Gate-Drain (. Miller. ) Charge		18.6			See Fig 6 & Fig 12 (4) (5)	

## Source-Drain Diode Ratings and Characteristics

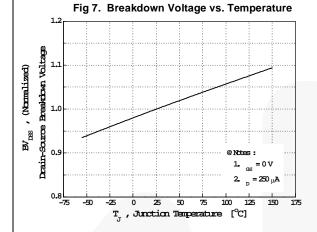
Symbol	Characteristic	Min.	Тур.	Max.	Units	Test Condition
I <sub>S</sub>	Continuous Source Current		1	18	^	Integral reverse pn-diode
I <sub>SM</sub>	Pulsed-Source Current (1)		1	63	Α	in the MOSFET
$V_{SD}$	Diode Forward Voltage (4)		I	1.5	V	T <sub>J</sub> =25°C,I <sub>S</sub> =18A,V <sub>GS</sub> =0V
t <sub>rr</sub>	Reverse Recovery Time		224		ns	T <sub>J</sub> =25°C,I <sub>F</sub> =18A
Q <sub>rr</sub>	Reverse Recovery Charge		1.55		μС	$di_F/dt=100A/\mu s$ (4)

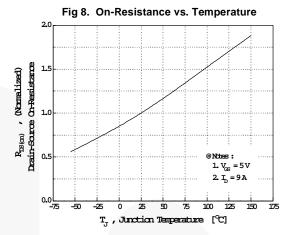
#### Notes:

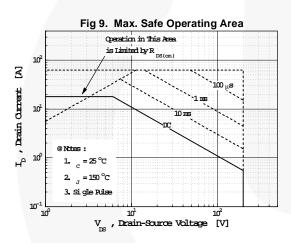
- (1) Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- (2) L=0.3mH, I<sub>AS</sub>=18A, V<sub>DD</sub>=50V, R<sub>G</sub>=27 $\Omega$ , Starting T<sub>J</sub>=25°C
- (3)  $I_{SD} \le 18A$ ,  $di/dt \le 260A/\mu s$ ,  $V_{DD} \le BV_{DSS}$ , Starting  $T_J = 25^{\circ}C$ (4) Pulse Test: Pulse Width = 250 $\mu s$ , Duty Cycle  $\le 2\%$
- (5) Essentially Independent of Operating Temperature

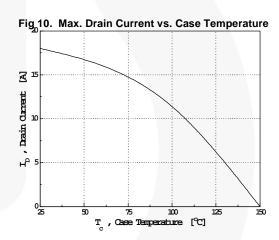
#### **Typical Characteristics** Fig 1. Output Characteristics Fig 2. Transfer Characteristics V<sub>GS</sub> Top: 60 V 55 V ₹ $\Xi$ 10<sup>1</sup> 45V 40V Ip , Drain Current 10<sup>1</sup> Drain Current 35 V Bottom: 3.0 V 100 1. $_{\rm GS}$ = 0 V <sub>DS</sub> = 40 V 2. 1. 25 μs Pulse c = 25 °C 10<sup>-1</sup> 10<sup>-1</sup> 10° 10<sup>1</sup> V Drain-Source Voltage [V] V<sub>GS</sub> , Gatte-Source Voltage [V] Fig 3. On-Resistance vs. Drain Current Fig 4. Source-Drain Diode Forward Voltage ₹ In , Reverse Drain Current Drain-Source On-Resistance 10<sup>1</sup> $R_{be(cm)}$ , [ $\Omega$ ] 0.1 1. <sub>GS</sub> = 0 V @Note: $T_{_{\!\mathcal{I}}} = 25\,^{\circ}\mathrm{C}$ 2. 25 $\mu$ s Rulse Test 0.0 10 I , Drain Current [A] 0.4 1.0 1.2 1.4 1.6 V<sub>SD</sub> , Source-Drain Voltage [V] Fig 5. Capacitance vs. Drain-Source Voltage Fig 6. Gate Charge vs. Gate-Source Voltage C<sub>iss</sub>=C<sub>gs</sub>+C<sub>gd</sub> (C<sub>ds</sub>=shorted) $C_{oss} = C_{ds} + C_{gd}$ Crss=Cgd $V_{DS} = 40 \text{ V}$ Σ $V_{DS} = 100 \text{ V}$ ď $V_{\rm GB}$ , Gatte-Source Voltage V<sub>DS</sub> = 160 V Capacitance @ Notes: 1. $V_{GS} = 0 \text{ V}$ 2. f = 1 MHz 0L 20 30 40 Q, , Total Gate Charge [nC] V<sub>DS</sub> , Drain-Source Voltage [V]

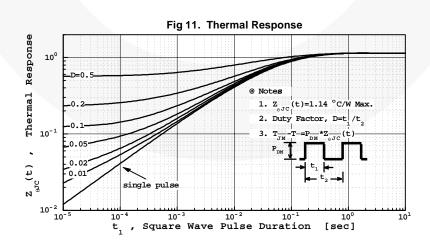
### Typical Characteristics (continued)











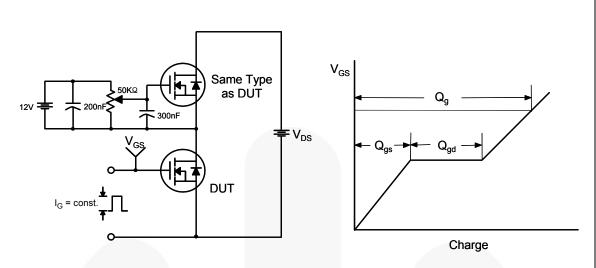


Figure 12. Gate Charge Test Circuit & Waveform

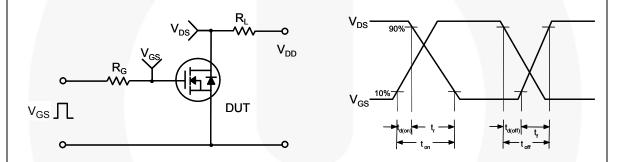


Figure 13. Resistive Switching Test Circuit & Waveforms

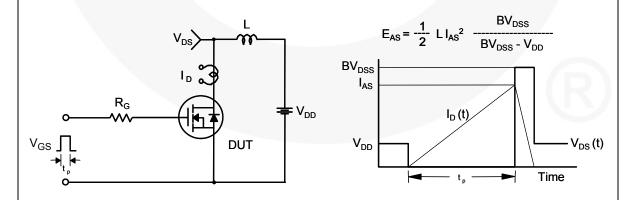
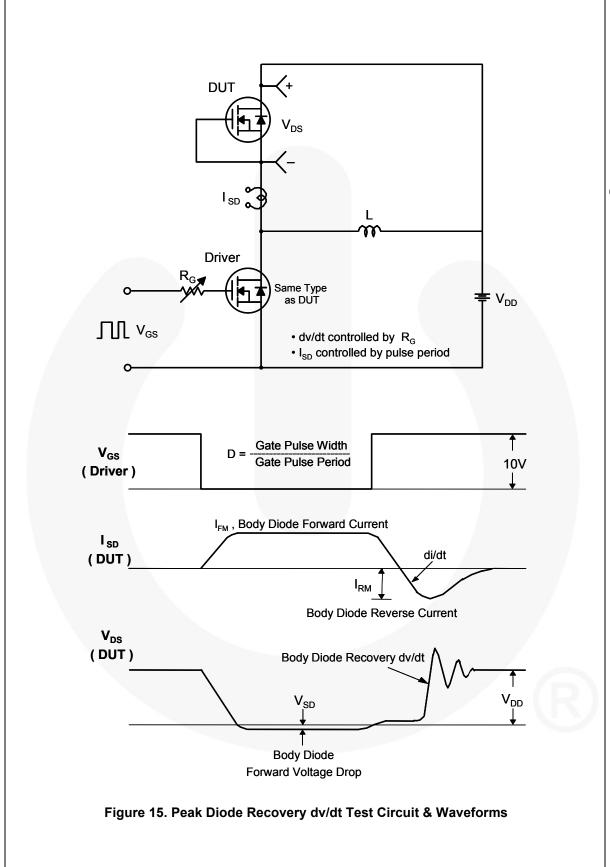


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



#### **Mechanical Dimensions**

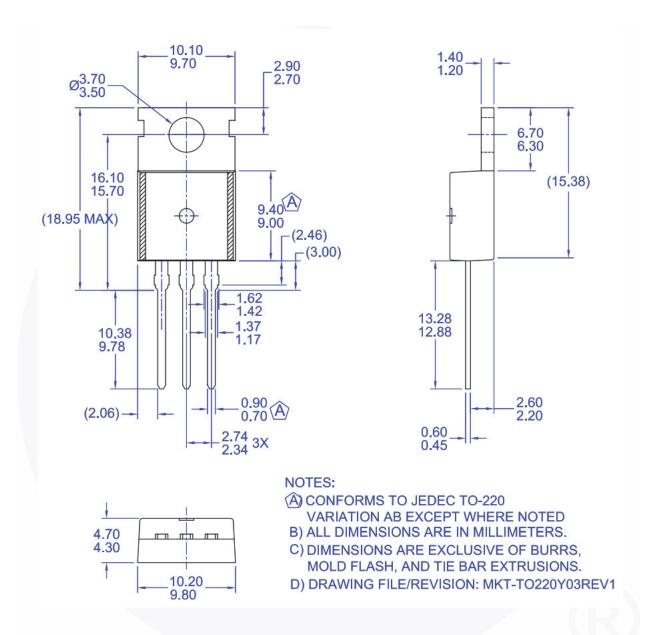


Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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