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February 2013

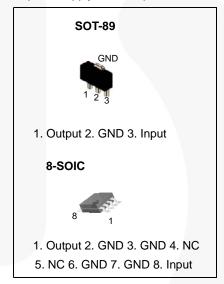
KA78L05AI 3-Terminal 0.1 A 5 V Positive Voltage Regulator

Features

- · Maximum Output Current of 100 mA
- · Output Voltage of 5 V
- Thermal Overload Protection
- · Short-Circuit Current Limiting
- Output Voltage Offered in ±5% Tolerance

Description

The KA78L05Al of fixed-voltage monolithic integrated circuit voltage regulators are suitable for applications that required supply current up to 100 mA.



Ordering Information

Product Number	Package	Packing Method	Output Voltage Tolerance	Operating Temperature		
KA78L05AIDTF	8-SOIC	Tape and Reel	±5%	-40 to +125°C		
KA78L05AIMTF	SOT-89	Tape and Reel	±3 /%	-40 t0 +125 C		

1

Block Diagram

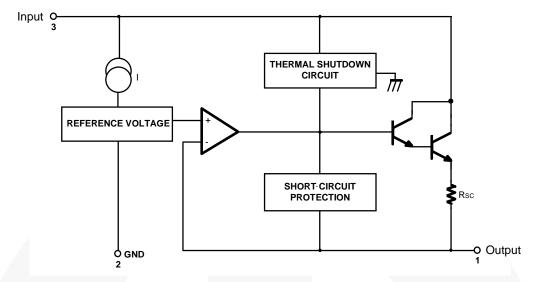


Figure 1. Block Diagram

Absolute Maximum Ratings(1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^{\circ}\text{C}$ unless otherwise noted.

Symbol	Parameter		Value	Unit
V _I	Input Voltage		30	V
T_J	Maximum Operating Junction Temperature	150	°C	
T _{OPR}	Operating Temperature Range	-40 to +125	°C	
T _{STG}	Storage Temperature Range	-65 to +150	°C	
D	Thermal Resistance Junction-Air	SOT-89	225	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Air	8-SOIC	160	°C/W

Note:

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
 Electrical specifications do not apply when operating the device outside of its stated operating conditions.

Electrical Characteristics

 $V_I = 10 \text{ V, } I_O = 40 \text{ mA, } -40^{\circ}C \leq T_J \leq 125^{\circ}C, \ C_I = 0.33 \ \mu\text{F, } C_O = 0.1 \ \mu\text{F, unless otherwise specified.}$

Symbol	Parameter		Conditions		Min.	Тур.	Max.	Unit
Vo	Output Voltage		T _J = 25°C		4.8	5.0	5.2	V
ΔV_{O}	Line Regulation ⁽²⁾		T _J = 25°C	$7 \text{ V} \leq \text{V}_{\text{I}} \leq 20 \text{ V}$		8	150	mV
700				$8 \text{ V} \leq \text{V}_{\text{I}} \leq 20 \text{ V}$		6	100	mV
ΔV_{O}	Load Regulation ⁽²⁾		T _J = 25°C	$1~\text{mA} \le I_O \le 100~\text{mA}$		11	60	mV
ΔνΟ				1 mA \leq I _O \leq 40 mA		5.0	30.0	mV
V	Output Voltage		7 V ≤V _I ≤ 20 V	1 mA \leq I _O \leq 40 mA	4.75		5.25	V
Vo			$7 \text{ V} \leq \text{V}_{\text{I}} \leq \text{V}_{\text{MAX}}^{(3)}$	$1 \text{ mA} \le I_O \le 70 \text{ mA}$	4.75		5.25	V
IQ	Quiescent Current		T _J = 25°C			2.0	5.5	mA
ΔI_{Q}	Quiescent Current	With Line	8 V ≤V _I ≤ 20 V				1.5	mA
ΔI_{Q}	Change	With Load	$1 \text{ mA} \le I_{O} \le 40 \text{ mA}$	\ ⁽⁴⁾			0.5	mA
V _N	Output Noise Voltage ⁽⁴⁾		T _A = 25°C, 10 Hz	≤ f ≤ 100 kHz		40		μV/Vo
$\Delta V_{O}/\Delta T$	Temperature Coefficient of V _O ⁽⁴⁾		$I_O = 5 \text{ mA}$			-0.65		mV/°C
RR	Ripple Rejection ^{(4), (5)}		f = 120 Hz, 8 V ≤ 3	V _I ≤ 18 V, T _J = 25°C	41	80		dB
V_D	Dropout Voltage		T _J = 25°C			1.7		V

Notes:

- The maximum steady-state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represents pulse test conditions with junction temperature as indicated at the initiation of tests.
- 3. Power dissipation $P_D \le 0.75 \text{ W}$.
- 4. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
- 5. Recommend minimum load capacitance of 0.01 μF to limit high-frequency noise.

Typical Application(6)

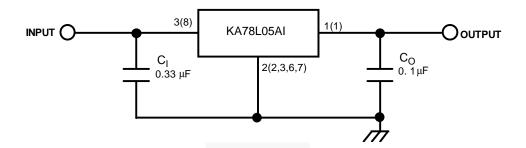


Figure 2. Typical Application

Note:

6. C_1 is required if the regulator is located an appreciable distance from the power supply filter. Though C_0 is not needed for stability, it improves transient response. Bypass capacitors are recommended for optimum stability and transient response and should be located as close as possible to the regulator.

Physical Dimensions

SOT-89

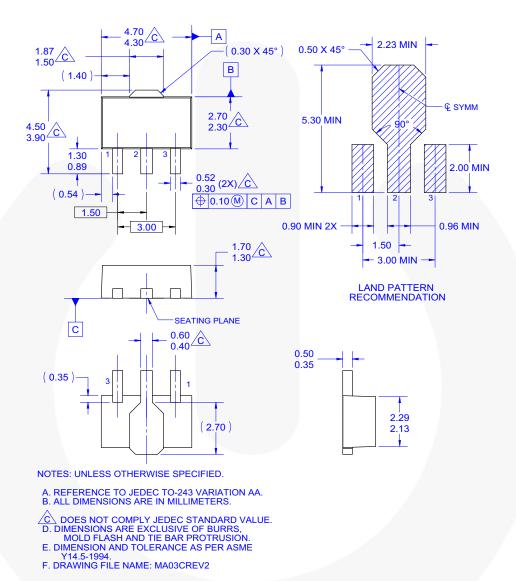


Figure 3. 3-Lead, SOT-89, JEDEC TO-243, Option AA

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Physical Dimensions (Continued)

8-SOIC

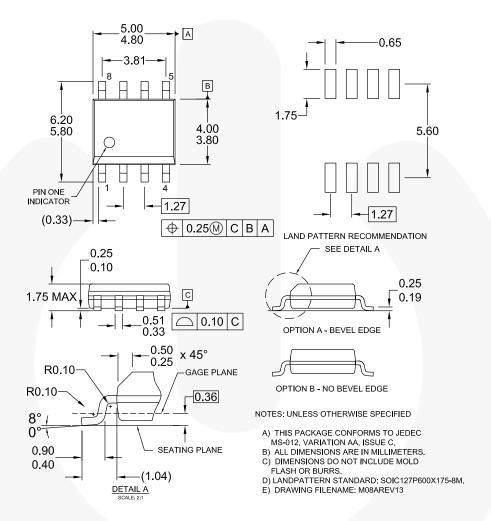


Figure 4. 8LD, SOIC, JEDEC MS-012, 0.150" NARROW BODY

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