EVBUM2284/D

KLI-4104 Imager Board User's Manual

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EVAL BOARD USER'S MANUAL

Description

The KLI−4104 Imager Evaluation Board, referred to in this document as the Imager Board, is designed to be used as part of a two−board set, used in conjunction with a Timing Generator Board. ON Semiconductor offers an Imager Board / Timing Generator Board package that has been designed and configured to operate with the KLI−4104 Image Sensors.

The Timing Generator Board generates the timing signals necessary to operate the CCD, and provides the power required by the Imager Board. The timing signals, in LVDS format, and the power, are provided to the Imager Board via the interface connector (J5). In addition, the Timing Generator Board performs the processing and digitization of the analog video output of the Imager Board.

The KLI−4104 Imager Board has been designed to operate the KLI−4104 with the specified performance at 30 MHz pixel clocking rate and nominal operating conditions. (See the KLI−4104 performance specifications for details).

For testing and characterization purposes, the KLI−4104 Imager board provides the ability to adjust many of the CCD bias voltages and CCD clock level voltages by adjusting potentiometers on the board. The Imager Board provides the means to modify other device operating parameters (e.g., CCD Reset clock pulse width, Input Diode clock pulse width) by populating components differently on the board.

INPUT REQUIREMENTS

Table 1. POWER REQUIREMENTS

Power Supplies	Minimum	Typical	Maximum	Units	Comments
+5 V_MTR Supply	4.9	5.0	5.1	V	
		1.3		A	
−5 V_MTR Supply	−5.1	−5.0	−4.9	V	
		0.2		A	
VPLUS Supply	18	20	21	V	
		1.8		A	
Total Power Dissipation		42		W	Air cooling recommended

Table 2. SIGNAL LEVEL REQUIREMENTS

Input Signals (LVDS)	V_{min}	$V_{threshold}$	V_{max}	Units	Comments
H1A (±)	0	±0.1	2.4	V	H1 clock
H1B (±)	0	±0.1	2.4	V	ID clock
H2A (±)	0	±0.1	2.4	V	H2 clock
H2B (±)	0	±0.1	2.4	V	(not used)
FDG	0	±0.1	2.4	V	LOGR clock
R (±)	0	±0.1	2.4	V	Reset clock
V1 (±)	0	±0.1	2.4	V	TG1 clock
V2 (±)	0	±0.1	2.4	V	TG2 clock
V2B (±)	0	±0.1	2.4	V	LOGB clock
V3RD (±)	0	±0.1	2.4	V	LOGG clock
VES (±)	0	±0.1	2.4	V	LOGL clock

KLI−4104 IMAGER BOARD ARCHITECTURE OVERVIEW

The following sections describe the functional blocks of the KLI−4104 Imager Board; refer to Figure 1 and the schematics.

Power Filtering and Regulation

Power is supplied to the Imager Board via the J1 interface connector. The power supplies are de−coupled and filtered with ferrite beads and capacitors to suppress noise. Voltage regulators are used to create the +15 V supply from the VPLUS supply.

NOTE: Because of the large capacitive load of the CCD horizontal clocks, the VPLUS supply will typically draw 1.8 A of current and heat sinking is installed under the voltage regulators VR1 and VR2. In addition, it is recommended that a cooling fan be placed to the side of the board to create air flow over the heat sinks. This will prevent the CCD image sensor from exceeding its recommended operating temperature.

LVDS Receivers / TTL Buffers

LVDS timing signals are input to the Imager Board via the J5 board interface connector. These signals are shifted to TTL levels before being sent to the CCD clock drivers.

CCD Pixel−Rate Clock Drivers (H1, H2 & Reset Clocks)

The pixel rate CCD clock drivers utilize two fast switching transistors that are designed to translate TTL−level input clock signals to the voltage levels required by the CCD. The high level of the CCD clocks is set by potentiometers buffered by operational amplifiers. High−current pin drivers are used to drive the CCD Horizontal clock gates. In order to effectively drive the capacitance of the Chroma Horizontal clock gates on the KLI−4104, multiple pin drivers are configured in parallel.

H1L CCD Timing Adjustment Potentiometers

Minor timing adjustments can be made to the H1L CCD right and left clock positions using the delay adjust potentiometers R180 and R181. Each potentiometer, along with a capacitor, forms an RC network that acts to delay the position of the H1L clock with respect to the H1A clock.

Reset Clock & ID Clock One−Shots

The pulse widths of the RESET_CCD and ID_CCD clocks are set by programmable One−Shots. Each One−Shot can be configured to provide a clock signal with a pulse width from 5 ns to 15 ns.

CCD TGCLK Drivers

The Transfer Gate clock (TGCLK) drivers consist of MOSFET driver IC's. These drivers are designed to translate the TTL−level clock signals to the voltage levels required by the CCD. The high voltage levels of the TG clocks are set by potentiometers buffered by operational amplifiers.

CCD LOG Drivers

The Exposure Control (LOG) clocks are independently controlled line−rate clocks, driven by a quad high−current pin driver. The LOG_HIGH voltage level is set by a resistor divider circuit, and is buffered by an operational amplifier.

CCD Bias Voltages

The CCD bias voltages (TG1L, IG, OG, LS, RD) are set by potentiometers, buffered by operational amplifiers. The bias voltages are de−coupled at the CCD pin.

CCD Image Sensor

This evaluation board supports the KLI−4104 Interline Image Sensor.

Emitter−Follower

The VOUT_CCD signals are buffered using bipolar junction transistors in the emitter−follower configuration. These circuits also provide the necessary 5 mA current sink for the CCD output circuits.

Line Drivers

The buffered VOUT_CCD signals are AC−coupled and driven from the Imager Board by operational amplifiers in a non−inverting configuration. The operational amplifiers are configured to have a gain of 1.125, to compensate for the high amplitude video output, and to correctly drive 75 Ω video coaxial cabling from the SMB connectors.

Optional DAC Input Connector (P1)

The P1 connector is provided for ON Semiconductor test purposes, and is not populated.

KLI−4104 OPERATIONAL SETTINGS

The Imager board is configured to operate the KLI−4104 Image Sensors under the following operating conditions:

DC Bias Voltages

The following voltages are fixed, or adjusted with a potentiometer as noted. The nominal values listed in Table 3 were correct at the time of this document's publication, but may be subject to change; refer to the KLI−4104 device specification.

Table 3. DC BIAS VOLTAGES

Description	Symbol	Min	Nominal	Max	Units	Potentiometer	Notes
Output Amplifier Supply	VDD		15.0		V		
Substrate	VSUB		0.0		V		
Accumulation Phase Bias, Luma	TG1L	0.0	0.0	7.5	V	R62	1, 2
Reset Drain	RD	7.3	11.0	14.5	V	R75	1
Light Shield / Drain Bias	LS	7.3	15.0	15.0	V	R33	1, 3
Test Pin − Input Gate	IG	0.0	0.0	7.5	V	R61	1, 4
Output Gate	OG	0.0	0.7	2.5	V	R42	1

1. The Min and Max voltages in the table indicate the imager board potentiometer adjustable voltage range. These values may exceed the specified CCD operating conditions. See the KLI−4104 device specification for details.
2. For Test purposes only, the TG1L signal is adjustable up to 7.5 V; it is fixed at 0.0 V by populating R218 and removing R85.
3. For Test purposes only, the LS signal is adjustable up to 14.5 V; it is fixed at +15.0 V by populating R217 and removing R98.
4. For Test purposes only, the IG signal is adjustable up to 7.5 V; it is fixed at 0.0 V by populating R43 and removing R44.

Clock Voltages

The following clock voltage levels are fixed, or adjusted with a potentiometer as noted. The nominal values listed in Table 4 were correct at the time of this document's publication, but may be subject to change; refer to the KAI−4011 / KAI−4021 /KAI−04022 device specification.

Table 4. CLOCK VOLTAGES

Description	Symbol	Level	Min	Nom	Max	Unit	Potentiometer	Notes
H1 Horizontal CCD Clock	H1xx_CCD	Low		0.0		V		
		High	4.7	7.25	9.4	V	R199	5, 6
H2 Horizontal CCD Clock	H2xx_CCD	Low		0.0		V		
		High	4.7	7.25	9.4	V	R177	5, 7
TG1 Transfer Gate CCD Clock	TG1C_CCD	Low		0.0		V		
		High	6.1	7.25	13.5	V	R128	5, 8
TG2 Transfer Gate CCD Clock	TG2_CCD	Low		0.0		V		
		High	6.1	7.25	13.5	V	R103	5
Reset Clock	RESET_CCD	Low		0.0		V		
		High	6.1	7.25	13.5	V	R74	5
Exposure Control Clock	LOGx_CCD	Low		0.0		V		
		High	6.1	7.25	13.5	V	R112	5
Test Pin − Input Diode	ID	Low	0.0	7.5	10.0	V	R173	5
		High	7.5	15.0	15.0	V	R166	9

5. The Min and Max voltages in the table indicate the imager board potentiometer adjustable voltage range. These values may exceed the specified CCD operating conditions. See the KLI−4104 device specification for details.
6. The H1LA_CCD, H1LB_CCD, H1CA_CCD, and H1CB_CCD high levels are controlled by the same potentiometer (R199).
7. The H2LA_CCD, H2LB_CCD, H2CA_CCD, and H2CB_CCD high levels are controlled by the same potentiometer (R177).
8. TG1 clock is used to drive TG1C only; TG1L is a fixed bias voltage. See Table 3.
9. For Test purposes only, the ID_HIGH voltage is adjustable up to 14.5 V; for normal operation, the ID_CCD signal is fixed at +15.0 V by populating R163 and removing R161 and R162.

Reset Clock Pulse Width

The pulse width of RESET_CCD is set by configuring P[2..0], the inputs to the programmable one−shot U46. P[2..0] can be tied high or low to achieve the desired pulse width by populating the resistors R188−191 accordingly.

Table 5. RESET CLOCK PULSE WIDTH

Pulse Width	P0	P1	P2	R188	R191	R189	R190	Notes
15 ns	0	0	0	IN	OUT	IN	OUT	
5 ns	1	0	0	OUT	IN	IN	OUT	Default Setting
7.5 ns	0	1	0	IN	OUT	OUT	IN	
10 ns	1	1	0	OUT	IN	OUT	IN	

ID Clock Pulse Width

The pulse width of ID_CCD is set by configuring P[2..0], the inputs to the programmable one−shot U49. P[2..0] can be tied high or low to achieve the desired pulse width by populating the resistors R193−196 accordingly. This circuit is provided for ON Semiconductor test purposes only.

Table 6. ID CLOCK PULSE WIDTH

Pulse Width	P0	P1	P2	R195	R193	R196	R194	Notes
15 ns	0	0	0	IN	OUT	IN	OUT	
5 ns	1	0	0	OUT	IN	IN	OUT	Default Setting
7.5 ns	0	1	0	IN	OUT	OUT	IN	
10 ns	1	1	0	OUT	IN	OUT	IN	

BLOCK DIAGRAM AND PERFORMANCE DATA

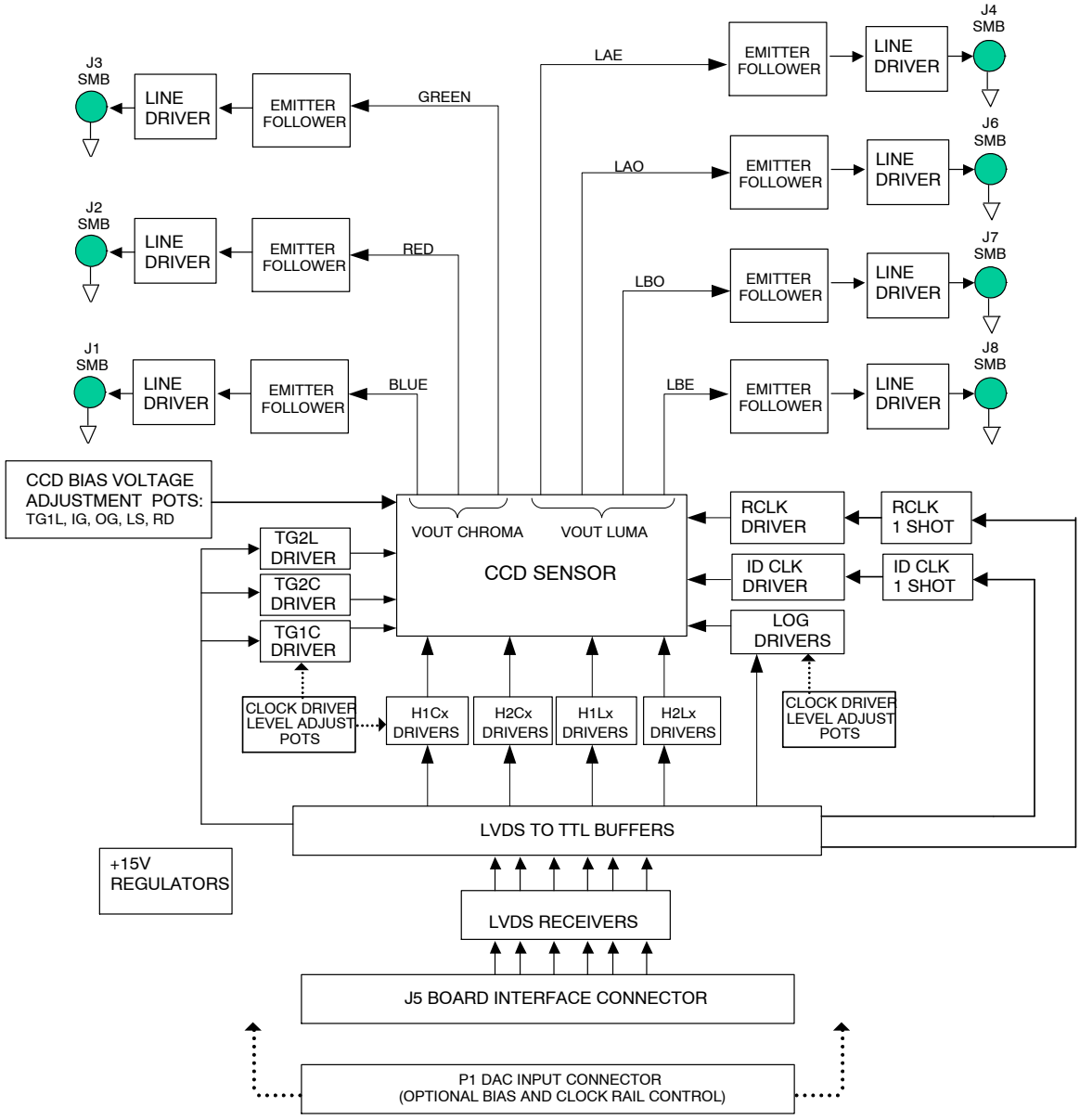

Figure 1. KLI−4104 Imager Board Block Diagram

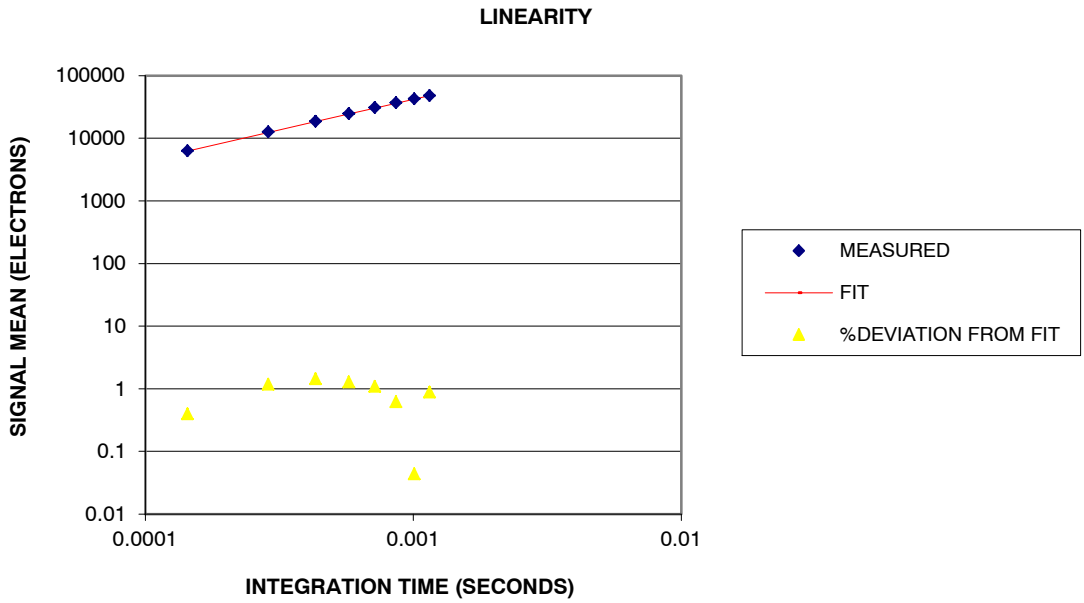

Figure 2. Measured Performance − Linearity (Luma Channel)

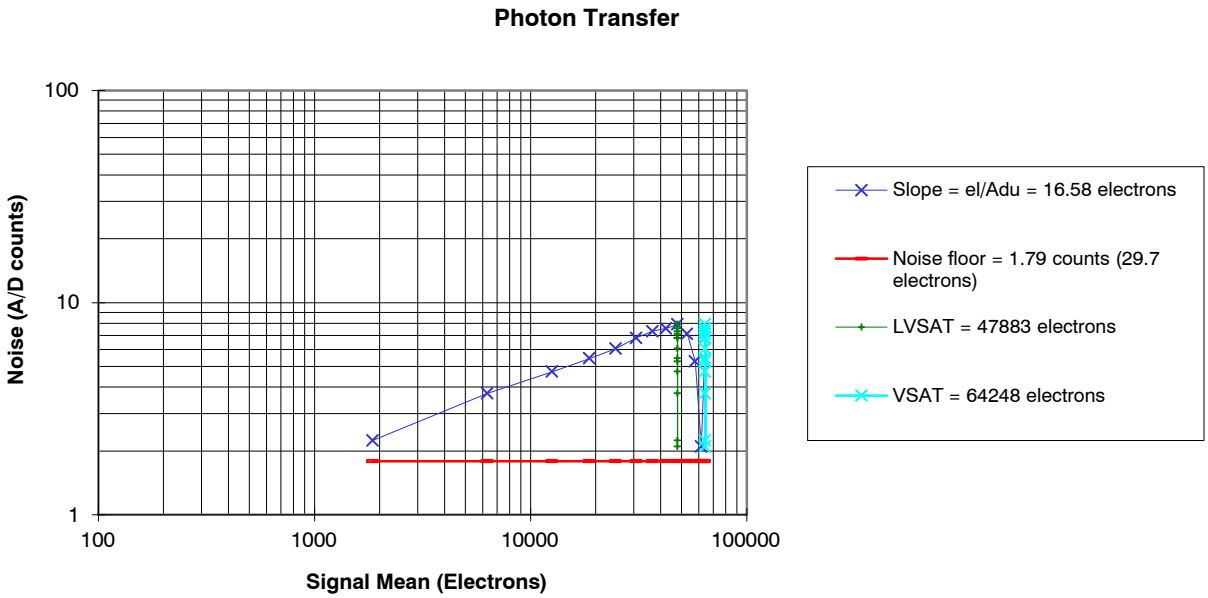

Figure 3. Measured Performance − Dynamic Range and Noise Floor (Luma Channel)

CONNECTOR ASSIGNMENTS AND PINOUTS

Video Out SMB Connectors

The emitter−follower buffered CCD_VOUT signals are driven from the Imager Board via the SMB connectors J1, J2, J3, J4, J6, J7, and J8. Coaxial cable with a characteristic impedance of 75 Ω should be used to connect the imager board to the Timing Generator Board to match the series and terminating resistors used on these boards.

Table 7. J5 INTERFACE CONNECTOR PIN ASSIGNMENTS

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	AGND	4	AGND
5	VES+	6	VES−
7	AGND	8	AGND
9	FDG+	10	FDG−
11	AGND	12	AGND
13	V3RD+	14	V3RD−
15	AGND	16	AGND
17	V2B+	18	V2B−
19	AGND	20	AGND
21	V2+	22	V2−
23	AGND	24	AGND
25	V1+	26	V1−
27	AGND	28	AGND
29	R+	30	R−
31	AGND	32	AGND
33	H2B+	34	H2B−
35	AGND	36	AGND
37	H2A+	38	H2A−
39	AGND	40	AGND
41	H1B+	42	H1B−
43	AGND	44	AGND
45	H1A+	46	H1A−
47	N.C.	48	N.C.
49	AGND	50	AGND
51	N.C.	52	N.C.
53	VMINUS_MTR	54	VMINUS_MTR
55	N.C.	56	N.C.
57	AGND	58	AGND
59	N.C.	60	N.C.
61	−5 V_MTR	62	−5 V_MTR
63	N.C.	64	N.C.
65	AGND	66	AGND
67	N.C.	68	N.C.
69	+5 V_MTR	70	+5 V_MTR
71	N.C.	72	N.C.
73	AGND	74	AGND
75	N.C.	76	N.C.
77	VPLUS_MTR	78	VPLUS_MTR
79	N.C.	80	N.C.

Warnings and Advisories

ON Semiconductor is not responsible for customer damage to the Imager Board or Imager Board electronics. The customer assumes responsibility and care must be taken when probing, modifying, or integrating the ON Semiconductor Evaluation Board Kits.

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of an Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, ON Semiconductor. Changes to the firmware are at the risk of the customer.

Ordering Information

Please address all inquiries and purchase orders to:

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