Ordering number : EN2770D

Discontinued

SANYO Semiconductors

DATA SHEET

LA5692D, 5692S LA5692M

Monolithic Linear IC

With Watchdog Timer Voltage Regulator Driver

Overview

The LA5692 is a single-chip voltage regulator for microcomputer system monitor use that performs the functions of 5V output voltage control, watchdog timer, and voltage detector. Since the LA5692 can hold the reset output, it is especially suited for use in peripheral control and monitor output applications (example : valves used in refrigeration equipment, hot water supply system).

Applications

- Microcomputer system for car equipment, refrigeration/heating equipment, office automation equipment.

Features

- An external PNP transistor can be used to provide a low saturation voltage regulator.
- CK input with edge detector.
- Variable detection voltage.
- The watchdog time can be made longer.

Functions

- Output voltage 5V control.
- Watchdog timer.
- Reset generation at power-ON mode.
- Reset hold output [RES (2)] (Cleared with CK re-input).

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61808 MS JK/D0597HA (KT)/8099YT/8037TA, TS No.2770-1/7

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Control pin voltage	V_{CONT} max	1s	60	V
Control pin voltage	V_{CONT} max		41	V
Control pin current	I_{CONT} max	$V_{CC} \geq 6V$ *	11	mA
CK input voltage	V_{CK} max		25	V
Reset pin voltage	$V_{\overline{RES}}$ (1) max, $V_{\overline{RES}}$ (2) max		41	V
Allowable power dissipation	Pd max	LA5692D, 5692S	500	mW
		LA5692M	370	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +150	°C

* : A PNP transistor is connected to the LA5692D, 5692S externally to provide a low-saturation voltage regulator.
Therefore, $I_{CONT} \approx 100mA$ will flow, as starting current, in the V_{CC} range where the output cannot be regulated.

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Control pin voltage	V_{CONT}		6 to 40	V
Control pin current	I_{CONT} max		10	mA
Reset output current	$I_{\overline{RES}}$ (1) max, $I_{\overline{RES}}$ (2) max	External R pull-up	8	mA
Reset detection voltage	V_S min		4	V

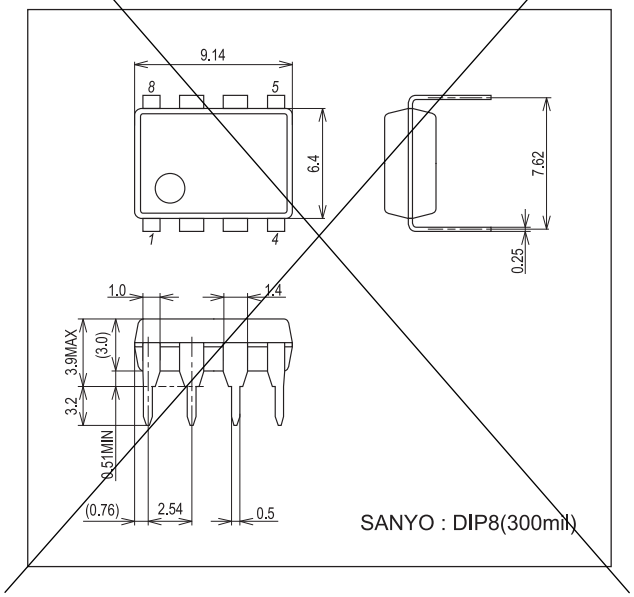
Electrical Characteristics at Ta = 25°C, V_{CC} = 14V, I_O = 50mA, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output voltage	V_O		4.8	5.0	5.2	V
Line regulation1	$\Delta V_{OLN}1$	$9V \leq V_{CC} \leq 16V$		2	10	mV
Line regulation2	$\Delta V_{OLN}2$	$6V \leq V_{CC} \leq 40V$		4	30	mV
Load regulation	ΔV_{OLD}	$1mA \leq I_O \leq 50mA$		4	30	mV
Current dissipation	I_{CC}	$I_O = 0$		4.4	6.5	mA
Output noise voltage	V_{NO}	$10Hz \leq f \leq 100kHz$, $V_{CK} = 0$		150		µV
Temperature coefficient of output voltage	$\Delta V_O/\Delta Ta$	I_O = 5mA, –40°C ≤ Ta ≤ +85°C		±0.2		mV/°C
Reference voltage	V_{REF}		1.13	1.18	1.23	V
'H'-level CK input voltage	V_{IH}		2			V
'L'-level CK input voltage	V_{IL}				0.8	V
'H'-level CK input current	I_{IH}	V_{CK} = 5V		0.3	0.7	mA
'L'-level CK input current	I_{IL}	V_{CK} = 0V	–1.0	–0.1		µA
'H'-level reset output voltage	$V_{\overline{ORH}}$ (1) $V_{\overline{ORH}}$ (2)	$\overline{RES}$ (2) : 10KΩ pull-up	4.8	5.0	5.2	V
'L'-level reset output voltage1	$V_{\overline{ORL}}$ (1) 1 $V_{\overline{ORL}}$ (2) 1	$\overline{RES}$ (2) : 10KΩ pull-up		40	200	mV
'L'-level reset output voltage2	$V_{\overline{ORL}}$ (1) 2 $V_{\overline{ORL}}$ (2) 2	$I_{\overline{RES}}$ (1) = I_{RES} (2) = 8mA		0.16	0.8	V
CK input pulse width	t_{CKW}	V_{CK} = 5V	3			µs
Reset output delay time	t_d	C_t = 1µF	7.5	10	12.5	ms
Watchdog time	t_{WD}	C_t = 1µF	30	40	50	ms
Watchdog reset time	t_{WR}	C_t = 1µF	0.1	0.25	0.4	ms
Reset hysteresis voltage	V_{hys}	V_S = 4.5V	100	200	300	mV

Package Dimensions

unit : mm (typ)

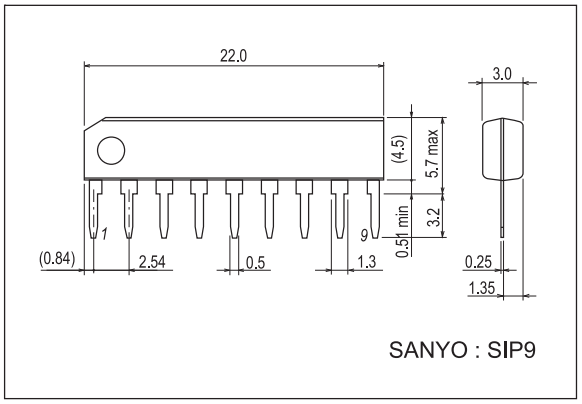
3001D [LA5692D]



Package Dimensions

unit : mm (typ)

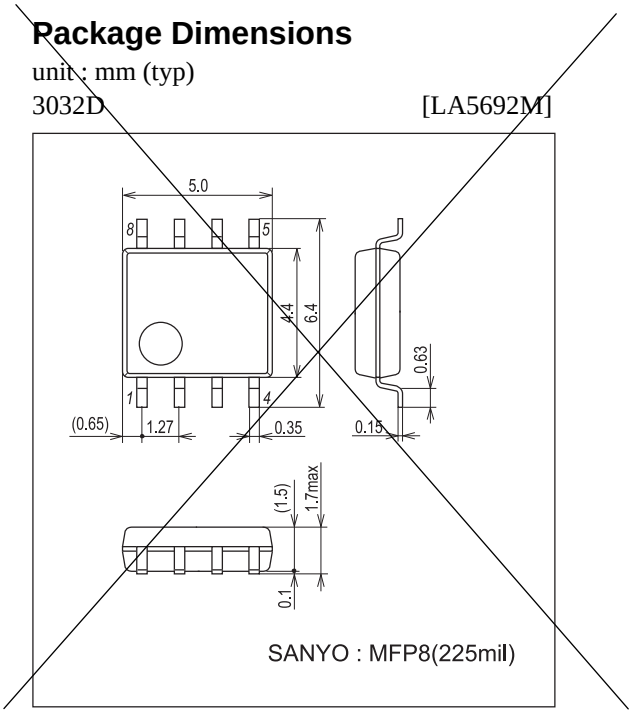
3017D [LA5692S]



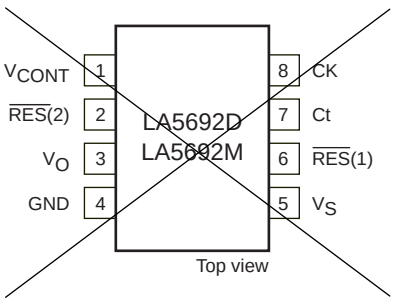
Package Dimensions

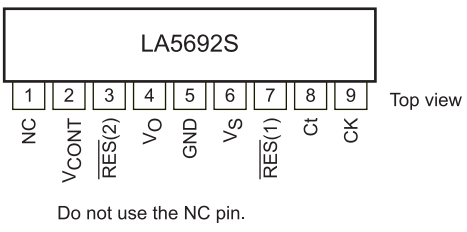
unit : mm (typ)

3032D [LA5692M]



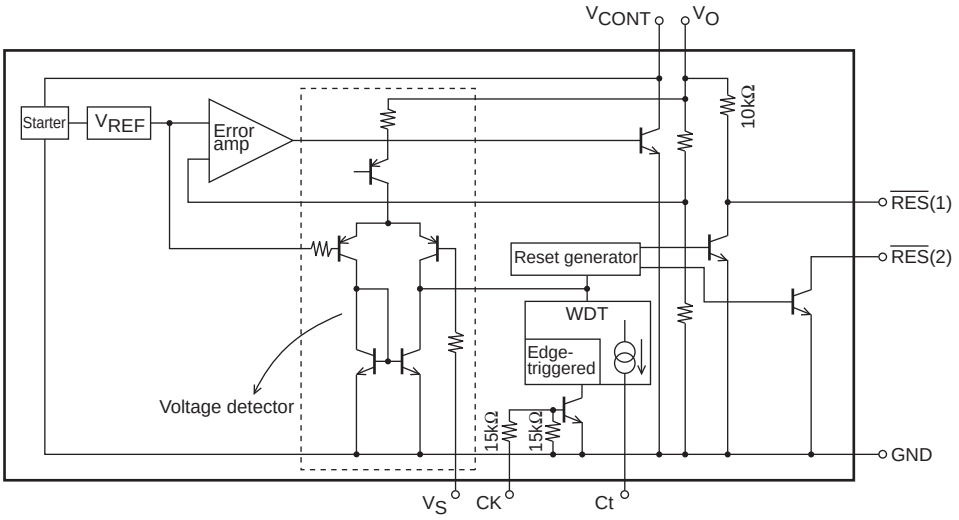
Pin Assignment





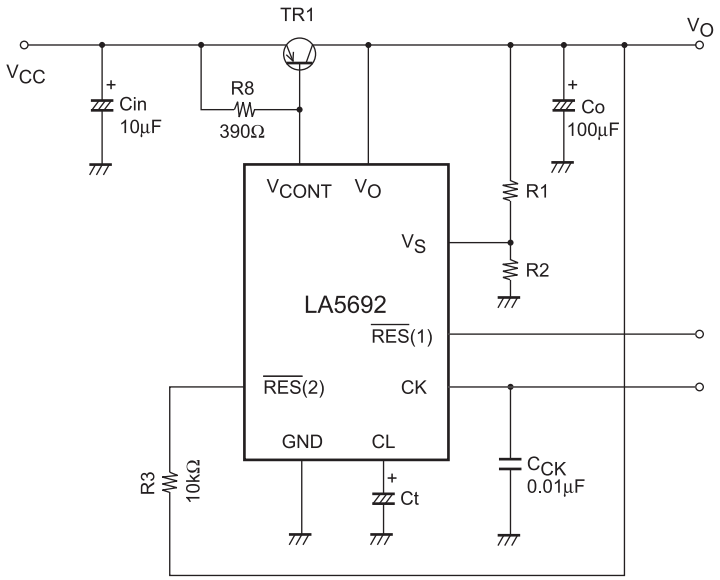
Do not use the NC pin.

Block Diagram

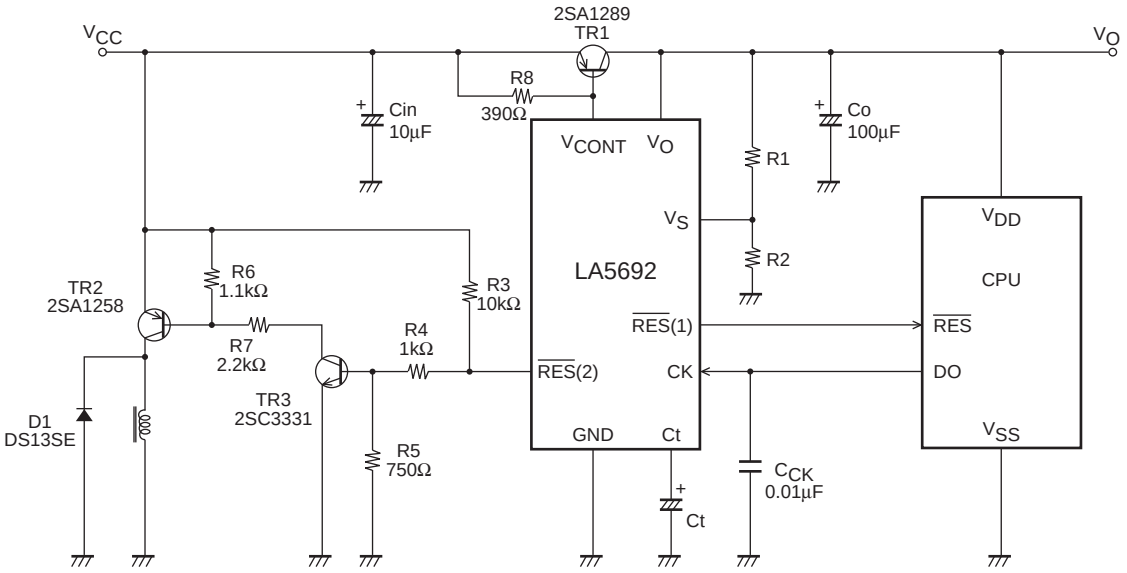


* $\overline{\text{RES}}$(1) : Contains a pull-up resistor of 10kΩ.
$\overline{\text{RES}}$(2) : Open collector

Test Circuit



Sample Application Circuit



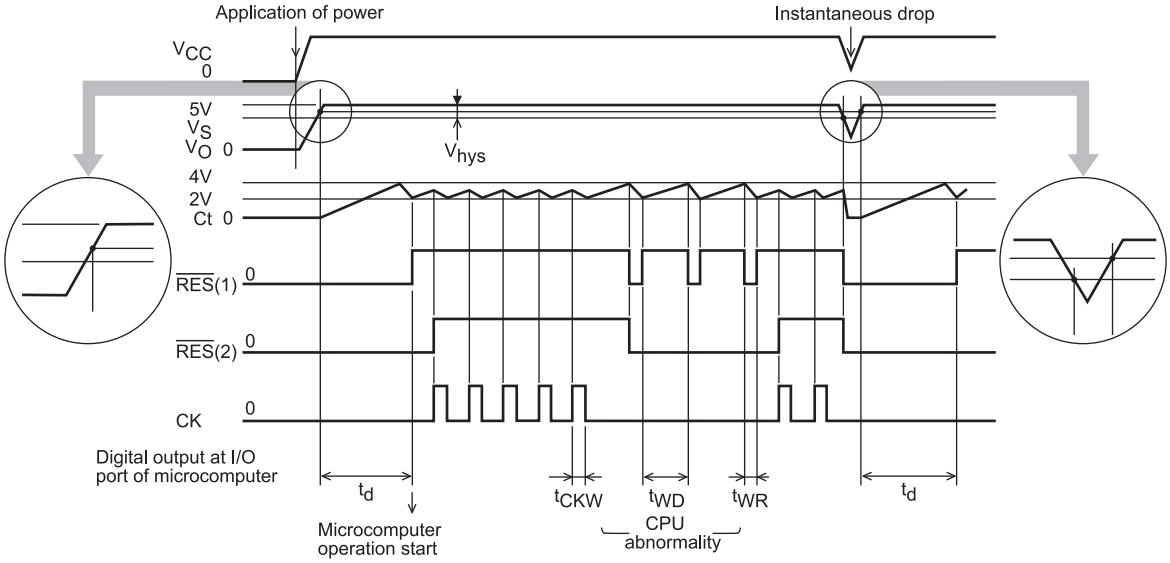
$$V_S = V_{REF} \times \left(\frac{R1}{R2} + 1\right)$$
$$V_{REF} \approx 1.18\ [V]$$

$$t_d = 10 \times Ct\ (\mu F)\quad [ms]$$
$$t_{WD} = 40 \times Ct\ (\mu F)\quad [ms]$$
$$t_{WR} = 0.25 \times Ct\ (\mu F)\quad [ms]$$

Note on application

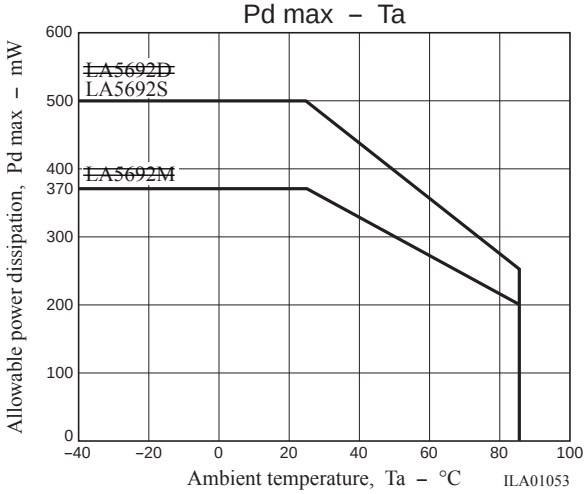
1. For stable operation, place C_{in}, C_O, and TR1 as near to the IC as possible.
2. When used in 0°C or below it, a capacitor of which impedance at high-frequency operation is low and has a good temperature characteristic (such as SANYO OS-CON capacitor or others) should be used to prevent oscillation.
3. Set V_S to the output voltage level where the circuit will be reset using external resistors R1 and R2. V_S should be set to 4V or greater due to internal circuit operation.
4. C_{CK} must be inserted to cut the high range element of clock noise to prevent it from becoming a reset output noise.
5. For Ct, a capacitor which less varies the capacitance according to the temperature should be used.

Timing Chart

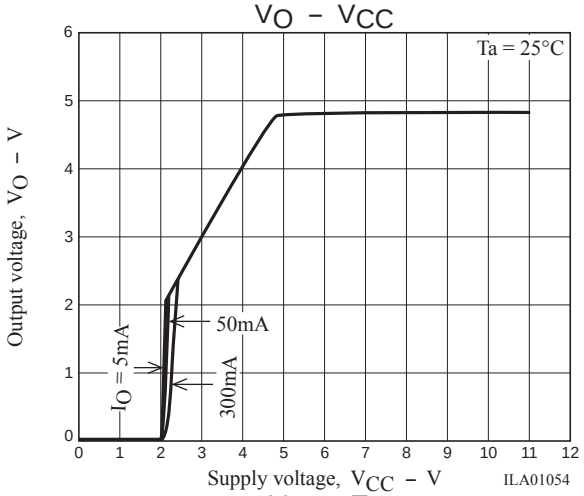


Note : Edge-triggered at the point indicated by the arrow of C_K signal.

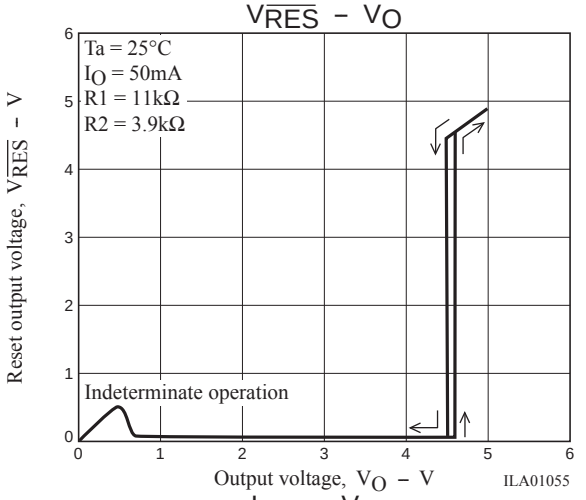
Pd max – Ta



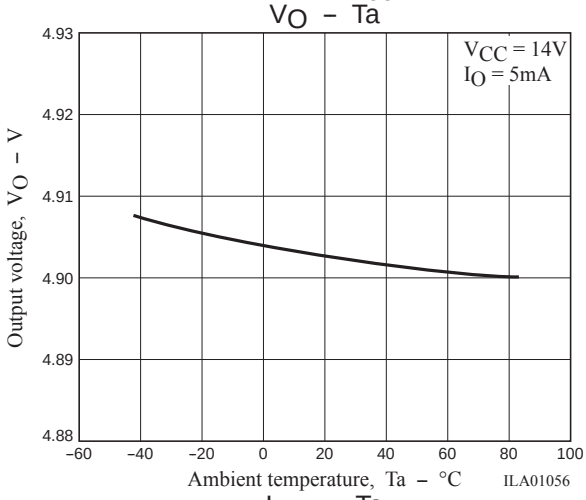
V_O – V_{CC}



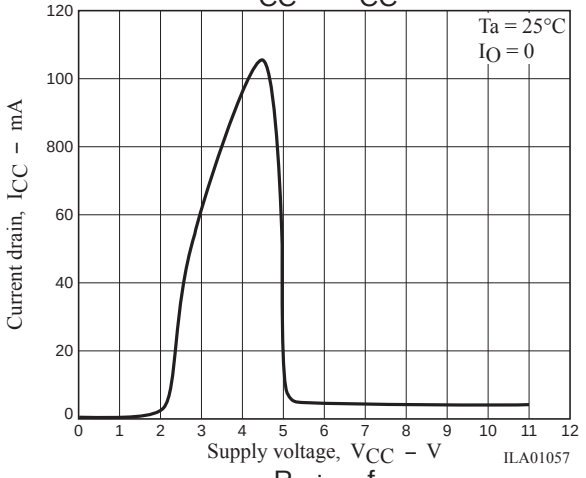
$V\overline{RES}$ – V_O



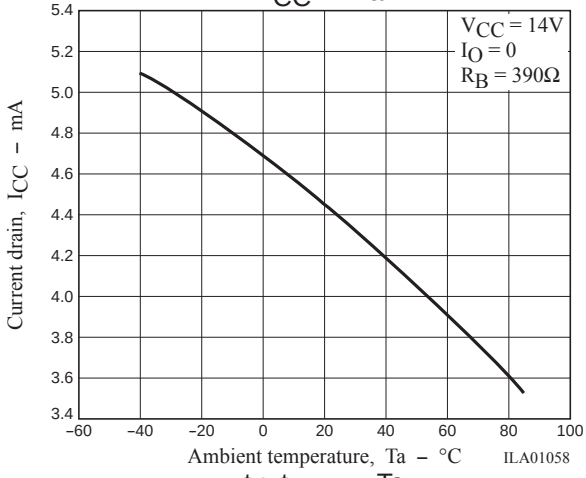
V_O – Ta



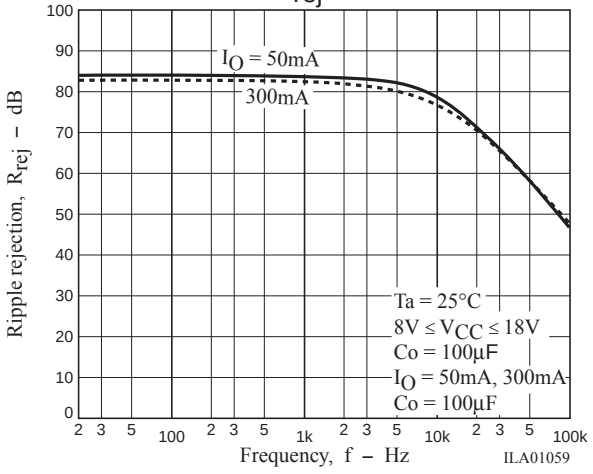
I_{CC} – V_{CC}



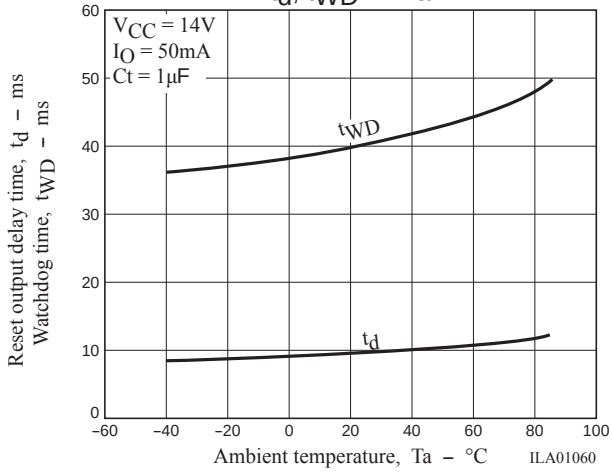
I_{CC} – Ta

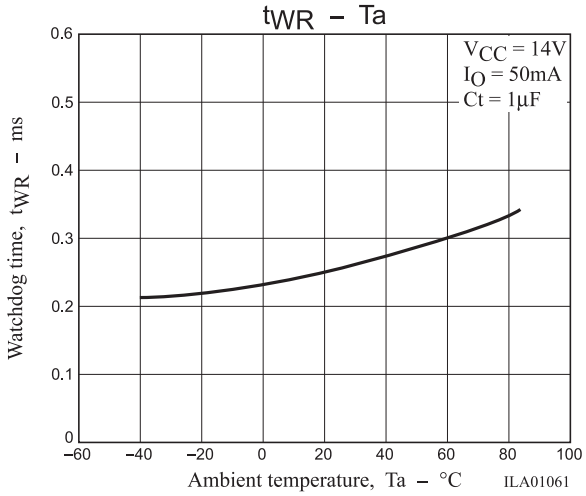


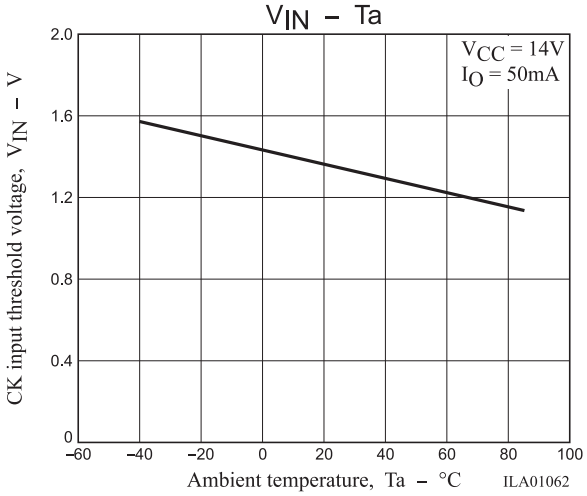
R_{rej} – f

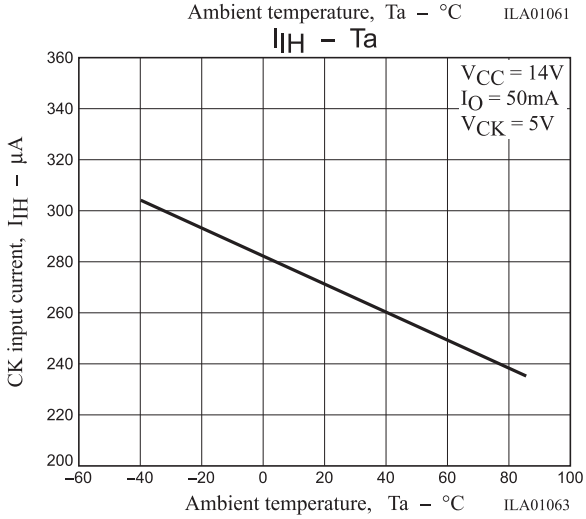


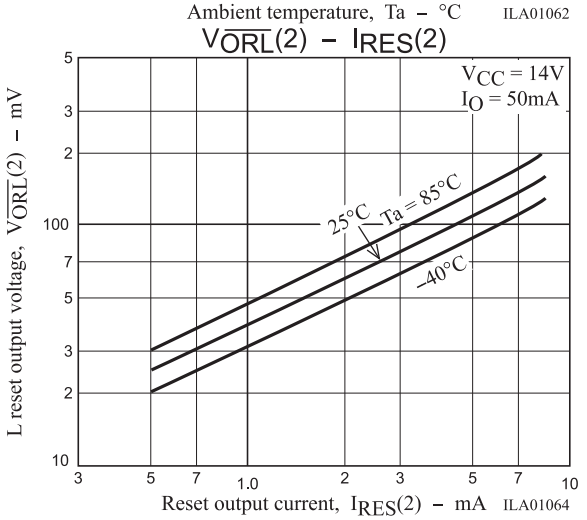
t_d, t_{WD} – Ta











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