Ordering number : EN7109A

LB11826

Monolithic Digital IC

For OA Products

Three-Phase Brushless Motor Driver

ON Semiconductor®

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Overview

The LB11826 is a three-phase brushless motor driver that is optimal for driving drum and paper feed motors in laser printers and plain paper copiers. This IC adopts a direct PWM drive technique for minimal power loss. Flexible control of motor speed in response to an externally provided clock frequency (corresponding to the FG frequency) can be implemented by using the LB11826 in conjunction with the Sanyo LB11825M.

Features

- Three-phase bipolar drive (30V, 2.5V)
- Direct PWM drive
- Built-in low side inductive kickback absorbing diode
- Speed discriminator + PLL speed control
- Speed locked state detection output
- Built-in forward/reverse switching circuit
- Full complement of built-in protection circuits, including current limiter circuit, thermal protection circuit, and motor constraint protection circuit.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		30	V
Output current	I_O max	T ≤ 500ms	2.5	A
Allowable power dissipation	Pd max1	Independent IC	3	W
	Pd max2	When infinitely large heat sink	20	W
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1	V_{CC}		9.5 to 28	V
Voltage output current	IREG		0 to -30	mA
LDn output current	ILD		0 to 15	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = VM = 24V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	$I_{CC}1$			23	30	mA
Supply current 2	$I_{CC}2$	Stop mode		3.5	5	mA
Output block						
Output saturation voltage 1	V_O sat1	I_O = 1.0A, V_O (sink) + (source)		2.0	2.5	V
Output saturation voltage 2	V_O sat2	I_O = 2.0A, V_O (sink) + (source)		2.6	3.2	V
Output leakage current	I_O leak				100	μA
Lower side diode forward voltage 1	VD1	ID = -1.0A		1.2	1.5	V
Lower side diode forward voltage 2	VD2	ID = -2.0A		1.5	2.0	V
5V Voltage output						
Output voltage	VREG	I_O = -5mA	4.65	5.00	5.35	V
Voltage regulation	ΔVREG1	V_{CC} = 9.5 to 28V		30	100	mV
Load regulation	ΔVREG2	I_O = -5 to -20mA		20	100	mV
Hall Amplifier						
Input bias current	IHB		-2	-0.5		μA
Common-mode input voltage range	VICM		1.5		VREG-1.5	V
Hall input sensitivity			80			mVp-p
Hysteresis width	ΔV_{IN}		15	24	42	mV
Input voltage low → high	VSLH			12		mV
Input voltage high → low	VSHL			-12		mV
PWM oscillator circuit						
Output H level voltage	V_{OH} (PWM)		2.5	2.8	3.1	V
Output L level voltage	V_{OL} (PWM)		1.2	1.5	1.8	V
Oscillator frequency	f (PWM)	C = 3900pF		18		kHz
Amplitude	V (PWM)		1.05	1.30	1.55	Vp-p
CSD circuit						
Operating voltage	V_{OH} (CSD)		3.6	3.9	4.2	V
External C charge current	ICHG		-17	-12	-9	μA
Operating time	T (CSD)	C = 10μF, Design target value*		3.3		s
Current limiter operation						
Limiter	VRF	V_{CC}-VM	0.45	0.5	0.55	V
Thermal shutdown operation						
Thermal shutdown operating temperature	TSD	Design target value* (junction temperature)	150	180		°C
Hysteresis width	ΔTSD	Design target value* (junction temperature)		50		°C
FG amplifier						
Input offset voltage	V_{IO} (FG)		-10		10	mV
Input bias current	IB (FG)		-1		1	μA
Output H level voltage	V_{OH} (FG)	IFGO = -0.2mA	VREG-1.2	VREG-0.8		V
Output L level voltage	V_{OL} (FG)	IFGO = 0.2mA		0.8	1.2	V
FG input sensitivity		Gain 100-fold	3			mV
Schmitt amplitude for the next stage		Design target value*	100	180	250	mV
Operation frequency range					2	kHz
Open-loop gain		f (FG) = 2kHz	45	51		dB

Note : * These items are design target values and are not tested.

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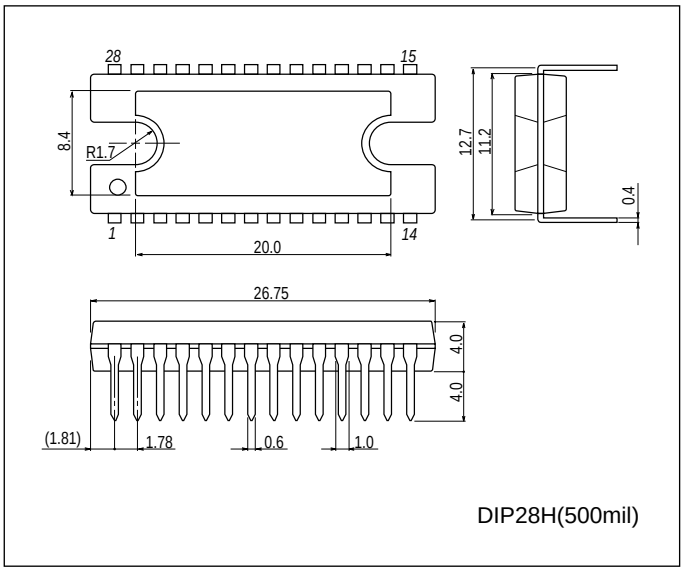
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Speed discriminator						
Output H level voltage	V_{OH} (D)	IDO = -0.1mA	VREG-1.0	VREG-0.7		V
Output L level voltage	V_{OL} (D)	IDO = 0.1mA		0.8	1.1	V
Number of counts				512		
PLL output						
Output H level voltage	V_{OH} (P)	IPO = -0.1mA	VREG-1.8	VREG-1.5	VREG-1.2	V
Output L level voltage	V_{OL} (P)	IDO = 0.1mA	1.2	1.5	1.8	V
Lock detection						
Output L level voltage	V_{OL} (LD)	ILD = 10mA		0.15	0.5	V
Lock range				6.25		%
Integrator						
Input bias current	IB (INT)		-0.4		0.4	µA
Output H level voltage	V_{OH} (INT)	IINTO = -0.2mA	VREG-1.2	VREG-0.8		V
Output L level voltage	V_{OL} (INT)	IINTO = 0.2mA		0.8	1.2	V
Open-loop gain		f (INT) = 1kHz	45	51		dB
Gain width product		Design target value*		450		kHz
Reference voltage		Design target value*	-5%	VREG/2	5%	V
Clock input pin						
Operating frequency range	f_{OSC}				1	MHz
L level pin voltage	V_{OSCL}	I_{OSC} = -0.5mA		1.55		V
H level pin current	I_{OSCH}	$V_{OSC} = V_{OSCL}$ + 0.5V		0.4		mA
Start/Stop pin						
H level input voltage range	V_{IH} (S/S)		3.5		VREG	V
L level input voltage range	V_{IL} (S/S)		0		1.5	V
Input open voltage	V_{IO} (S/S)		VREG-0.5		VREG	V
Hysteresis width	ΔV_{IN}		0.35	0.50	0.65	V
H level input current	I_{IH} (S/S)	V (S/S) = VREG	-10	0	10	µA
L level input current	I_{IL}(S/S)	V (S/S) = 0V	-280	-210		µA
Forward/Reverse pin						
H level input voltage range	V_{IH} (F/R)		3.5		VREG	V
L level input voltage range	V_{IL} (F/R)		0		1.5	V
Input open voltage	V_{IO} (F/R)		VREG-0.5		VREG	V
Hysteresis width	ΔV_{IN}		0.35	0.50	0.65	V
H level input current	I_{IH} (F/R)	V (F/R) = VREG	-10	0	10	µA
L level input current	I_{IL}(F/R)	V (F/R) = 0V	-280	-210		µA

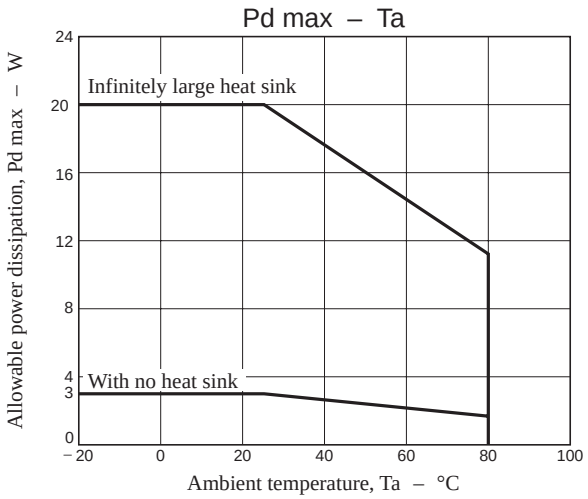
Note : * These items are design target values and are not tested.

Package Dimensions

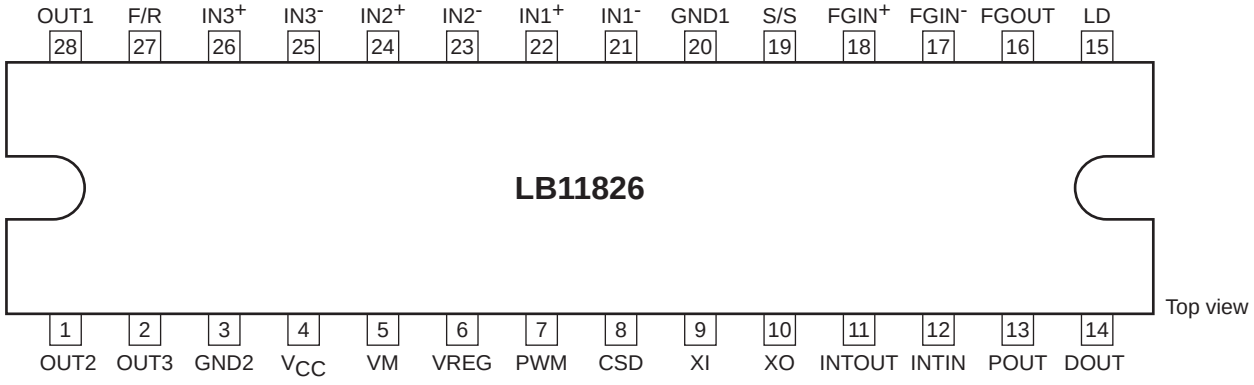
unit : mm (typ)

3174C





Pin Assignment



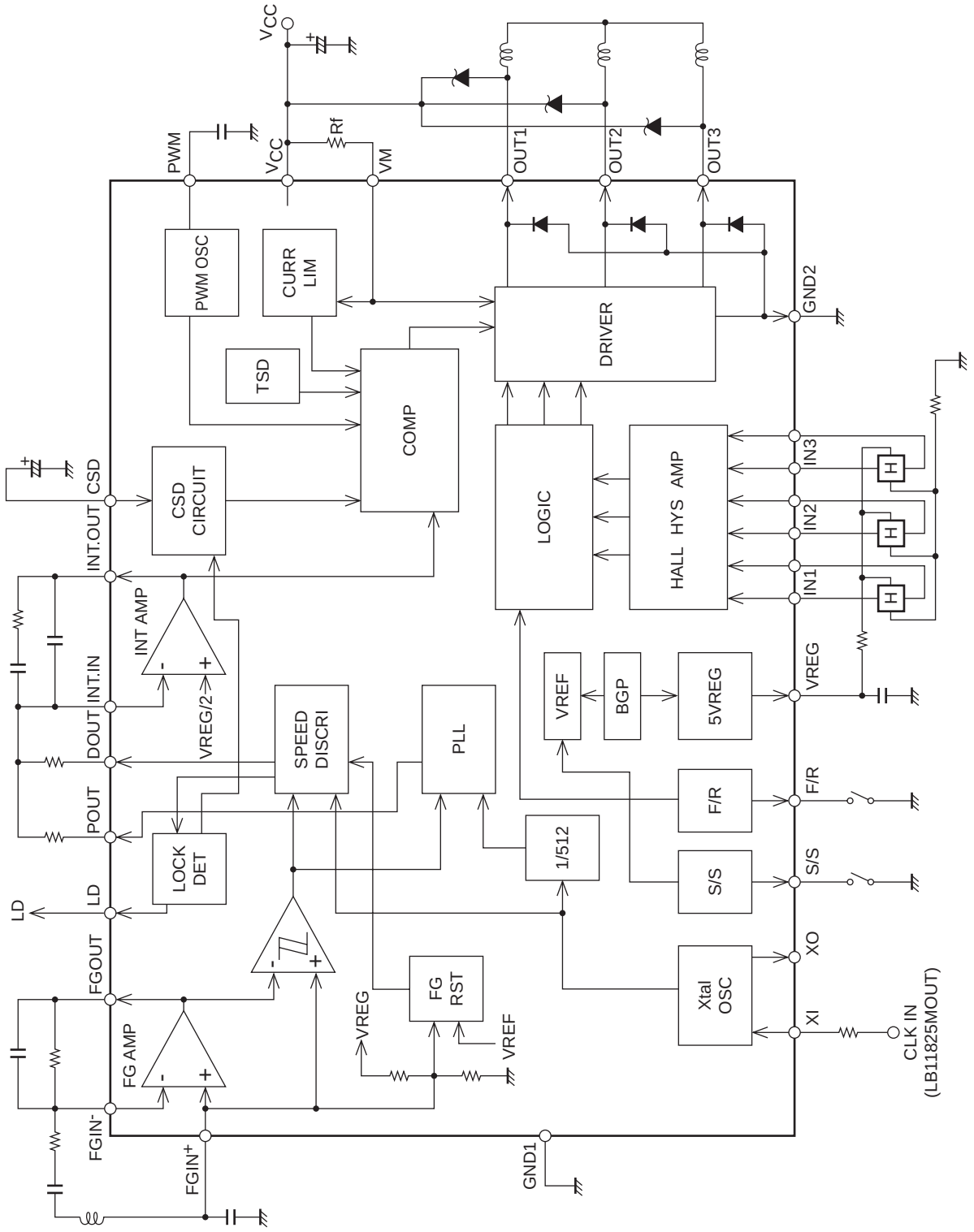
Truth Table

	Source / Sink	F/R= L			F/R= H		
		IN1	IN2	IN3	IN1	IN2	IN3
1	OUT2 → OUT1	H	L	H	L	H	L
2	OUT3 →OUT1	H	L	L	L	H	H
3	OUT3 → OUT2	H	H	L	L	L	H
4	OUT1 → OUT2	L	H	L	H	L	H
5	OUT1 → OUT3	L	H	H	H	L	L
6	OUT2 → OUT3	L	L	H	H	H	L

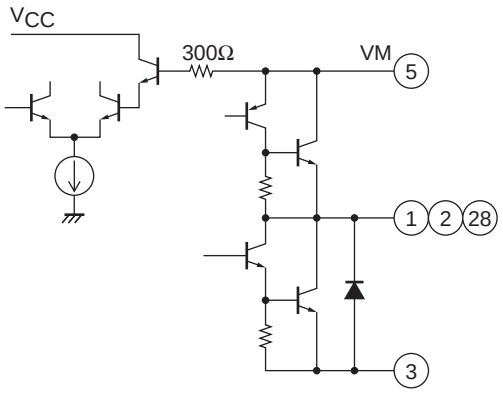
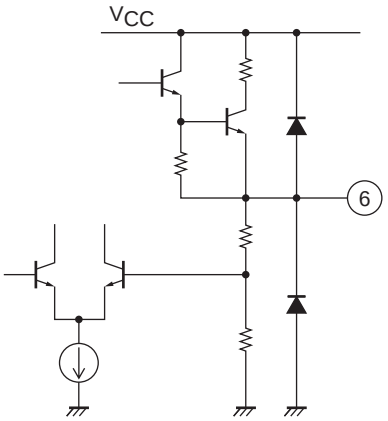
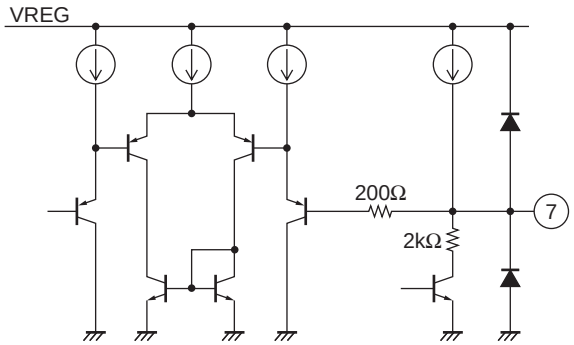
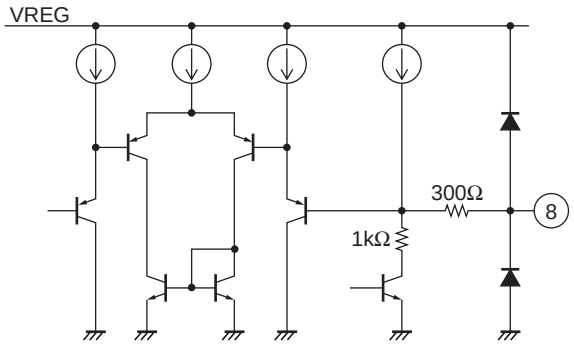
The relation between the clock frequency, f_{CLK}, and the FG frequency, f_{FG}, is given by the following equation.

f_{FG} (servo) = f_{CLK}/<number of counts>
= f_{CLK}/512

Block Diagram and Peripheral Circuits



Pin Functions

Pin No.	Pin name	Pin function	Equivalent circuit
28 1 2	OUT1 OUT2 OUT2	Motor drive output pin. Connect the Schottky diode between the output - V_{CC}.	
3	GND2	Output GND pin.	
5	VM	Power and output current detection pins of the output. Connect a low resistance (Rf) between this pin and V_{CC}. The output current is limited to the current value set with $I_{OUT} = V_{RF}/Rf$.	
4	V_{CC}	Power pin (Other than the output).	
6	VREG	Stabilized power supply output pin (5V output). Connect a capacitor (about 0.1μF) between this pin and GND for stabilization.	
7	PWM	Pin to set the PWM oscillation frequency. Connect a capacitor between this pin and GND. This can be set to about 18kHz with C = 3900pF.	
8	CSD	Pin to set the operation time of motor lock protection circuit. Connection of a capacitor (about 10μF) between CSD and GND can set the protection operation time of about 3.3seconds.	

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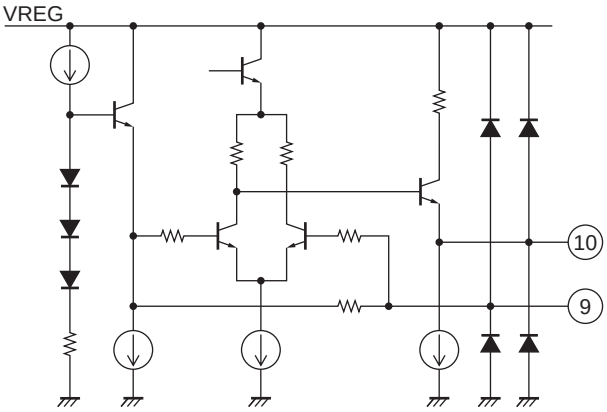
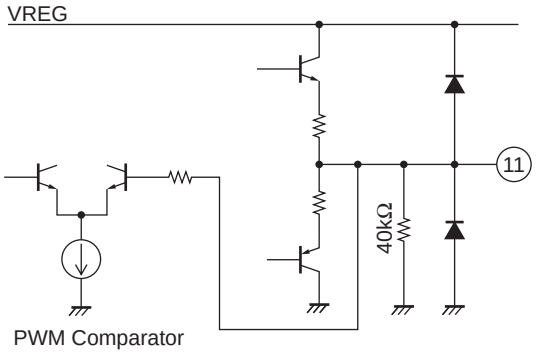
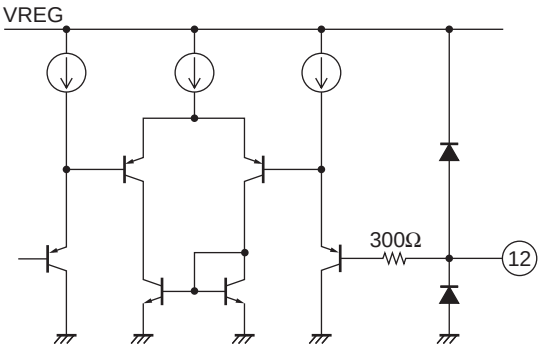
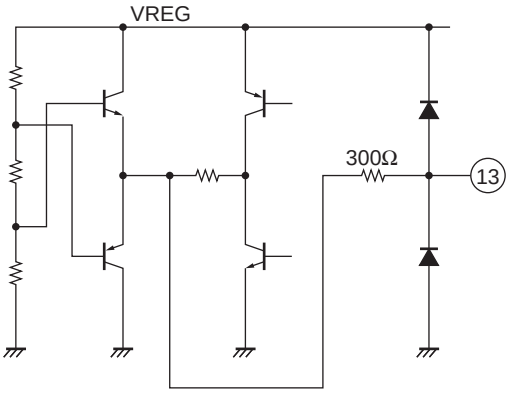
Pin No.	Pin name	Pin function	Equivalent circuit
9 10	XI XO	Clock input pin, which enters the clock signal (1MHz or less) to the XI pin via resistor (about 5.1kΩ). Keep the XO pin open.	
11	INTOUT	Integrating amplifier output (speed control pin).	
12	INTIN	Integrating amplifier input pin.	
13	POUT	PLL output pin.	

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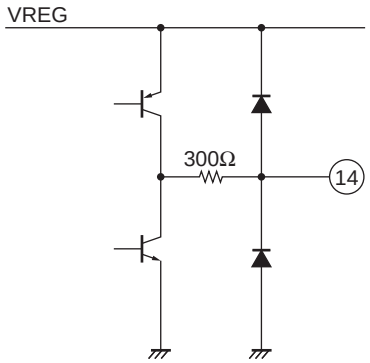
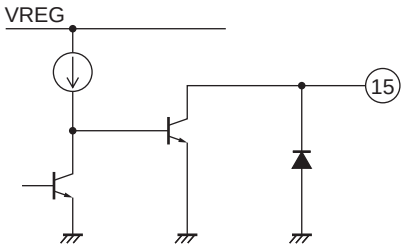
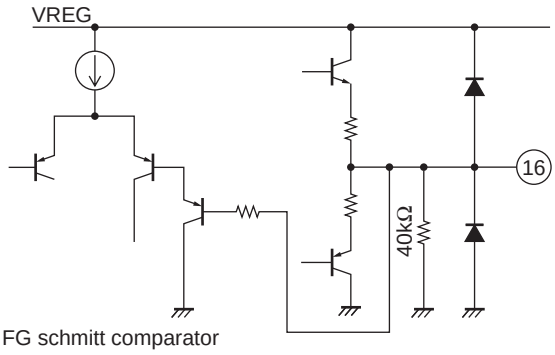
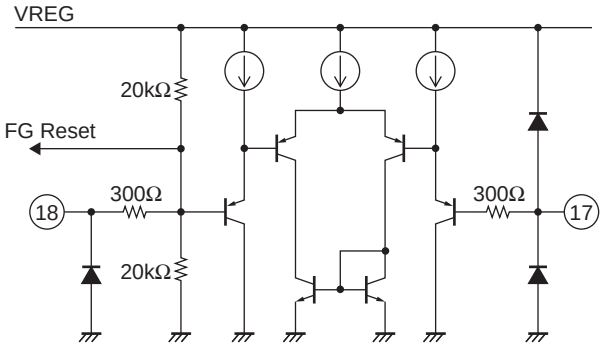
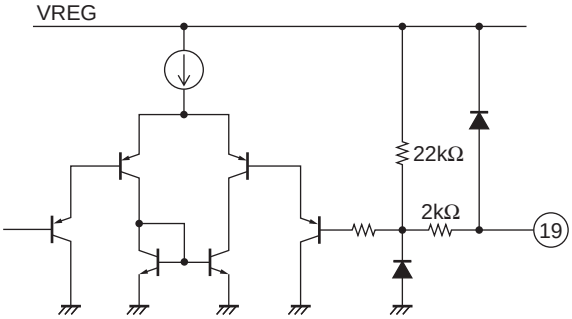
Pin No.	Pin name	Pin function	Equivalent circuit
14	DOUT	Speed discriminator output. Accelerate : high, decelerate : low.	
15	LD	Speed lock detection output. L when the motor speed is within the speed lock range (±6.25%). Voltage resistance 30V max.	
16	FGOUT	FG amplifier output pin.	
17 18	$FGIN^-$ $FGIN^+$	FG amplifier input pin. Connection of a capacitor (about 0.1µF) between FGIN and GND causes initial reset to the logic circuit.	
19	S/S	Start/stop control pin. Low : 0V to 1.5V High : 3.5V to VREG H level when open. Hysteresis width about 0.5V.	
20	GND1	GND pin (Other than the output).	

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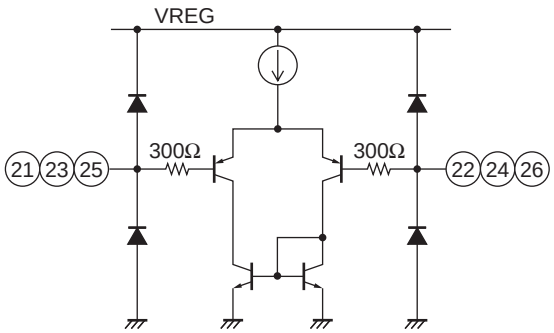
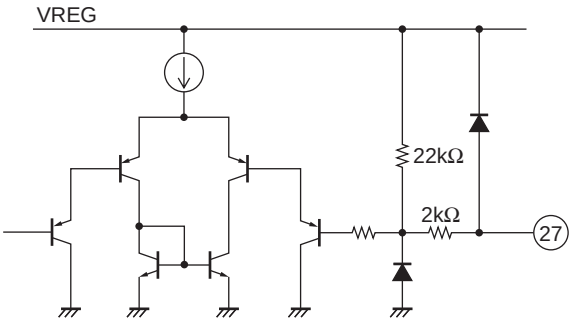
Pin No.	Pin name	Pin function	Equivalent circuit
22 21 24 23 26 25	$IN1^+$ $IN1^-$ $IN2^+$ $IN2^-$ $IN3^+$ $IN3^-$	Hall amplifier input. $IN^+ > IN^-$ is the input high state, and the reverse is the input low state. It is recommended that the Hall signal has an amplitude of 100mVp-p (differential) or more. Connect a capacitor between the IN^+ and IN^- inputs if there is noise in the Hall sensor signals.	
27	F/R	Forward/reverse control pin. Low : 0V to 1.5V High : 3.5V to VREG H level when open. Hysteresis width about 0.5V.	

LB11826 Description

1. Speed control circuit

This IC performs speed control by using both the speed discriminator circuit and PLL circuit. The speed control circuit outputs the error signal once for every two cycles of FG (one FG cycle counted). The PLL circuit outputs the phase error signal once for each cycle of FG.

As the FG servo frequency is calculated as follows, the motor speed is set with the number of FG pulses and clock frequency.

f_{FG} (servo) = $f_{CLK}/512$

f_{CLK} : Clock frequency

This IC achieves variable speed control with ease when combined with LB11825M.

2. Output drive circuit

This IC employs a direct PWM drive method to minimize the power loss at output. The output Tr is always saturated at ON, and the motor drive force is adjusted through change of the duty at which the output is turned ON. Since the output PWM switching is made with the lower-side output Tr, it is necessary to connect the schottky diode between OUT and V_{CC} (because the through current flows at an instant when the lower-side Tr is turned ON if the diode with a short reverse recovery time is not used). The diode between OUT and GND is incorporated. When the large output current presents problem (waveform disturbance at kickback on the lower side), connect a commutating diode or schottky diode externally.

3. Current limiting circuit

The current limiting circuit performs limiting with the current determined from $I = V_{RF}/Rf$ (V_{RF} = 0.5Vtyp, Rf : current detector resistance) (that is, this circuit limits the peak current).

Limiting operation includes decrease in the output on-duty to suppress the current.

4. Power save circuit

This IC enters the power save condition to decrease the current dissipation in the stop mode. In this condition, the bias current of most of circuits is cut off. Even in the power save condition, the 5 V regulator output is given.

5. Reference clock

This is entered from the external signal source (1MHz max) via a resistor (reference : about 5.1kΩ) in series with the XI pin. The XO pin is left open.

Input signal source levels :

Low-level voltage : 0 to 0.8V

High-level voltage : 2.5 to 5.0V

6. Speed lock range

The speed lock range is ±6.25% of the constant speed. If the motor speed falls inside the lock range, the LD pin goes to "L" (open collector output). When the motor speed falls outside the lock range, the on-duty ratio of motor drive output changes according to the speed error, causing control to keep the motor speed within the lock range.

7. PWM frequency

PWM frequency is determined from the capacity C (F) of capacitor connected to the PWM pin.

$$f_{PWM} \approx 1/ (14{,}400 \times C)$$

It is recommended to keep the PWM frequency at 15k - 20kHz.

8. Hall input signal

The Hall input requires the signal input with an amplitude exceeding the hysteresis width (42mV max). Considering the effect of noise, the input with the amplitude of 100mV or more is recommended.

9. F/R changeover

Motor rotation direction can be changed over with the F/R pin. When changing F/R while the motor is running, pay attention to following points.

- For the through current at a time of changeover, the countermeasure is taken using a circuit. However, it is necessary to prevent exceeding of the rated voltage (30V) due to rise of V_{CC} voltage at a time of changeover (because the motor current returns instantaneously to the power supply). When this problem exists, increase the capacity of a capacitor between V_{CC} and GND.
- When the motor current exceeds the current limit value after changeover, the lower-side Tr is turned OFF. But, the upper-side Tr enters the short-brake condition and the current determined from the motor counter electromotive voltage and coil resistance flows. It is necessary to prevent this current from exceeding the rated current (2.5A). (F/R changeover at high motor speed is dangerous.)

10. Motor lock protection circuit

A motor lock protection circuit is incorporated for protection of IC and motor when the motor is locked.
When the LD output is "H" (unlocked) for a certain period in the start condition, the lower-side Tr is turned OFF. This time is set with the capacity of the capacitor connected to the CSD pin. The time can be set to about 3.3 seconds with the capacity of 10μF (variance about ±30%).

$$\text{Set time (s)} \approx 0.33 \times C\ (\mu F)$$

When the capacitor used has a leak current, due consideration is necessary because it may cause error in the set time, etc.
Cancelling requires either the stop condition or re-application of power supply (in the stop condition). When the lock protection circuit is not to be used, connect the CSD pin to GND.
When the stop period during which lock protection is to be cancelled is short, the charge of capacitor cannot be discharged completely and the lock protection activation time at restart becomes shorter than the set value. It is necessary to provide the stop time with an allowance while referring to the following equation. (The same applies to restart in the motor start transient condition.)

$$\text{Stop time (ms)} \geq 15 \times C\ (\mu F)$$

11. Power supply stabilization

This IC has a large output current and is driven by switching, resulting in ready oscillation of the power line. It is therefore necessary to connect a capacitor with a sufficient capacity between the V_{CC} pin and GND for stabilization. When a diode is inserted in the power line to prevent breakdown due to reverse connection of power supply, the power line is particularly readily oscillated. The larger capacity need be selected.

12. Constant of integrating amplifier parts

Arrange the integrating amplifier external parts as near as possible to IC to protect them from noise effects. Arrange them by keeping the largest possible distance from the motor.

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