LB11868V

Variable Speed Single-phase Full-wave Pre-driver for Fan Motor

Monolithic Digital IC

Overview

LB11868V is a single-phase bipolar driving motor pre-driver with the variable speed function compatible with external PWM signal. With a few external parts, a highly-efficient and highly-silent variable drive fan motor with low power consumption can be achieved. This product is best suited for driving of the server requiring large air flow and large current and the fan motor of consumer appliances.

Functions and Features

- Single-phase Full-wave Driving Pre-driver
- Variable Speed Control Possible with External PWM Input
- Current Limiting Circuit Incorporated
- Reactive Current Cut Circuit Incorporated
- Minimum Speed Setting Pin
- Soft Start Setting Pin
- Start Setting Pin of On Time
- Pch-FET Kickback Absorption Setting Pin
- Lock Protection and Automatic Reset Circuits Incorporated
- FG (Rotational Speed Detection) Output, RD (Lock Detection) Output
- Thermal Shutdown Circuit Incorporated

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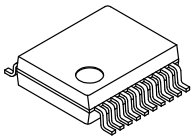

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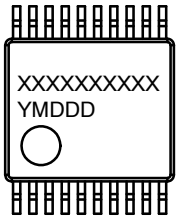
MARKING DIAGRAM



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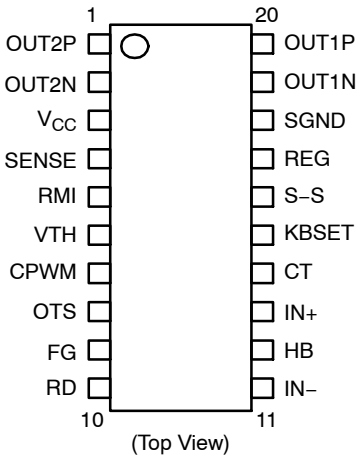
PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC} max	V_{CC} Pin Maximum Supply Voltage		18	V
I_{OUT}N max	OUTN Pin Maximum Current		30	mA
V_{OUT}N max	OUTN Pin Output Withstand Voltage		18	V
I_{OUT}P max	OUTP Pin Maximum Sink Current		30	mA
I_{OUT}P off max	Maximum Inflow Current at OUTP Pin OFF	DUTY 8% under	10	mA
V_{OUT}P max	OUTP Pin Output Withstand Voltage	(Note 1)	19	V
VVTH/ VRMI max	VTH/RMI Pins Withstand Voltage		7	V
V_{S-S} max	S−S Pin Withstand Voltage		7	V
V_{OTS} max	OTS Pin Withstand Voltage		7	V
V_{KBSET} max	KBSET Pin Withstand Voltage		7	V
$V_{FG/RD}$ max	FG/RD Pin Withstand Voltage		19	V
$I_{FG/RD}$ max	FG/RD Pin Maximum Sink Current		10	mA
I_{REG} max	REG Pin Maximum Output Current		10	mA
I_{HB} max	HB Pin Maximum Output Current		10	mA
P_d max	Allowable Power Dissipation	With specified substrate (Note 2)	800	mW
T_{opr}	Operating Temperature	(Note 3)	−30 to +95	°C
T_{stg}	Storage Temperature		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The direct input from the power supply is improper. There must be resistance between OUTP and the power side power supply.
2. Specified substrate: 114.3 mm × 76.1 mm × 1.6 mm, glass epoxy board.
3. T_j max = 150°C must not be exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = 25°C)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	V_{CC} Supply Voltage		4.0 to 16	V
$V_{TH/RMI}$	VTH/RMI Input Voltage Range		0 to 4.0	V
V_{ICM}	Hall Input Voltage Range		0.2 to 1.8	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}1	CircuitCcurrent	During drive	7.5	9.0	10.5	mA
I_{CC}2		During lock protection	6.0	7.6	9.0	mA
V_{REG}	REG Voltage	I_{REG} = 5 mA	3.65	3.80	3.95	V
V_{HB}	HB Voltage	I_{HB} = 5 mA	1.14	1.24	1.34	V
V_{LIM}	Current Limiting Voltage		195	215	235	mV
V_{CPWM}H	CPWM Pin “H” Level Voltage		2.35	2.50	2.65	V
V_{CPWM}L	CPWM Pin “L” Level Voltage		0.65	0.80	0.95	V
I_{CPWM}1	CPWM Pin Charge Current	V_{CPWM} = 0.5 V	19	24	29	μA

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CPWM}2$	CPWM Pin Discharge Current	V_{CPWM} = 2.8 V	19.5	24.5	29.5	μA
FPWM	CPWM Oscillation Frequency	C = 220 pF	–	32	–	kHz
$V_{CT}H$	CT Pin “H” Level Voltage		2.35	2.50	2.65	V
$V_{CT}L$	CT Pin “L” Level Voltage		0.65	0.80	0.95	V
$I_{CT}1$	CT Pin Charge Current	V_{CT} = 0.5 V	1.6	2.0	2.4	μA
$I_{CT}2$	CT Pin Discharge Current	V_{CT} = 2.8 V	0.16	0.20	0.24	μA
R_{CT}	CT Pin Charge/Discharge Ratio	$I_{CT}1/I_{CT}2$	8	10	12	times
I_{S-S}	S−S Pin Discharge Current	V_{S-S} = 1 V	0.35	0.45	0.55	μA
$I_{OTS}1$	OTS Pin Charge Current	V_{OTS} = 0.5 V	0.65	0.85	1.05	μA
$I_{OTS}2$	OTS Pin Discharge Current	V_{OTS} = 0.5 V	50	58	66	μA
V_{OTS}	OTS Pin Threshold Voltage		1.2	1.3	1.4	V
V_ONH	OUTN Output H-level Voltage	I_O = 1 mA	–	V_{CC}−0.9	V_{CC}−1.0	V
		I_O = 10 mA	–	V_{CC}−1.9	V_{CC}−2.1	V
V_ONL	OUTN Output L-level Voltage	IO = 10 mA	–	0.9	1.05	V
V_OPL	OUTP Output L-level Voltage	IO = 10 mA	–	0.4	0.55	V
V_{HN}	Hall Input Sensitivity	IN+, IN− differential voltage (including offset and hysteresis)	–	±10	±20	mV
$V_{FG}L/_{RD}L$	FG/RD Output L−level Voltage	$I_{FG/RD}$ = 5 mA	–	0.2	0.3	V
$I_{FG}L/_{RD}L$	FG/RD Pin Leakage Current	$V_{FG/RD}$ = 19 V	–	–	10	μA
I_{VTH}/I_{RMI}	VTH/RMI Pin Bias Current	CPWM = 2 V, $V_{TH/RMI}$ = 1 V	–	–	0.3	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TRUTH TABLE − DRIVE LOCK CPWM = H VTH, RMI, S-S = L

IN−	IN+	CT	OUT1P	OUT1N	OUT2P	OUT2N	FG	RD	Mode
H	L	L	L	L	OFF	H	L	L	OUT1 → 2 drive
L	H		OFF	H	L	L	OFF	L	OUT2 → 1 drive
H	L	H	OFF	L	OFF	H	L	OFF	Lock protection
L	H		OFF	H	OFF	L	OFF	OFF	

TRUTH TABLE − SPEED CONTROL CT, S-S = L

VTH, RMI	CPWM	OTS	IN−	IN+	OUT1P	OUT1N	OUT2P	OUT2N	Mode
L	H	L	H	L	L	L	OFF	H	OUT1 → 2 drive
			L	H	OFF	H	L	L	OUT2 → 1 drive
H	L		H	L	OFF	L	OFF	H	Regeneration mode
			L	H	OFF	H	OFF	L	
H	L	H	H	L	OFF	L	OFF	L	Standby mode
			L	H	OFF	L	OFF	L	

NOTE: For VTH, RMI, and S−S pins, refer to the timing chart.

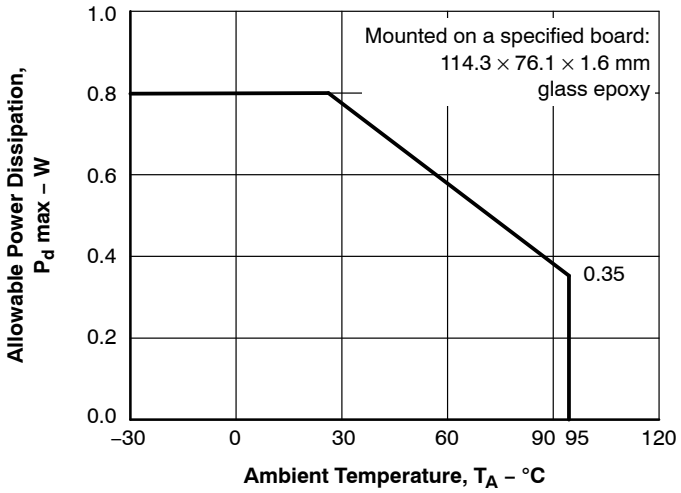


Figure 1. P_d max – T_A

BLOCK DIAGRAM

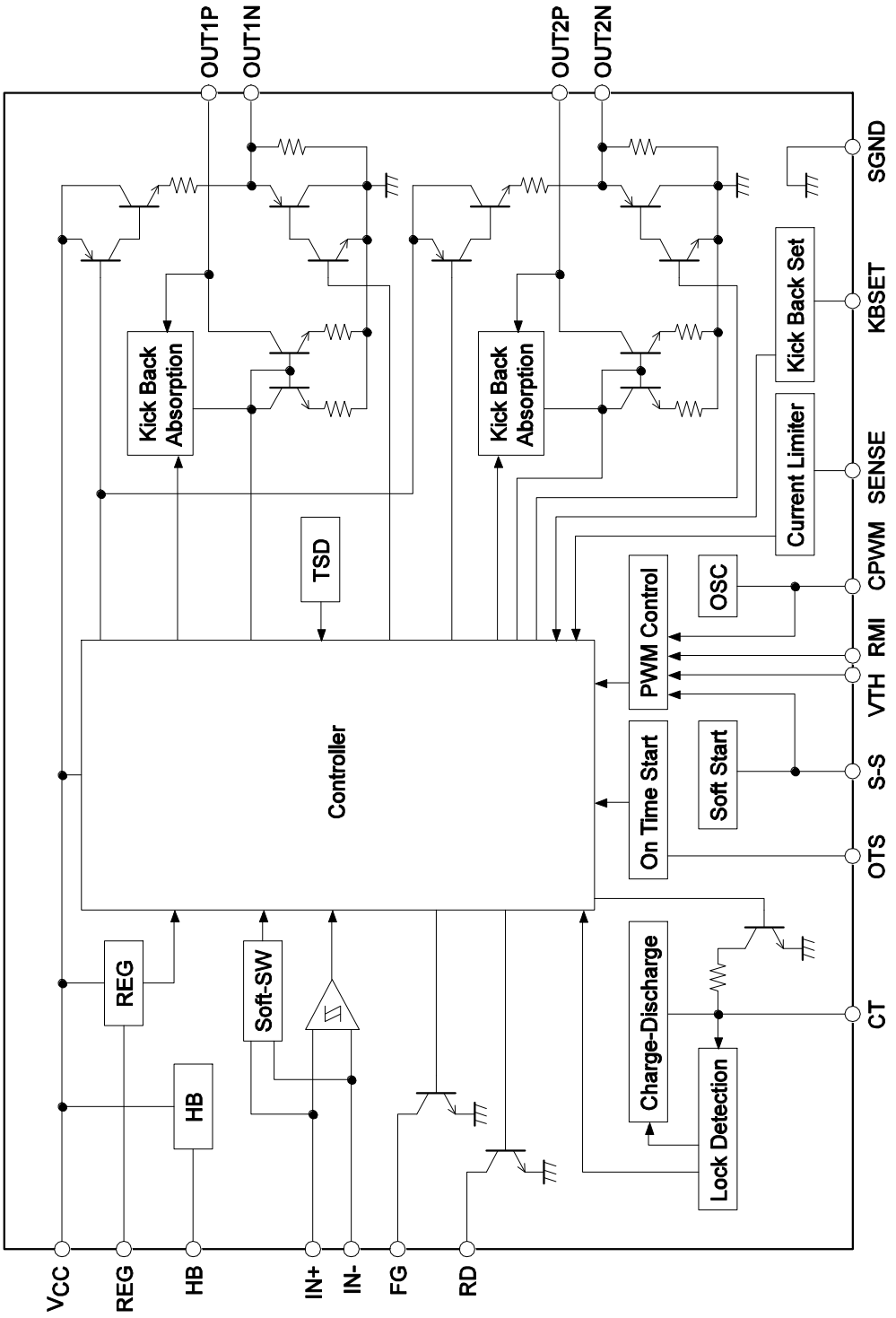


Figure 2. Block Diagram

APPLICATION CIRCUIT

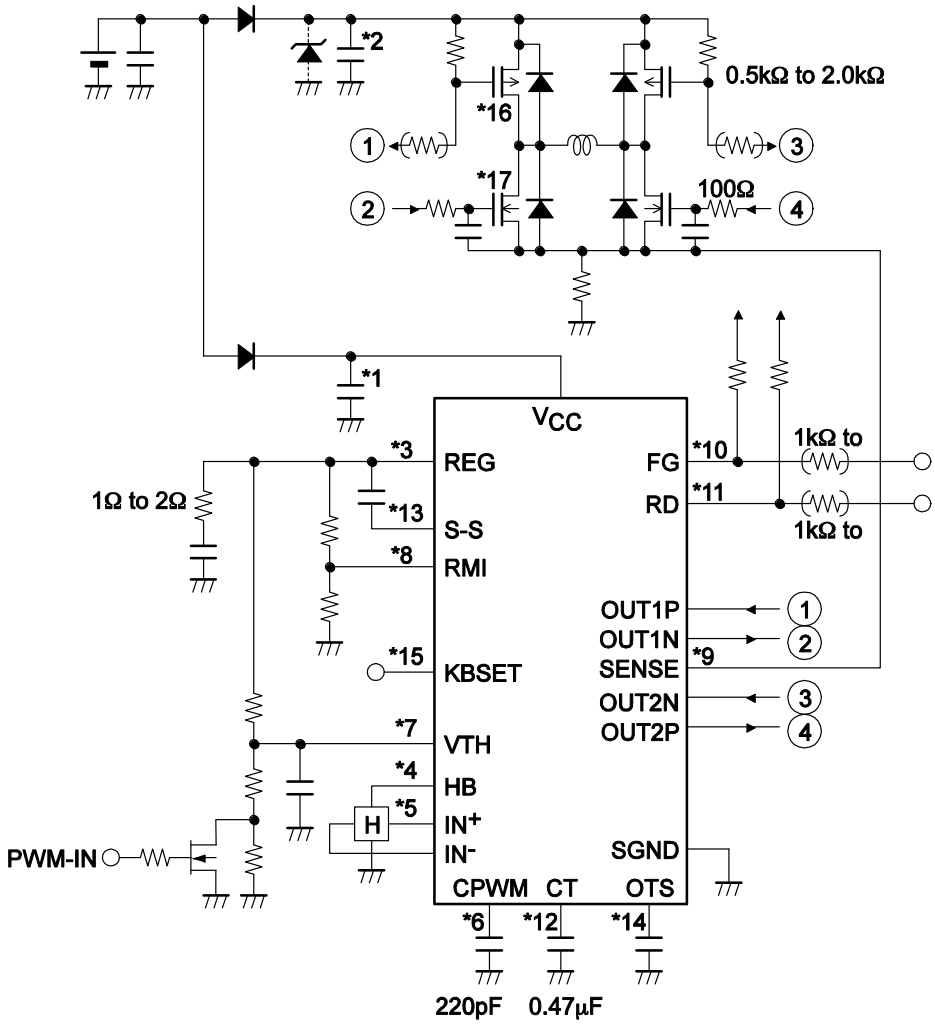


Figure 3. Application Circuit Example

*1: Power Stabilization Capacitor:
For the power stabilization capacitor on the signal side, use the capacitance of 1 μF or more.
Connect V_{CC} and SGND with a thick and shortest pattern.

*2: Power Stabilization Capacitor on the Power Side:
For the power stabilization capacitor on the power side, use the capacitance of 1 μF or more.
Connect the power supply on the power side and GND with a thick and shortest pattern.
When the IC is used for a fan with a high current level, insert a zener diode between the power supply on the power side and GND.

*3: REG Pin:
3.8 V constant-voltage output pin. For the REG oscillation prevention and stabilization, use a capacitor with capacitance of 1 μF or more.
Connect the REG pin and SGND with a thick and shortest pattern.

*4: HB Pin:
Used for Hall device bias purposes.

*5: IN+, IN− Pins:
Hall signal input pin.
Wiring should be short to prevent carrying of noise.
If noise is carried, insert the capacitor between IN+ and IN− pins.
The Hall input circuit functions as a comparator with hysteresis (15 mV).
This also has a soft switch section with ±30 mV (input signal differential voltage).
It is also recommended that the Hall input level is minimum 100mV (p−p).

*6: CPWM Pin:
Pin to connect the capacitor for generation of the PWM basic frequency.
The use of CP = 220 pF causes oscillation at f = 30 kHz (typical), which is the basic frequency

of PWM.
As this is used also for the current limiting canceling signal, ON-time start function and Soft start function, be sure to connect the capacitor even when the speed control is not made.

*7: RMI Pin:
Minimum speed setting pin.
Perform pull-up with REG when this pin is not to be used.
If the IC power supply is likely to be turned OFF first when the pin is used with external power supply, be sure to insert the current limiting resistor to prevent inflow of large current.
(The same applies to the VTH pin.)

*8: VTH Pin:
Speed control pin.
Connect this pin to GND when it is not used (at full speed).
For the control method, refer to the timing chart.
For control with pulse input, insert the current limiting resistor and use the pin with the frequency of 20 kHz to 100 kHz (20 kHz to 50 kHz recommended).

*9: SENSE Pin:
Current limiting detection pin.
When the pin voltage exceeds VLIM, the current is limited and the operation enters the lower regeneration mode.
Connect this pin to GND when it is not to be used.

*10: FG Pin:
Rotational speed detection pin.
Open collector output that can detect rotational speeds by the FG output in response to the phase switching signal.
Keep this pin open when it is not to be used.
It is recommended that a current-limiting resistor with a resistance of 1 kΩ or more be inserted in order to protect the pin during unplugging and plugging the connector or when mistakes are made in connection.

*11: RD Pin:
Lock detection pin.
In open collector output, L upon rotation and H when locked (using pull-up resistance).
Keep this pin open when it is not to be used.

*12: CT Pin:
Pin to connect the lock detection capacitor.
The constant-current charge and discharge circuits incorporated cause locking when the pin voltage becomes VCTH and unlocking when it is VCTL.
Connect the pin to GND when it is not to be used (locking not necessary).

*13: S−S Pin:
Pin to connect the soft-start setting capacitor.
Connect the capacitor between REG and S−S pin.
This pin enables setting of the soft start time according to the capacity of the capacitor.
See the timing char.
Connect the pin to GND when it is not to be used.

*14: OTS Pin:
Pin to connect the ON-time start setting capacitor.
A constant-current charging circuit and a discharging circuit based on the control duty ratio are incorporated, and when the pin voltage exceeds VOTS, the CT pin is discharged and the S−S pin is charged.
Connect the pin to GND when it is not to be used (when the lowest speed setting is used).

*15: KBSET Pin:
Pch kickback absorption circuit setting pin.
Open: The kickback absorption circuit is activated at a VCC voltage of 7.4 V (typ) or above.
Pull-down to GND: Always OFF
Pull-up to REG: Always ON (but when the IC power is OFF, the kickback absorption circuit is OFF)
If the Pch load is to be reduced due to the large fan current, short the KBSET pin to GND, and use a zener diode between the power supply on the power side and GND.
Kickback absorption circuit ON: At OUTPOFF, the OUTP voltage is clamped at VCC + 0.85 V (at room temperature and inflow current 5 mA (typ)).
Kickback absorption circuit OFF: At OUTPOFF, the OUTP voltage is clamped at 18 V or so (at room temperature and inflow current 5 mA (typ)) in order to protect the pin.
At OUTPOFF, the maximum inflow current must not be exceeded.

*16: Pch FET:
If the Pch kickback absorption circuit is activated and a zener diode between the power supply and GND is not used, the kickback during phase switching is absorbed by Pch.
Since the circuit is activated with a high voltage difference between the drain and source, select a FET with sufficiently high capability.

*17: Nch FET:
If the Nch gate voltage fluctuates significantly due to the effects of switching, insert a capacitor between the gate and GND.
Since an Nch diode is used during coil current regeneration, select a FET with sufficiently high capability.

CONTROL TIMING CHART (SPEED CONTROL)

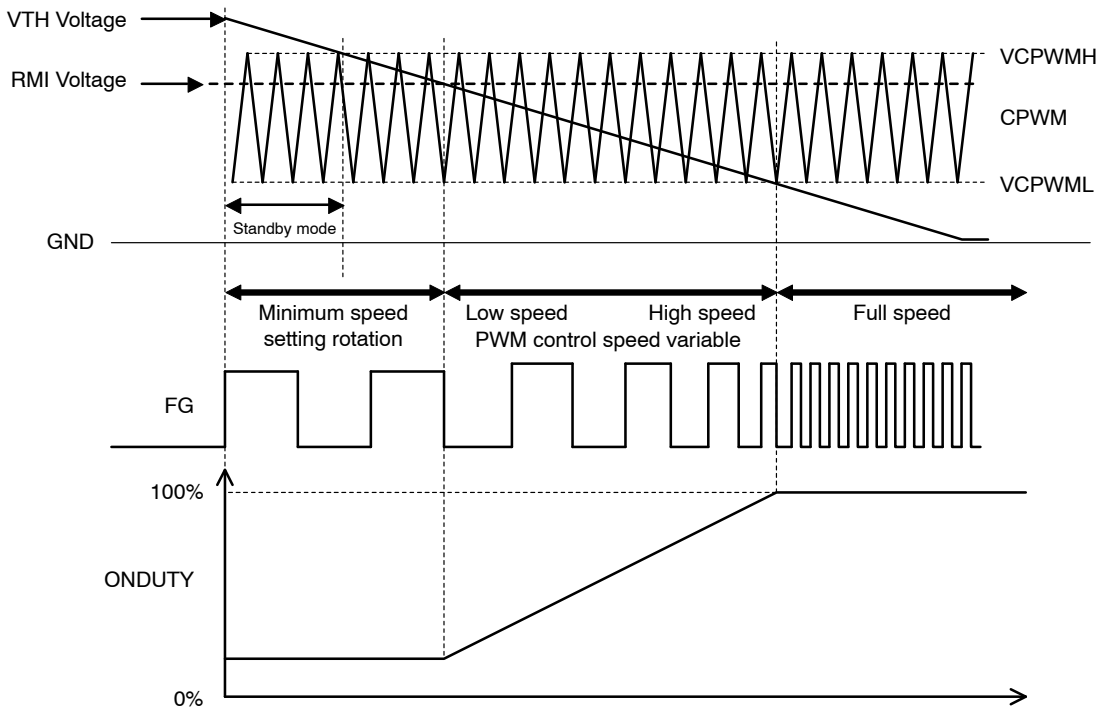


Figure 4. Control Timing Chart – Speed Control

1. Minimum Speed Setting (Standby) Mode:
   The low-speed fan rotation occurs at the minimum speed set with the RMI pin.
   When the minimum speed is not set (RMI pin pulled up to REG), the motor stops.
   If the VHT voltage rises when the lowest speed is not set (RMI pin is pulled up to REG), the fan stops running, and if the OTS pin capacitor is used, the standby mode is established.
   Details of the standby mode are given in the section “Control timing chart (ON-time start, Lock protection).
2. Low Speed ⇔ High Speed:
   PMW control is made by comparing the CPWM oscillation voltage (VCPWMLVCPEMH) and VTH voltage.
   The drive mode is established when the VTH voltage is low.
   Both upper and lower output FET are turned ON when the VTH voltage is low.
   When the VTH voltage is high, Pch is turned off, and the coil current is regenerated inside the lower FET. Therefore, as the VTH voltage decreases, the output ON-DUTY increases, causing an increase in the coil current and raising the motor rotation speed.
   The upper output Pch is turned OFF when the VTH voltage is high, regenerating the coil current in the lower TR. Therefore, as the VTH voltage decreases, the output ON-DUTY increases, causing increase in the coil current, raising the motor rotation speed.
   The rotational speed can be monitored using the FG output.
3. Full Speed Mode:
   The full speed mode becomes effective when the VTH voltage is VCPWML or less. (Set VTH = GND when the speed control is not to be made.)

CONTROL TIMING CHART (SOFT START)

1. At VTH < RMI Voltage

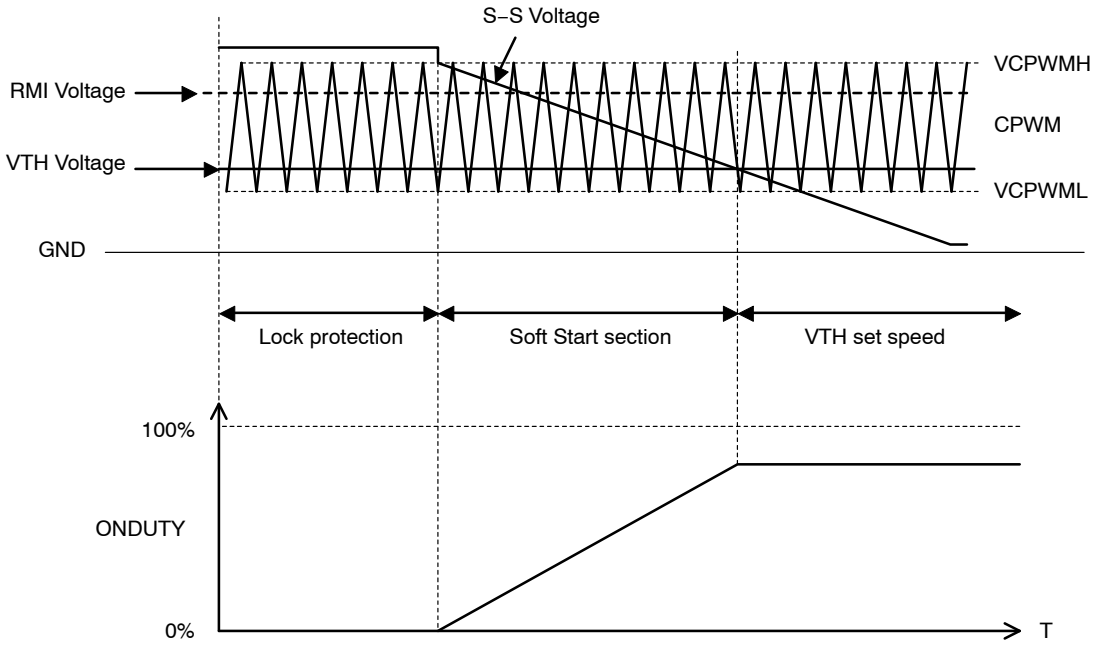


Figure 5. At VTH < RMI Voltage

2. At VTH > RMI Voltage

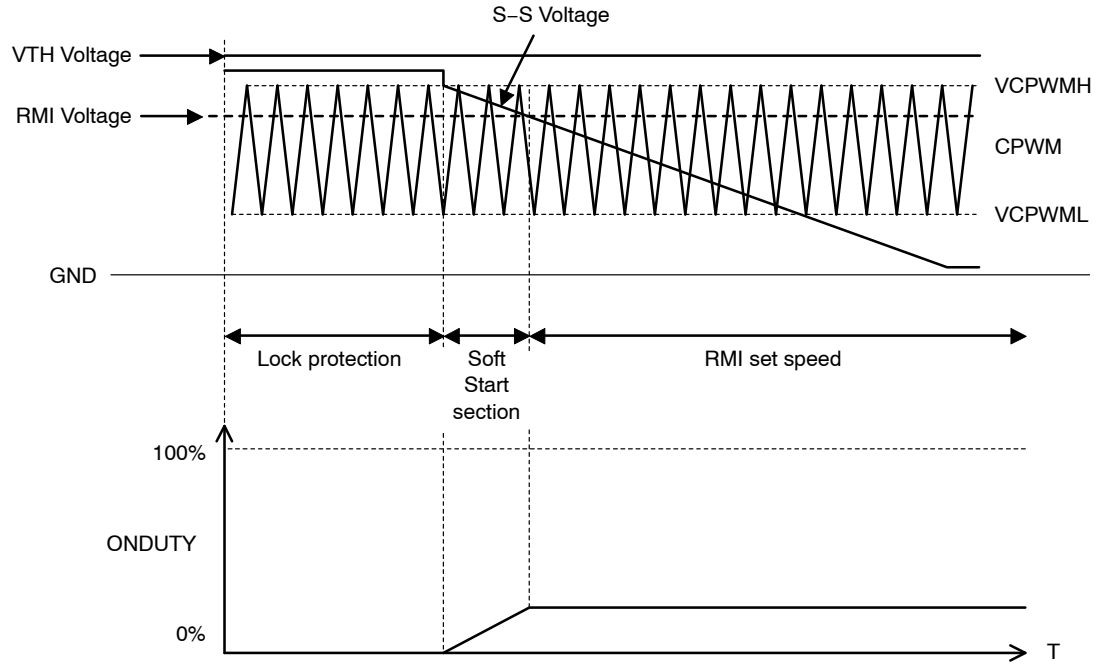


Figure 6. At VTH > RMI Voltage

Adjust the S−S pin voltage gradient by means of the capacitance of the capacitor between the S−S pin and REG.

Recommended capacitor: 0.1 μ to 1 μF

CONTROL TIMING CHART
(ON-TIME START, LOCK PROTECTION)

1. When a stop signal based on the VTH voltage has been input during normal rotation.

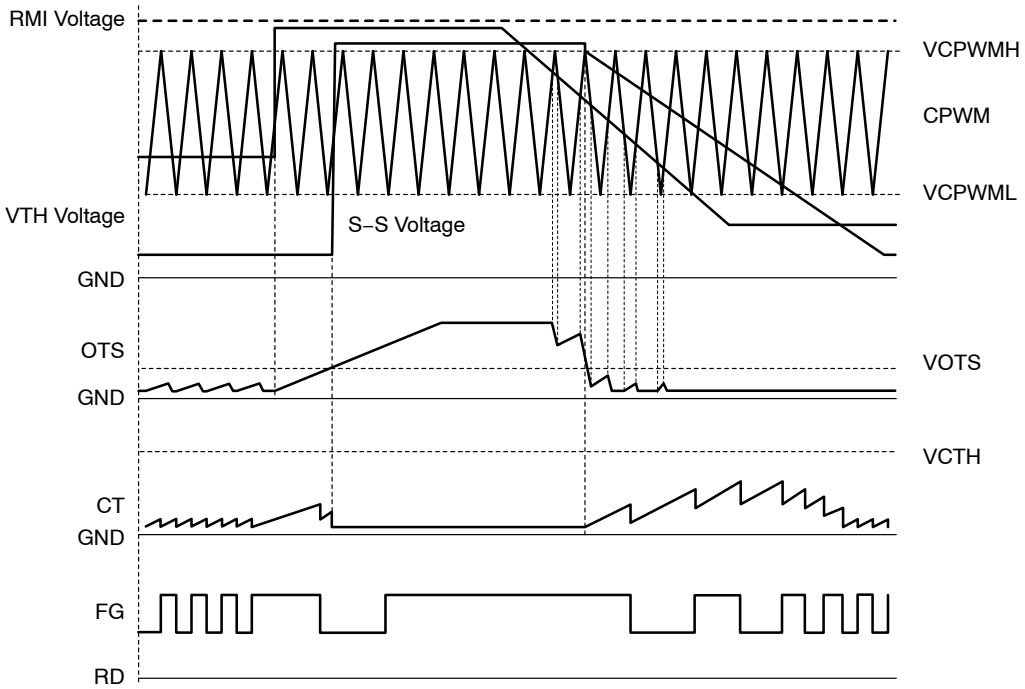


Figure 7.

When the output duty ratio based on the VTH/RMI input drops to below 1% or so, the OTS voltage rises, and when it reaches VOTS, the standby mode is established, the CT pin discharges, and the S−S pin is charged. In the standby mode, if the drive mode has been established again by the VTH/RMI input, the rotation is started immediately with soft start.

The CT pin discharges at the same time as the switching of FG. For details on lock protection, refer to 2.

2. When a stop signal based on the VTH voltage has been input while the fan is constrained

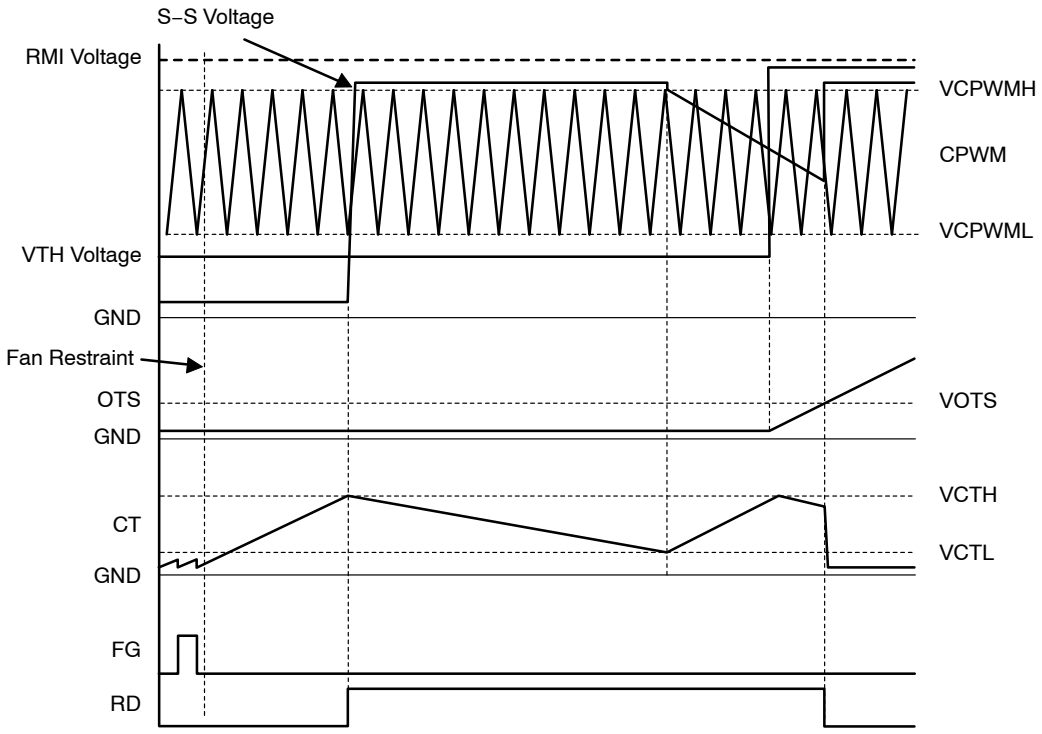


Figure 8.

When the fan is constrained, the CT pin voltage rises, and when it reaches VCTH, the lock protection mode is established, and OUTP is set to OFF and RD is set to OFF.

When the lock protection mode is established, the CT pin discharges, and when VCTL is reached, restart (soft start) is initiated. When rotation is started and the FG signal is switched, RD is set to low.

NOTE: RD is also set to low when the standby mode is established when locked.

ORDERING INFORMATION

Device	Package	Wire Bond	Shipping† (Qty / Packing)
LB11868V−TLM−H	SSOP20J (225mil) (Pb−Free / Halogen Free)	Au−wire	2,000 / Tape & Reel
LB11868V−W−AH	SSOP20J (225mil) (Pb−Free / Halogen Free)	Cu−wire	2,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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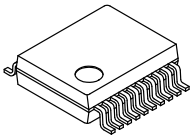
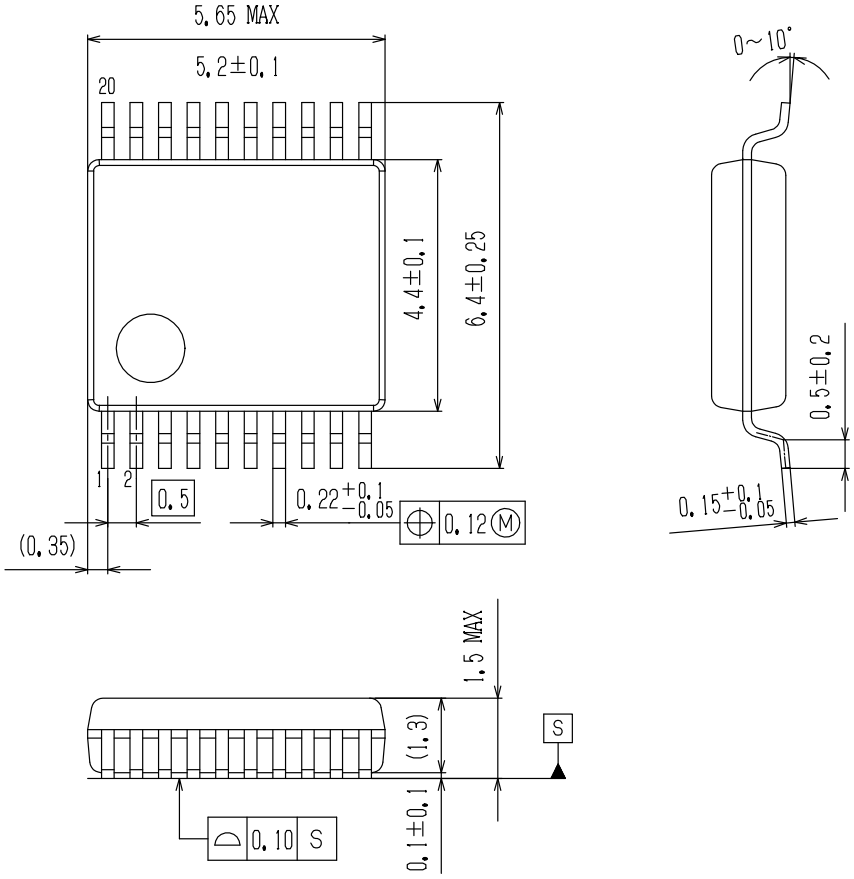
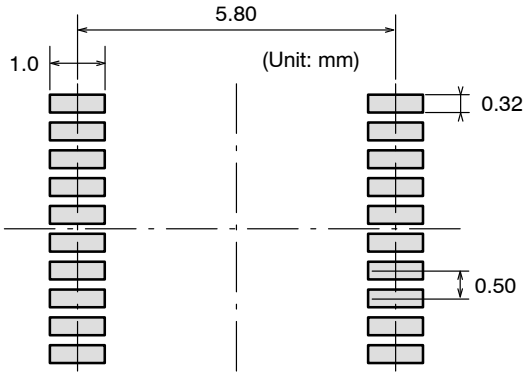
SSOP20J (225mil)
CASE 565AP
ISSUE A

DATE 23 OCT 2013





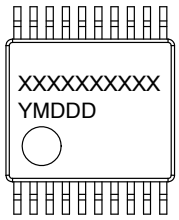
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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