

# LC709501F

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## Power Bank Controller with USB Type-C & Quick Charge™ 3.0 for 1-Cell Li-Ion and Li-Poly Battery

### Overview

LC709501F is a Lithium ion switching charger controller for Power Bank. This device has all functions to control Power Bank application. It can control Type-C port control IC and includes Quick Charge 3.0 HVDCP. The built-in switching controller can output from 5 V up to 12 V for Quick Charge. The high power output for USB Type-C and Quick Charge is possible with appropriate external MOSFETs.

### Features

- Easy power scaling with external MOSFETs.
- Buck charge / Boost charge
- Supports Quick Charge 3.0 HVDCP Class A. 5 V up to 12 V
- Supports USB type-C DRP with Port control IC.
- Prepared firmware supports various combination of USB port.
- Supports USB BC1.2
- Controls an external Boost-IC for 2<sup>nd</sup> USB output
- Battery level gauging
- Status & Battery level display with 4 LEDs
- Boost auto start-up
- Thermistor sensing function
- Over voltage / Over current detection
- JEITA compliance Battery management
- Safety timer
- Low quiescent current: 15  $\mu$ A at Low power mode

### Applications

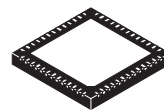
- Power Bank
- USB-related charging application



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QFN52 6x6, 0.4P  
Pb-Free, Halogen Free type

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### ORDERING INFORMATION

See detailed ordering and shipping information on page 29 of this data sheet

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## Application Circuit Example 1

### Micro-B (Sink, BC1.2) + Type-A (1) (Source, Quick Charge 3.0 HVDCP) with Portable device communication + Type-A (2) (Source, DCP)

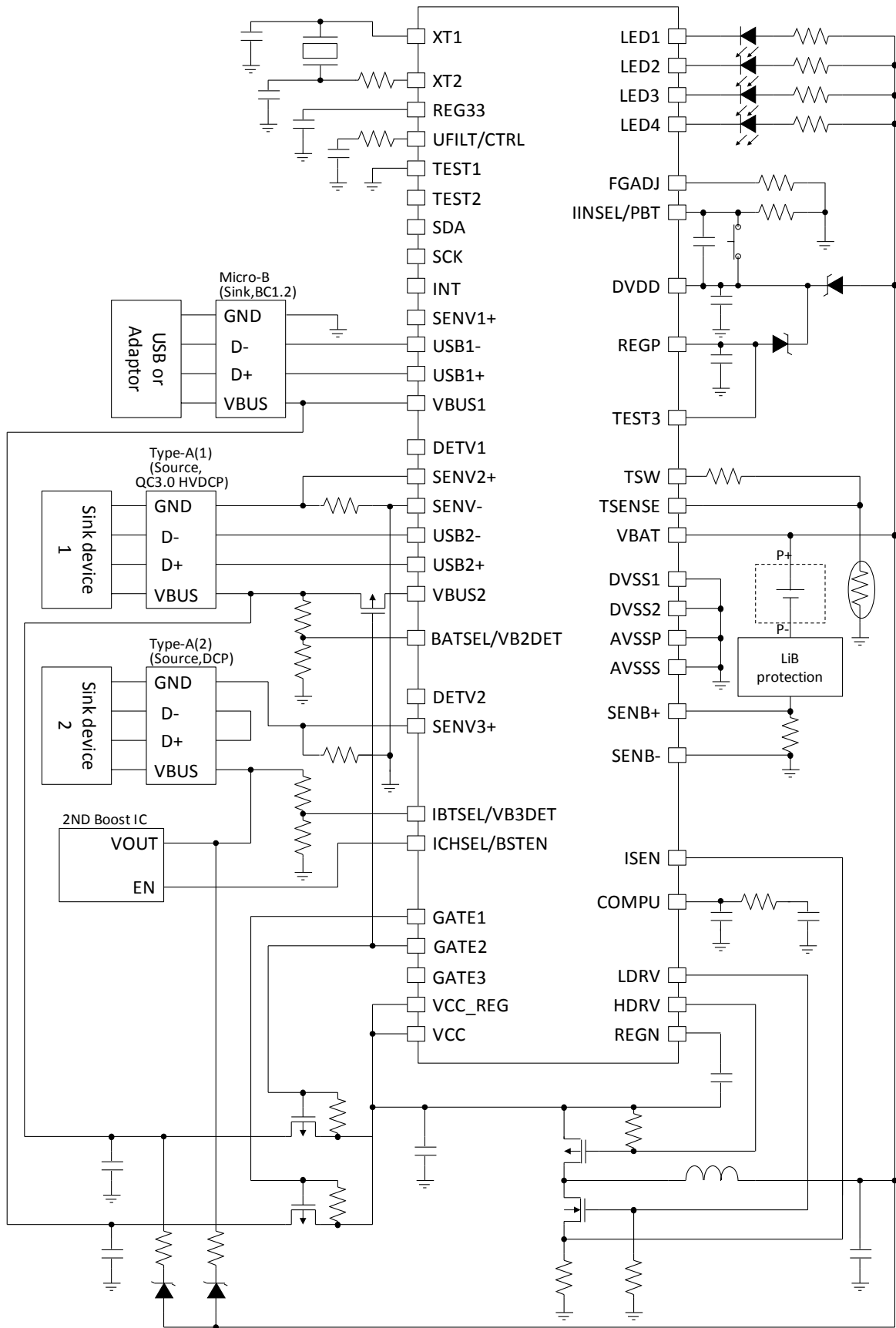


Figure 1: Example of an application schematic (Firmware: FW01)

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## Application Circuit Example 2

### Micro-B (Sink, BC1.2) + Type-A (1) (Source, Quick Charge 3.0 HVDCP) without Portable device communication + Type-A (2) (Source, DCP)

Note) XT oscillator and passive components for Portable device communication can be omitted.

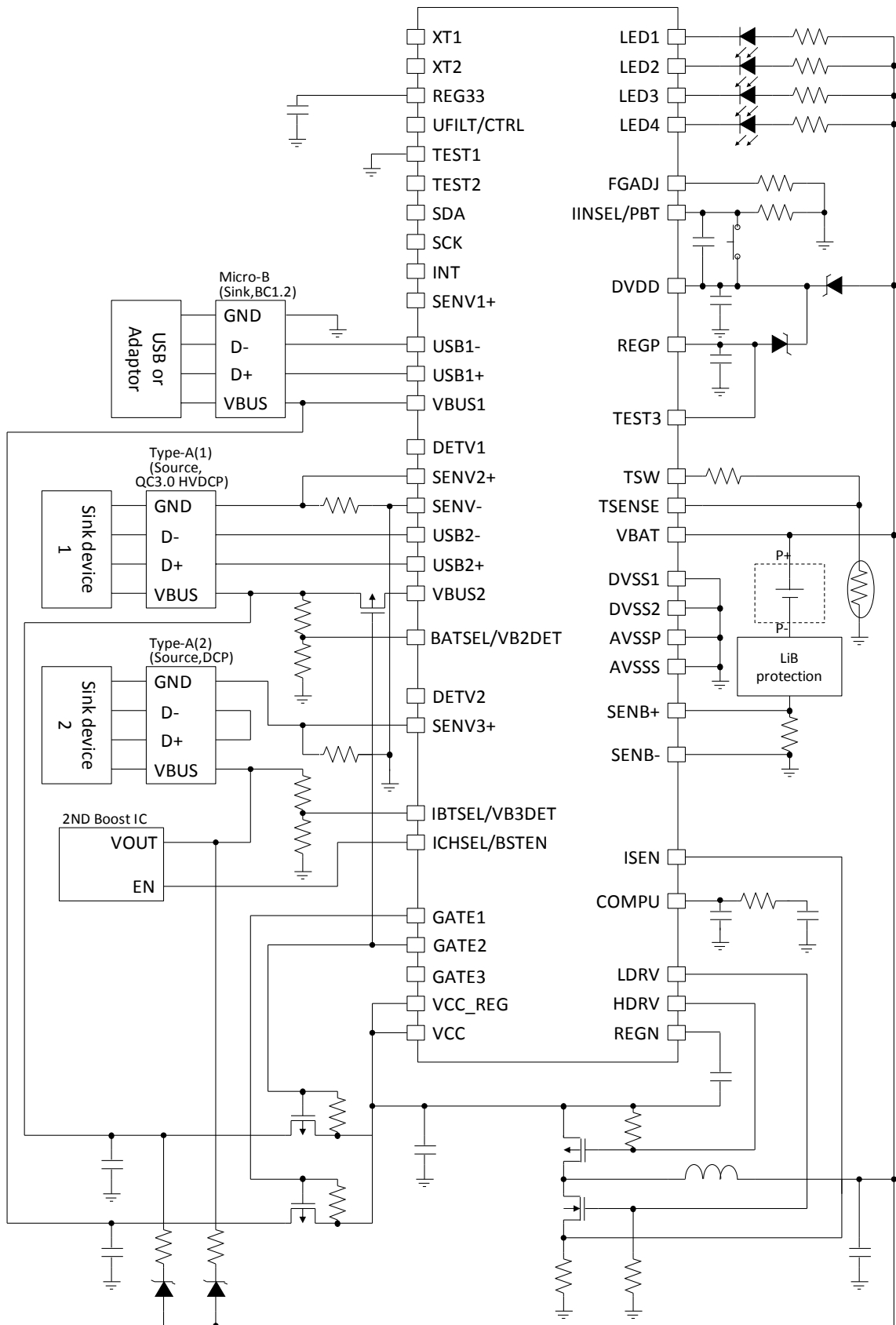


Figure 2: Example of an application schematic (Firmware: FW02)

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## Application Circuit Example 3 Type-C (DRP, Quick Charge 3.0 HVDCP) + Type-A (Source, DCP)

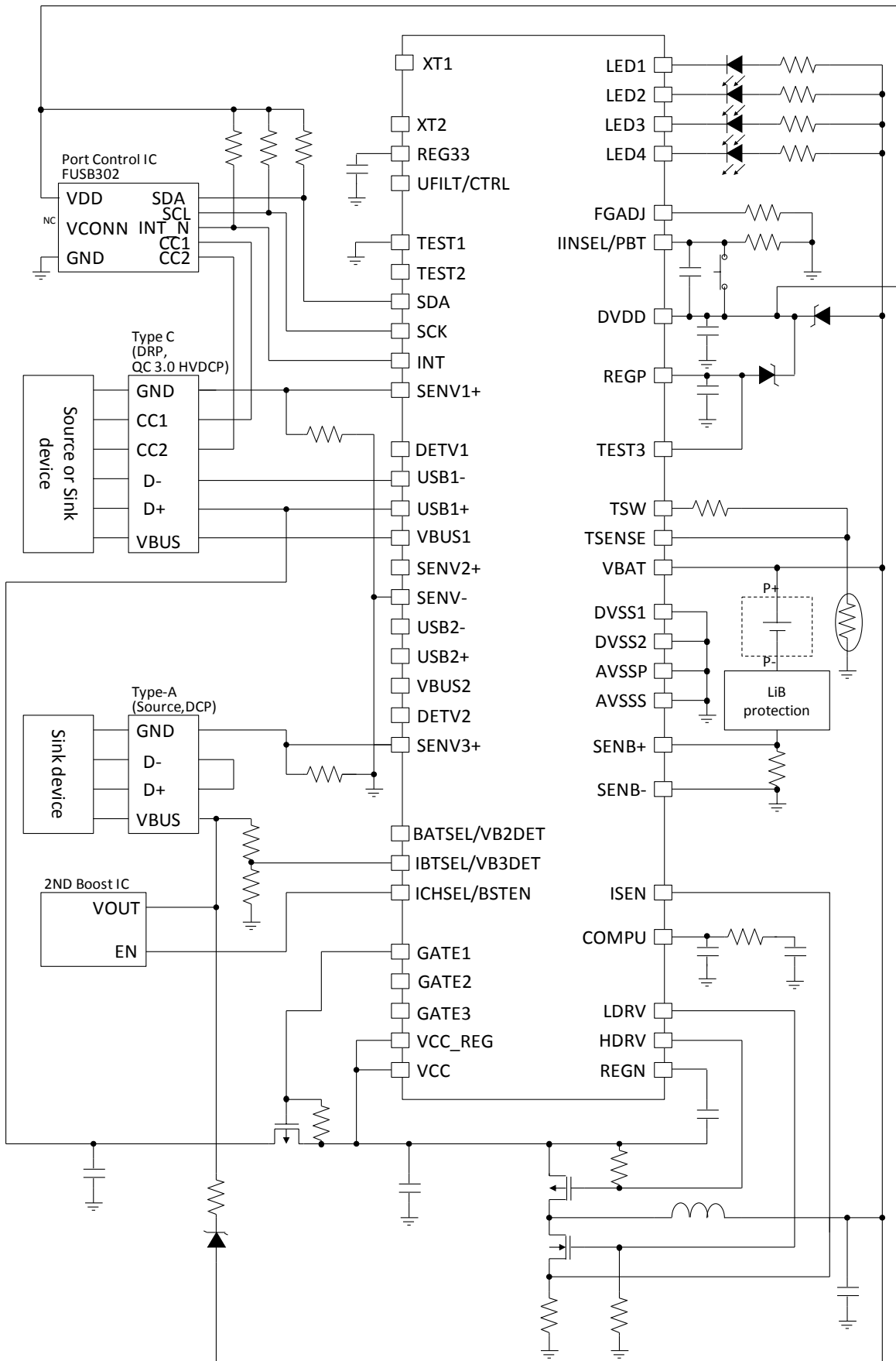


Figure 3: Example of an application schematic (Firmware: FW05)

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## Pin Assignment

QFN52 6x6, 0.4P

Top view

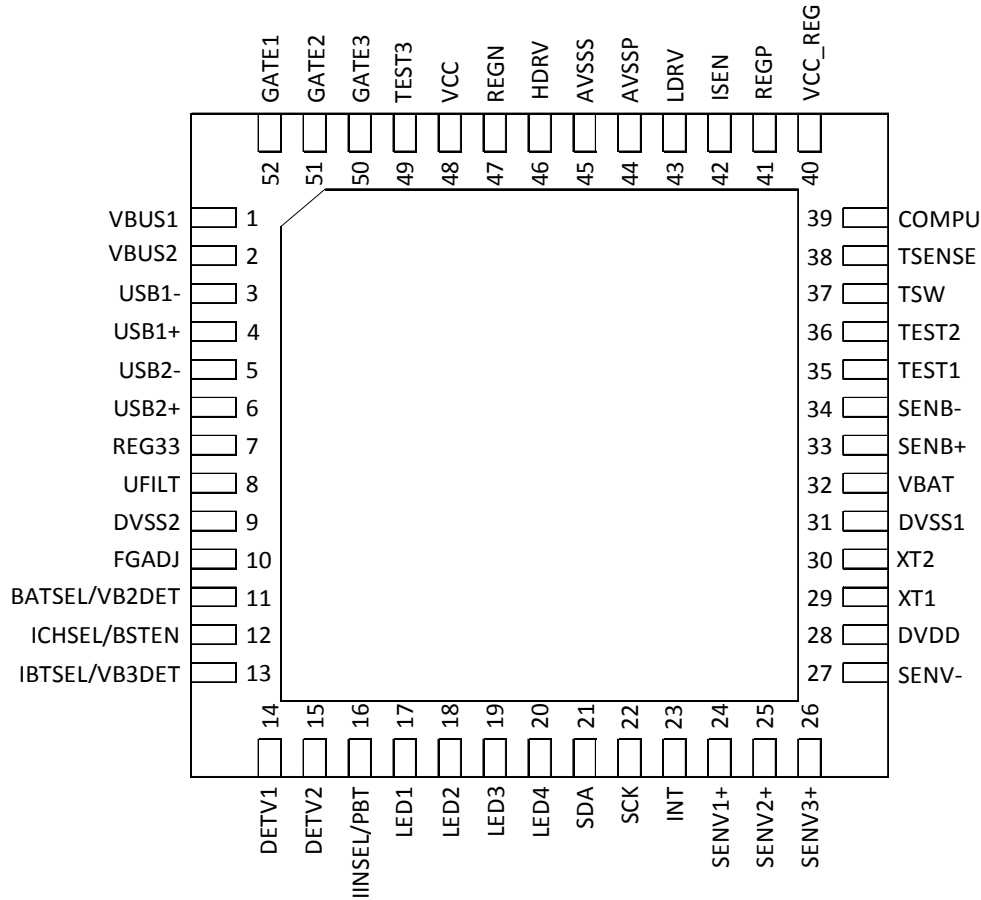


Figure 4: Pin Assignment

Table 1. Pin Function

No.	Pin Name	I/O	Description
1	VBUS1	I	Connect this pin to the VBUS of Micro B (sink) or Type-C.
2	VBUS2	I	Connects this pin to the VBUS of Type-A (1) through Pch-FET.
3	USB1-	I/O	USB D- data line input. Connect this pin to USB Host/Charging port to detect USB port (BC1.2, dedicated charger).
4	USB1+	I/O	USB D+ data line input. Connect this pin to USB Host/Charging port to detect USB port (BC1.2, dedicated charger).
5	USB2-	I/O	USB D- data line output. Connect this pin to communicate with Portable USB devices Supports Quick Charge 3.0 HVDACP.
6	USB2+	I/O	USB D+ data line output. Connect this pin to communicate with Portable USB devices Supports Quick Charge 3.0 HVDACP.
7	REG33	-	Connect this pin and a capacitor
8	UFILT	-	Connect this pin and a capacitor only for USB Full-speed host function. Keep this pin OPEN otherwise.
9	DVSS2	-	Connect this pin to GND.
10	FGADJ	I	Sets the design capacity of a battery. Pull down this pin to GND through resistor.
11	BATSEL/VB2DET	I	Detects USB Type-A (1) plug insertion.
12	ICHSEL/BSTEN	O	An external Boost-IC control. This pin is set to "HIGH" when it outputs to VBUS of Type-A (2).
13	IBTSEL/VB3DET	I	Detects USB Type-A (2) plug insertion.
14	DETV1(TEST)	-	Keep this pin OPEN.

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**Table 1. Pin Function (continue)**

No.	Pin Name	I/O	Description
15	DETV2(TEST)	-	Keep this pin OPEN.
16	IINSEL/PBT	I	Push button input.
17	LED1	O	Displays battery level. This is an open drain pin.
18	LED2	O	Displays battery level. This is an open drain pin.
19	LED3	O	Displays battery level. This is an open drain pin.
20	LED4	O	Displays battery level. This is an open drain pin.
21	SDA	I/O	Master I <sup>2</sup> C Data pin (open drain). This controls Port control ICs when the Firmware is FW05. Pull-up must be done externally when using it. Keep this pin OPEN otherwise.
22	SCK	I/O	Master I <sup>2</sup> C Clock pin (open drain). This controls Port control ICs when the Firmware is FW05. Pull-up must be done externally when using it. Keep this pin OPEN otherwise.
23	INT	I	Interrupt input from Port control IC when the Firmware is FW05. Pull-up must be done externally when using it. Keep this pin OPEN otherwise.
24	SENV1+	I	Connect this pin to positive terminal of sense resistor to detect the current when the Firmware is FW05.
25	SENV2+	I	Connect this pin to positive terminal of sense resistor to detect Type-A (1) output current.
26	SENV3+	I	Connect this pin to positive terminal of sense resistor to detect Type-A (2) output current.
27	SENV-	I	Connect this pin to negative terminal of sense resistor to detect the current.
28	DVDD	-	Digital power supply. Connect this pin to REGP through a schottky diode.
29	XT1	I	Crystal resonator input.
30	XT2	O	Crystal resonator output.
31	DVSS1	-	Connects this pin to GND.
32	VBAT	I	Connect this pin to positive pin of a battery.
33	SENB+	I	Connect this pin to positive terminal of sense resistor to detect battery current.
34	SENB-	I	Connect this pin to negative terminal of sense resistor to detect battery current.
35	TEST1	I	Connect this pin to GND.
36	TEST2	I	Keep this pin OPEN.
37	TSW	O	Power supply output for thermistor. This pin is set to "HIGH" when reading the temperature. Resistance value of TSW (for thermistor pull-up) must be the same value as the thermistor at 25°C.
38	TSENSE	I	Thermistor sense input. Use 100 Ω resistor when connecting this pin to a thermistor.
39	COMPU	-	Connect this pin to a capacitor through a resistor.
40	VCC_REG	-	Power supply. Connect this pin to V <sub>CC</sub> .
41	REGP	O	4.7 V LDO output. (for internal use) Connect capacitor to this pin.
42	ISEN	I	Senses buck-boost converter output current. The sense resistor must be placed between DC-DC converter ground and the source of the MOSFET (Figure 1)
43	LDRV	I	PWM output.
44	AVSSP	-	Connect this pin to GND.
45	AVSSS	-	Connect this pin to GND.
46	HDRV	O	PWM output.
47	REGN	O	VCC-4.7 V LDO output. (for internal use) Connect capacitor to this pin.
48	VCC	-	Power supply.
49	TEST3	I	Select PWM frequency with this pin. Connect this pin to GND to select 150 kHz. Connect this pin to REGP to select 300 kHz.
50	GATE3	-	Keep this pin open.
51	GATE2	O	Control the gate of a FET for Type-A (1).
52	GATE1	O	Control the gate of a FET for Micro-B (sink) or Type-C.

**Table 2. Absolute Maximum Ratings**

Parameter	Symbol	Pin/Remarks	Conditions	Specification			Unit
				min	typ	max	
Input voltage	HVIN max	VBUS1, VBUS2, GATE1, GATE2, GATE3, HDRV, VCC, VCC_REG		-0.3		+14	V
	VIN max	Low voltage pins except for HV pins.		-0.3		+6.5	
Allowable power dissipation	Pd max *					1	W
Storage ambient temperature	Tstg			-40		125	°C
Operating junction temperature	Tjopr			-40		125	

\* Thermal resistance evaluation board (size: 120.2 x 59.9 x 1.69 mm, 6 layers) is used. The device is solder-mounted.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. Electrical Characteristics**

**Recommended Operating Ranges**

Parameter	Symbol	Pin / Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	VCC	VCC, VCC_REG	2.8		13.2	V
Digital supply voltage	VDD	DVDD	2.8		5.5	V
Battery voltage	VVBAT	VBAT	3.0		4.35	V
Low power mode ambient temperature range	TASTB	Low power mode and displays battery level	-40		85	°C
Boost charge mode ambient temperature	TABST	Boost charge	-20		60	°C
Buck charge mode ambient temperature	TABUCK	Buck charge	0		60	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Electrical Characteristics at Ta = 25°C**

Parameter	Symbol	Pin / Conditions	Ratings			Unit
			min	typ	max	
Consumption current at Low power mode	ILOW	VCC = VCC_REG = 3.7 V ILOW = I_VCC + I_VCC_REG at Low power mode		15		μA
Consumption current at operating mode	IOPR	VCC = VCC_REG = 5 V IOPR = I_VCC + I_VCC_REG at Boost charge mode		10		mA
HDRV High-side ON Resistance	HDRVH	HDRV		2		Ω
HDRV Low-side ON Resistance	HDRV L	HDRV		3		Ω
LDRV High-side ON Resistance	LDRVH	LDRV		3		Ω
LDRV Low-side ON Resistance	LDRV L	LDRV		2		Ω
Gate1/2/3 Drive voltage	VGATE	GATE1, GATE2, GATE3 Pull up these pins to VCC through 510 kΩ	0		0.2	V
VCC UVLO	UVLO	VCC rising		2.72	2.8	V
		UVLO hysteresis		0.1		V
Thermal Shut down Threshold	THD			105		°C

**VBUS input / output**

VBUS over voltage detection	VBOVP	VBUS1, VBUS2, 5 V mode		5.6		V
		VBUS1, VBUS2, 9 V mode		10.2		V
		VBUS1, VBUS2, 12 V or Continuous mode		13.5		V
VBUS under voltage detection	VBUVP	VBUS1, VBUS2			4.4	V
Maximum input current	IINMAX	VBUS1, FW02: For Micro-B		2400		mA
		VBUS1, FW05: For Type-C		3000		mA

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## Electrical Characteristics at Ta = 25°C

### Buck charge

Parameter	Symbol	Pin / Conditions	Ratings			Unit
			min	typ	max	
Frequency	F <sub>BC</sub>	TEST3=Low		150		kHz
		TEST3=High		300		kHz
Battery capacity range			2000		24400	mAh
Quiescent input current	I <sub>CHROFF</sub>	VBUS1, VBUS2, Charge mode Switching OFF current VBUS = 5 V			3	mA
Pre-Charge Current range	I <sub>PRE</sub>	SENB+, SENB-, 10 mΩ resistor	200		500	mA
Pre-Charge Voltage Threshold	V <sub>PRE</sub>	VBAT		3.25		V
Constant Charge Current range	I <sub>CHG</sub>	SENB+, SENB-, 10 mΩ resistor VBAT = 3.7V	1000		6000	mA
Termination Current range	I <sub>TERM</sub>	SENB+, SENB-, 10 mΩ resistor	200		800	mA
Termination Battery Voltage	V <sub>CHG</sub>	VBAT, 4.2 V battery type		4.2		V
		VBAT, 4.35 V battery type		4.35		V
VBAT over voltage detection	V <sub>BATOVP</sub>	VBAT rising		4.6		V
Drop of Termination Battery Voltage at hot temperature	V <sub>CHGH</sub>	VBAT		200		mV
Cold temperature threshold at Buck charge	T <sub>COLD</sub>			0		°C
Cool temperature threshold at Buck charge	T <sub>COOL</sub>			10		°C
Warm temperature threshold at Buck charge	T <sub>WARM</sub>			45		°C
Hot temperature threshold at Buck charge	T <sub>HOT</sub>			60		°C

### Boost charge

Parameter	Symbol	Pin / Conditions	Ratings			Unit
			min	typ	max	
Boost frequency	F <sub>BT</sub>	TEST3=Low		150		kHz
		TEST3=High		300		kHz
Output Voltage Range	V <sub>BST</sub>	VBUS1, VBUS2, 5 V mode	4.75	5	5.25	V
		VBUS1, VBUS2, 9 V mode	8.2	9	9.8	V
		VBUS1, VBUS2, 12 V mode	10.9	12	13.1	V
Termination boost current	I <sub>BTERM</sub>	SENV1+, SENV2+, SENV3+, SENV-, 20 mΩ resistor		200		mA
Maximum output current	I <sub>OUTMAX</sub>	SENV1+, SENV2+, SENV-, 20 mΩ resistor				
		Output voltage ≤ 7.5 V		3000		mA
		7.5 V < Output voltage ≤ 10.5 V		2300		mA
		10.5 V < Output voltage		1800		mA
		SENV3+, SENV-, 20 mΩ resistor		2000		mA
Cold temperature threshold at Boost charge	T <sub>COLD2</sub>			-20		°C
Hot temperature threshold at Boost charge	T <sub>HOT2</sub>			60		°C

## Electrical Characteristics at Ta = -40 to +85°C, V<sub>DD</sub> = 2.8 V to 5.5 V, Ta = 25°C for typical values.

Parameter	Symbol	Pin / Conditions	Ratings			Unit
			min	typ	max	
LED sink current	I <sub>LED</sub>	LED1, LED2, LED3, LED4		10		mA
VBUS input detection voltage	V <sub>BDET</sub>	VBUS1, VBUS2 rising			4	V
High level input voltage	V <sub>IH</sub> (1)	PBT	0.3*V <sub>DD</sub> +0.7		V <sub>DD</sub>	V
	V <sub>IH</sub> (2)	SDA, SCL, INT	1.4			V
Low level input voltage	V <sub>IL</sub> (1)	PBT	V <sub>SS</sub>		0.15V <sub>DD</sub> +0.4	V
	V <sub>IL</sub> (2)	SDA, SCL, INT			0.5	V
Input voltage hysteresis	V <sub>HYS</sub>	SDA, SCL		0.1V <sub>DD</sub>		V
High level output voltage	V <sub>OH</sub>	TSW, BSTEN IOH = -0.4 mA	V <sub>DD</sub> -0.4			V
Low level output voltage	V <sub>OL</sub> (1)	BSTEN IOL = 0.4 mA			0.4	V
	V <sub>OL</sub> (2)	SDA, SCL, INT IOL = 3.0 mA			0.4	V
Pull-up resistance at turn on	R <sub>PU</sub>	FGADJ		50		kΩ
Oscillation frequency for USB host	F <sub>XT</sub>	XT1, XT2		12		MHz



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**Electrical Characteristics** at Ta = -40 to +85°C, V<sub>DD</sub> = 2.8 V to 5.5 V, Ta = 25°C for typical values.

## BC1.2 / HVDCP

Parameter	Symbol	Pin / Conditions	Ratings			Unit
			min	typ	max	
D- Pull Down Resistance	RDM_DWN	USB1-, USB2-		19.53		kΩ
D+ Pull Down Resistance	RDP_DWN	USB1+, USB2+		19.53		kΩ
D- Source Voltage	VDM_SRC	USB1-, USB2-		0.6		V
D+ Source Voltage	VDP_SRC	USB1+, USB2+		0.6		V
D- Sink Current	IDM_Sink	USB1-, USB2-		100		μA
D+ Sink Current	IDP_Sink	USB1+, USB2+		100		μA
Data line leakage resistance	R <sub>DAT_LKG</sub>	USB2-,USB2+	300	900	1500	kΩ
DCP resistance across D+/-	R <sub>DCP_DAT</sub>	USB2-,USB2+			45	Ω

## LED

Battery level indication time	T <sub>LBAT</sub>	LED1, LED2, LED3, LED4		3		s
Battery level indication delay	T <sub>LDELAY</sub>	LED1, LED2, LED3, LED4		0.1		s
Lighting time during flashing	T <sub>FLS_L</sub>	LED1, LED2, LED3, LED4		0.25		s
Lights out time during flashing	T <sub>FLS_H</sub>	LED1, LED2, LED3, LED4		0.25		s
Lights up time at start of Buck/Boost charge	T <sub>LSTA</sub>	LED1, LED2, LED3, LED4		2		s
Buck charge indication time	T <sub>LBUCK</sub>	LED1, LED2, LED3, LED4		30		s
Buck charge lights on delay after transition to Operating mode	T <sub>SBUCK</sub>			0.2		s
Boost charge indication time	T <sub>LBST</sub>	LED1, LED2, LED3, LED4		5		s
VBUS1 judge delay after transition to Operating mode	T <sub>VBDET</sub>			0.2		s
Temperature of TSENSE detection time	T <sub>TSDET</sub>			2		s
TSENSE Disconnect detection time	TTDISDET			2		s
Temperature of Internal Thermistor detection time	T <sub>ITDET</sub>			2		s
Lighting time during VBUS1 warning	T <sub>FLS2_L</sub>	LED1, LED2, LED3, LED4		0.1		s
Lights out time during VBUS1 warning	T <sub>FLS2_H</sub>	LED1, LED2, LED3, LED4		1.9		s
Lights out time during Temperature warning	T <sub>FLS3_H</sub>	LED1, LED2, LED3, LED4		0.3		s
Lights interval time during Temperature warning	T <sub>FLS_INT</sub>	LED1, LED2, LED3, LED4		3		s
Time recognized as short-press	T <sub>SBOT</sub>	PBT	0.06		1.8	s
Time recognized as long-press	T <sub>LBOT</sub>	PBT	2.2			s

## Safety timer

Continuous battery charging time	T <sub>CMAX</sub>			15		h
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## USB HOST at Ta = 0 to +70°C, V<sub>DD</sub> = 4.0 to 5.5 V

Parameter	Symbol	Pin/Conditions	Ratings			Unit
			min	typ	max	
High level output	VOH (USB2+/-)	14.25 kΩ to GND	2.8		3.6	V
Low level output	VOL (USB2+/-)	1.425 kΩ to 3.6 V	0		0.3	V
Output signal crossover voltage	V <sub>CRS</sub>		1.3		2	V
Differential input sensitivity	V <sub>DI</sub>	[(USB2+)-(USB2-)]	0.2			V
Differential input common mode range	V <sub>CM</sub>		0.8		2.5	V
High level input	V <sub>IH</sub> (USB2+/-)		2		3.6	V
Low level input	V <sub>IL</sub> (USB2+/-)		0		0.8	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Block diagram

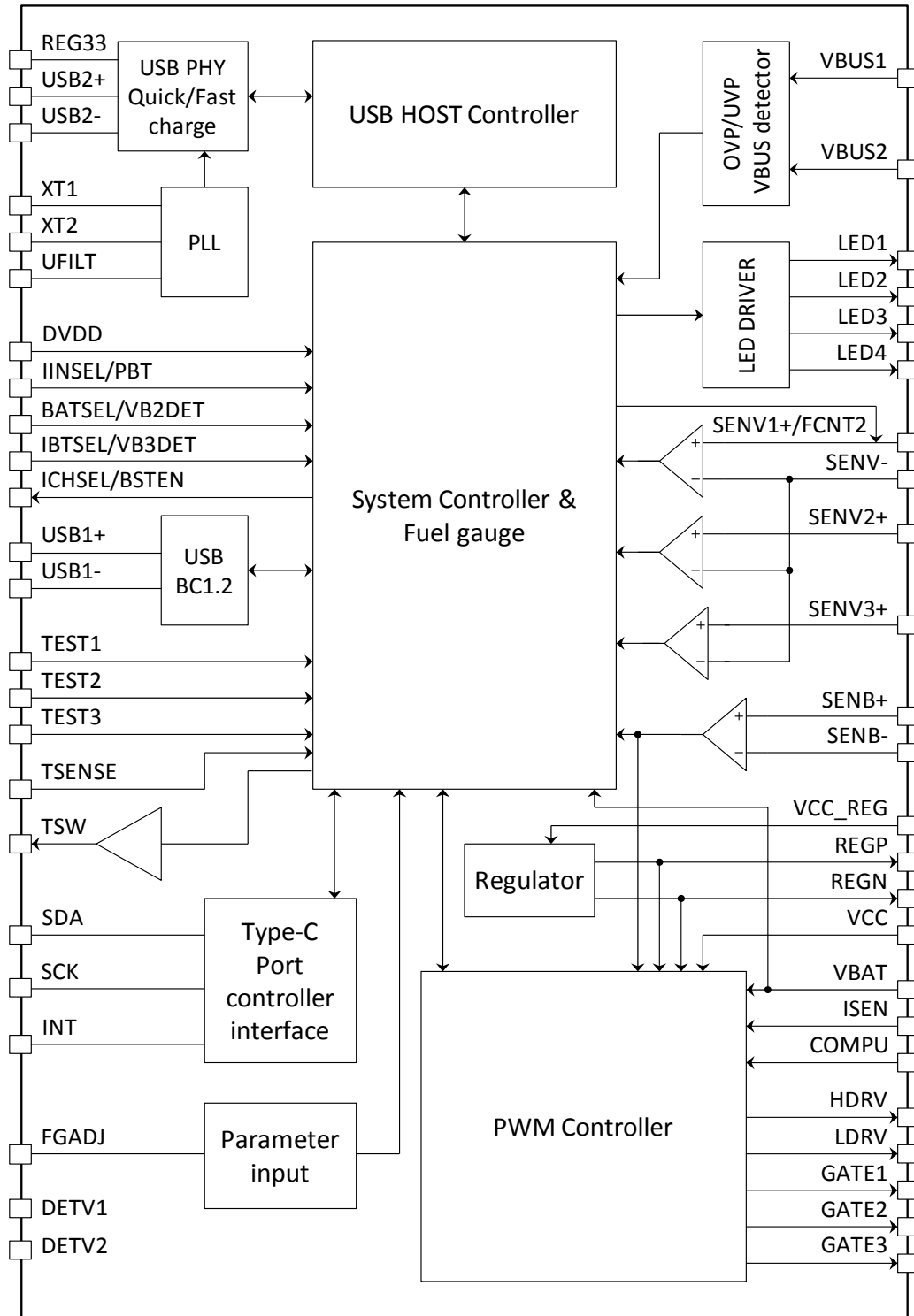


Figure 5: Block diagram

**USB Support**

This device allows 2 or 3 USB ports for Power Bank application. The USB port functions will vary by writing of prepared Firmware. The Firmware is distinguished by the Firmware number which is called FW01, FW02, FW05, and FW06.

• **FW01 (Planning)**

Micro-B input, Type-A output ×2-ch, Quick Charge 3.0 HVDCP, Boost auto start-up, External Boost-IC, Portable device communication. Displays Power Bank battery information on smartphones. USB 2.0 Full Speed Host Controller.

• **FW02 (Released)**

Micro-B input, Type-A output ×2-ch, Quick Charge 3.0 HVDCP, Boost auto start-up, External Boost-IC.

• **FW05 (Released)**

Type-C DRP, Type-A output, Quick Charge 3.0 HVDCP, Boost auto start-up, External Boost-IC.

• **FW06 (Planning)**

Supports USB-PD

The Relationship between the Firmware and the USB port functions is shown in Table 4 and Figures 6, 7, and 8. USB1+/- port of FW01/FW02 is a power sink. This port is an input for Buck charge. And it contains functions of BC1.2 and divided mode. USB2+/- port is a power source. This port is an output for Boost charge. Portable device communication and Quick Charge 3.0 are only enabled in USB2+/- port. Another power source that is Type-A (2) is boosted by an external Boost-IC. This device runs the Boost-IC when it detects the plug insertion to Type-A (2).

USB1+/- port of FW05 is fully TCPCI compliant. It is capable of controlling BC1.2 as well up to external port control IC (for USB Type-C implementations). The port can be dual-role, upward-facing, or downward-facing.

The firmware can be downloaded from the homepage of ON Semiconductor. Please refer to an application note for the writing tool.

Buck charge mode: Built-in battery charging via USB.

Boost charge mode: Charging the device from built-in battery via USB.

**Table 4 Firmware vs USB functions**

Firmware	Ports	Buck Charge	Boost Charge	USB	Portable device Communication	Quick Charge 3.0 HVDCP	Divided Mode1-3	Boost auto start-up	external Boost-IC
FW01 (Planning)	USB1+/USB1-	✓	-	Type-B	-	-	✓	-	-
	USB2+/USB2-	-	✓	Type-A (1)	✓	✓	-	✓	-
	-	-	✓	Type-A (2)	-	-	-	✓	✓
FW02 (Released)	USB1+/USB1-	✓	-	Type-B	-	-	✓	-	-
	USB2+/USB2-	-	✓	Type-A (1)	-	✓	-	✓	-
	-	-	✓	Type-A (2)	-	-	-	✓	✓
FW05 (Released)	USB1+/USB1-	✓	✓	Type-C DRP	-	✓ (Source mode)	✓ (Sink mode)	✓ (Note)	-
	-	-	✓	Type-A (2)	-	-	-	✓	✓

Note) Port control IC detects the Sink connection.

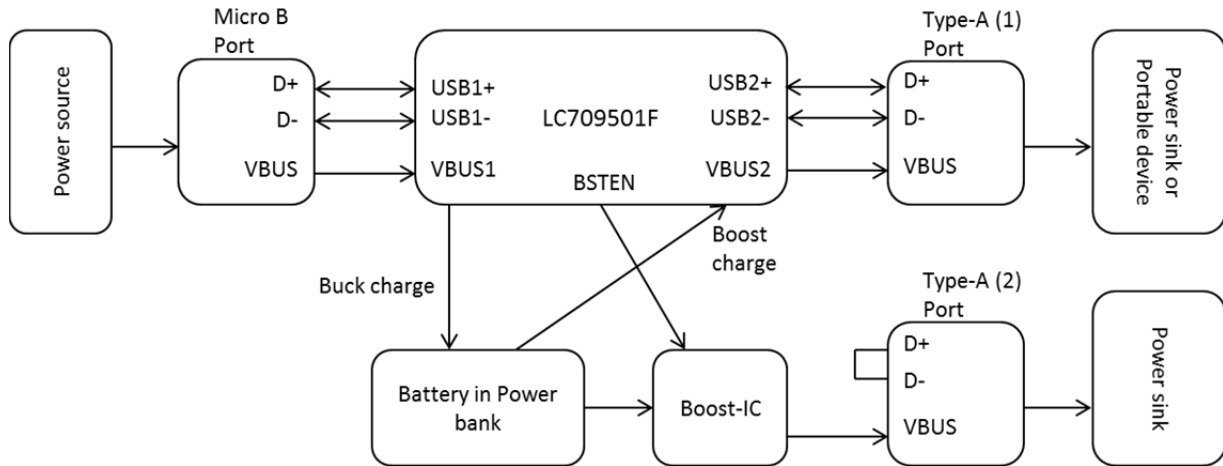


Figure 6: The function of FW01 & FW02

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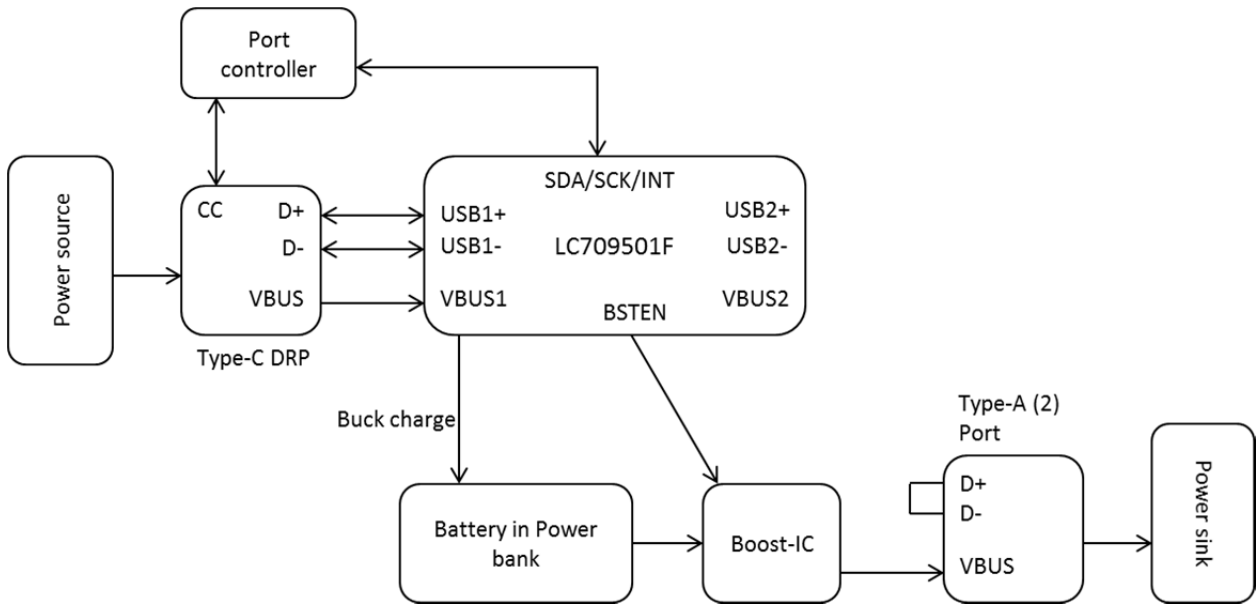


Figure 7: The function of FW05 (In case USB1+/- port is in Source)

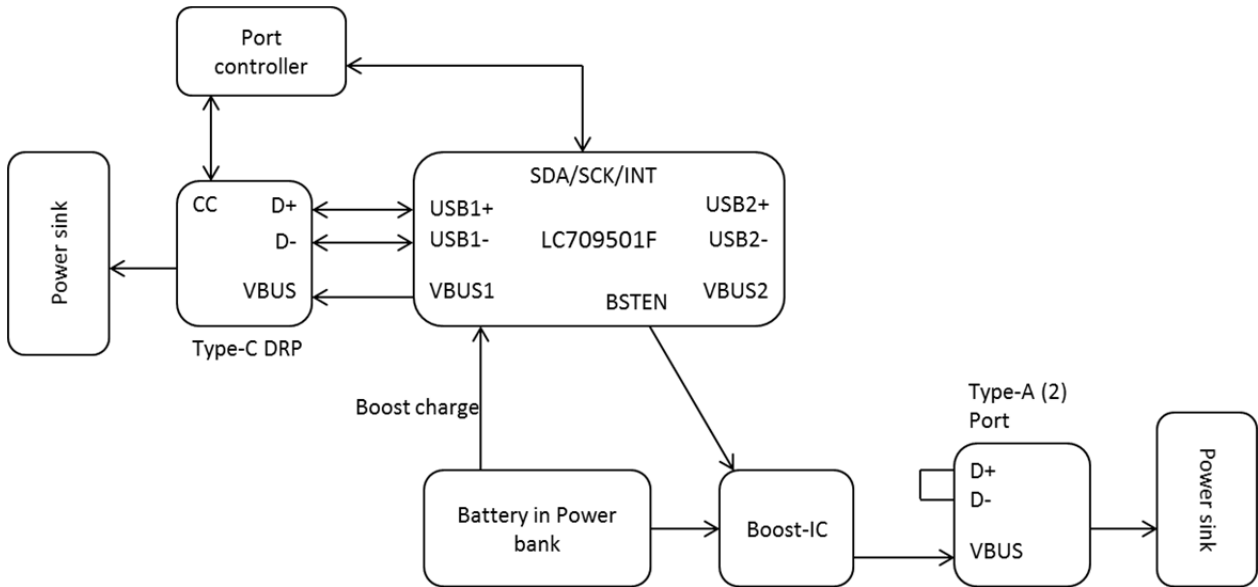


Figure 8: The function of FW05 (In case USB1+/- port is in Sink).

**Mode transition**

This device is set to a Low power mode to minimize power consumption when no USB device is connected. If this device detects connection, it transition to Operating mode.

**FW02**

In Figure 9: FW02 state diagram, when the VBUS1 rise (input) is detected and VBUS1 voltage exceeds the  $V_{BDET}$ , it transitions from Low power mode to Operating mode. Buck charge is enabled when VBUS1 voltage exceeds the  $V_{BUVP}$ , and the device will start Buck charging to the battery according to the power source supply capability. If the input plug is removed, it will transition back to Low power mode.

In the Low power mode, if the output-plug insertion is detected or the push button is pressed long, it transitions into the Operating mode to start 5 V Boost charge. At first 5 V is applied to  $V_{CC}$ , then it opens GATE to the detected plug. If the plug of External Boost-IC is connected, BSTEN is set to "HIGH" to output 5 V.

If the detected plug is Type-A (1), FW02 starts as Quick Charge 3.0 HVDCP. 9 V or 12 V or Continuous mode request is received from the portable device, the Boost voltage will automatically change according to the request. Boost charge will stop under following conditions of: a) Plug for the output is removed, b) Output current to the connected portable device falls under  $I_{BTERM}$ , c) Built-in battery voltage is judged as low, or d) Input plug is connected. If all Boost charge stops and input plug doesn't be connected, this device will transition into the Low power mode. If both the output-plugs and the input-plug are

connected, it will transition to Buck charge. Refer Table 5.

**FW05**

In Figure 10: FW05 DRP state diagram. Low power mode will transition into the Operating mode under following conditions of: a) Port control IC detects DRP is attached, or b) Connection to Type-A (2) port is detected by VB3DET, or c) Push button is pressed for long.

Figure 11 shows DRP Port control IC state diagram example. When DRP is in the unattached state, it alternates between Unattached.SRC and Unattached.SNK. It outputs  $R_p$  in the Unattached.SRC, and outputs  $R_d$  in the Unattached.SNK.  $R_p$  is set to 3.0 A @ 5 V. If the device attached to DRP is a power source, it transitions AttachWait.SNK. Then it transitions Attached.SNK after that VBUS1 voltage exceeds  $V_{BUVP}$ . This device receives the status from Port control IC to start Buck charge.

If the device connected to DRP is a power sink, it transitions AttachWait.SRC. Then it transitions Attached.SRC after that VBUS1 voltage is lower than  $V_{SAFE0V}$  and CC status is sink. This device receives the status from Port control IC to start Boost charge. Refer Table 6 according to CC status to judge that the connected device is sink.

Boost charge can be performed for DRP and Type-A (2) ports at the same time. If the output-plug is removed, or the output current decreases under  $I_{BTERM}$ , or the built-in battery voltage is judged to be low, boost charge will finish. If all Boost charge stops, this device will transition into the Low power mode. If DRP is Source mode and the other plug connection is detected, Buck charge takes priority to like FW02.

**Table 5 Connection vs charge modes**

**FW02**

Connected device			Charge mode
Type B(Sink)	Type-A (1) (Source)	Type-A (2) (Source)	
Source	-	-	Buck charge mode
Source	Sink	-	
Source	-	Sink	
Source	Sink	Sink	
-	Sink	-	Boost charge mode
-	-	Sink	
-	Sink	Sink	

**Table 5 Connection vs charge modes (continue)**

FW05

Connected device		Charge mode
Type C(DRP)	Type-A (2) (Source)	
Source	-	Buck charge mode
Source	Sink	
Sink	-	Boost charge mode
-	Sink	
Sink	Sink	

**Table 6 CC status to judge sink**

CC1	CC2	State
Open	Open	Nothing attached
Rd	Open	Enter Attached.SRC
Open	Rd	
Open	Ra	Keep AttachWait.SRC
Ra	Open	
Rd	Ra	Enter Attached.SRC
Ra	Rd	
Rd	Rd	Keep AttachWait.SRC
Ra	Ra	

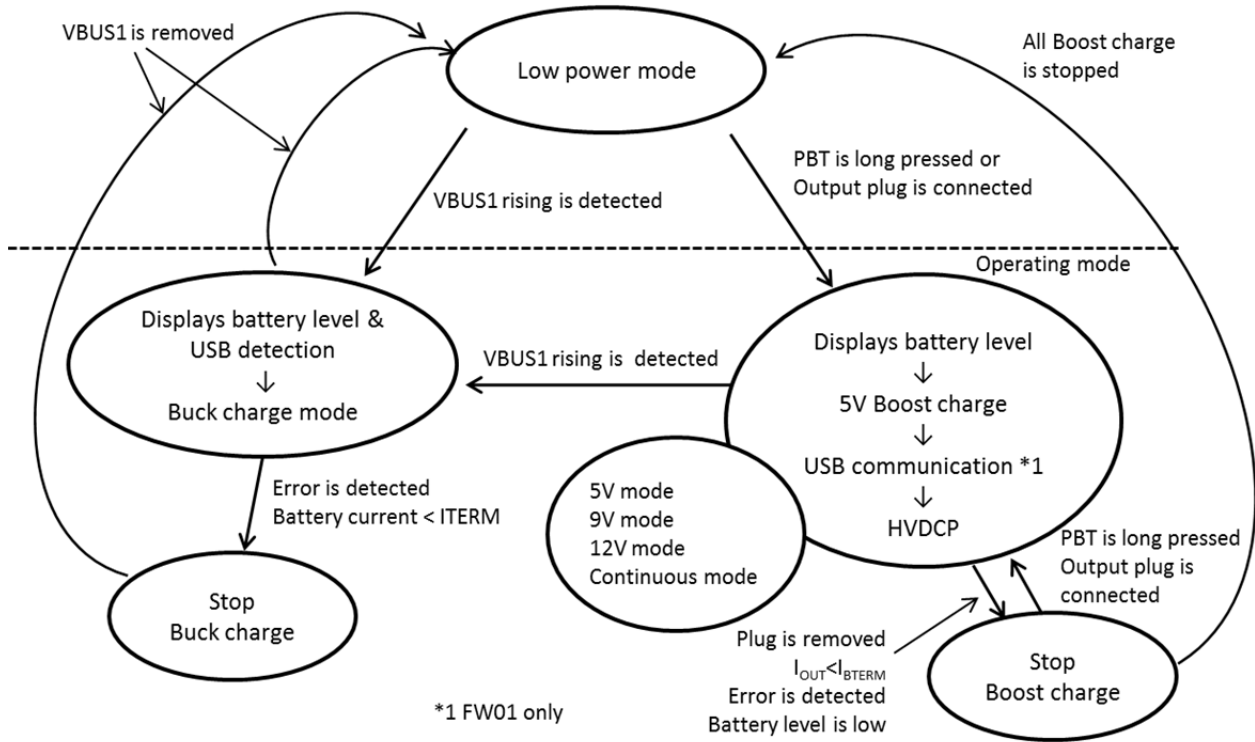


Figure 9: FW02 state diagram

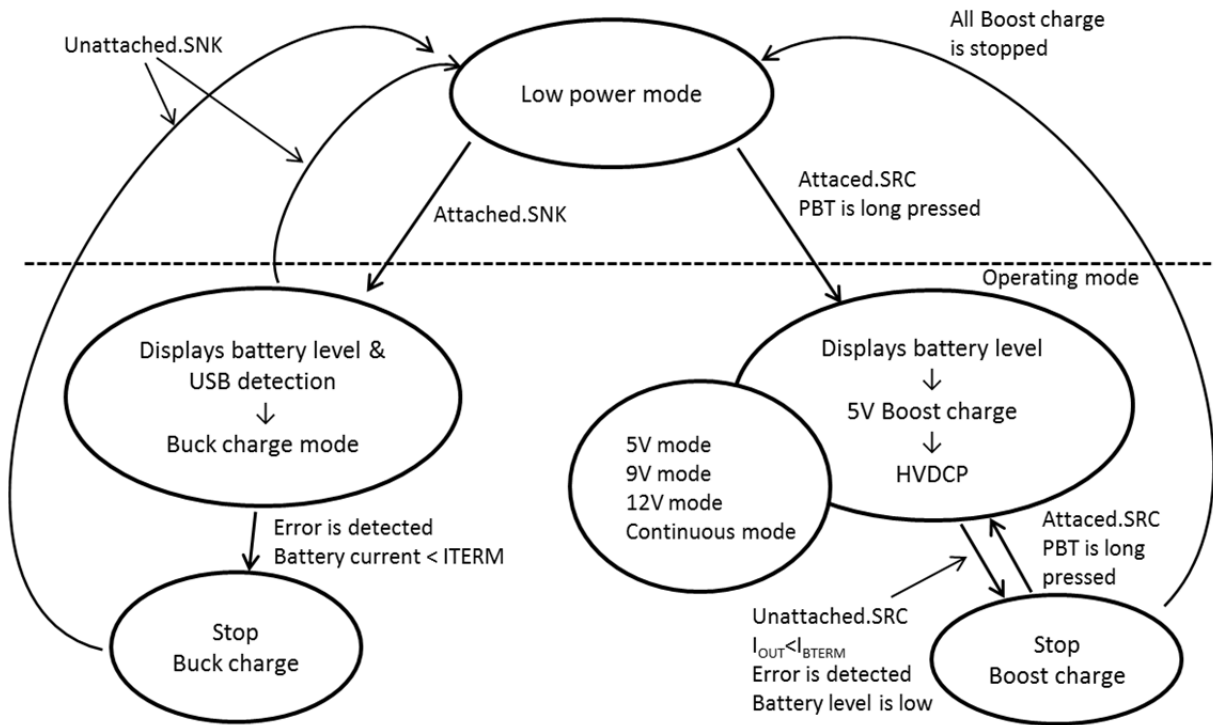


Figure 10: FW05 (DRP) state diagram

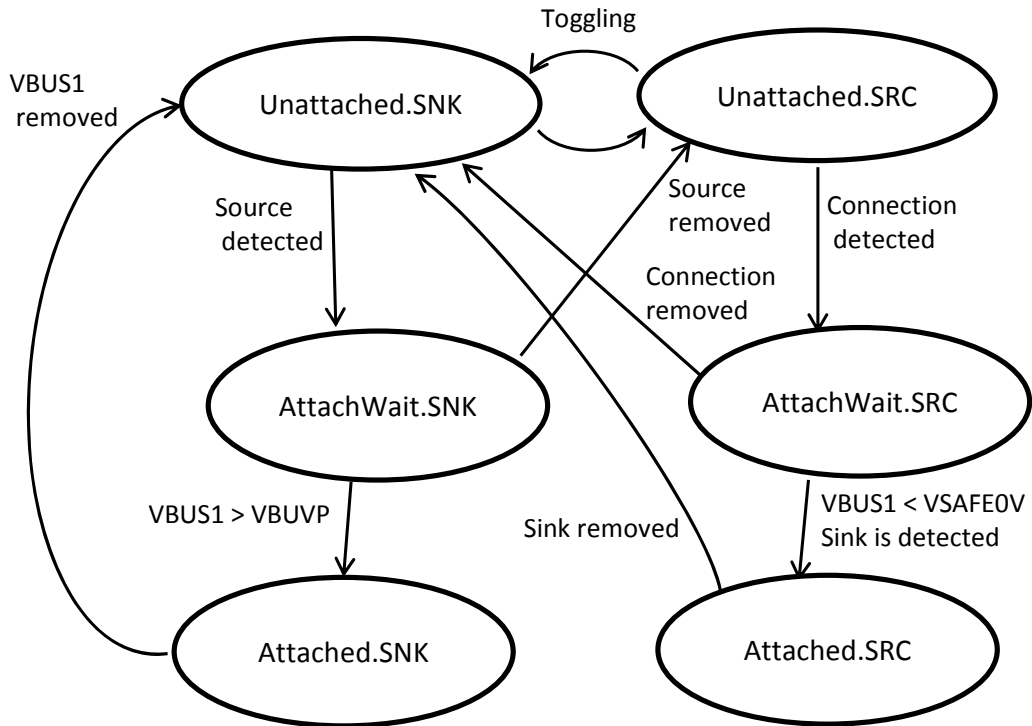


Figure 11: DRP Port control IC state diagram example

## Buck charge

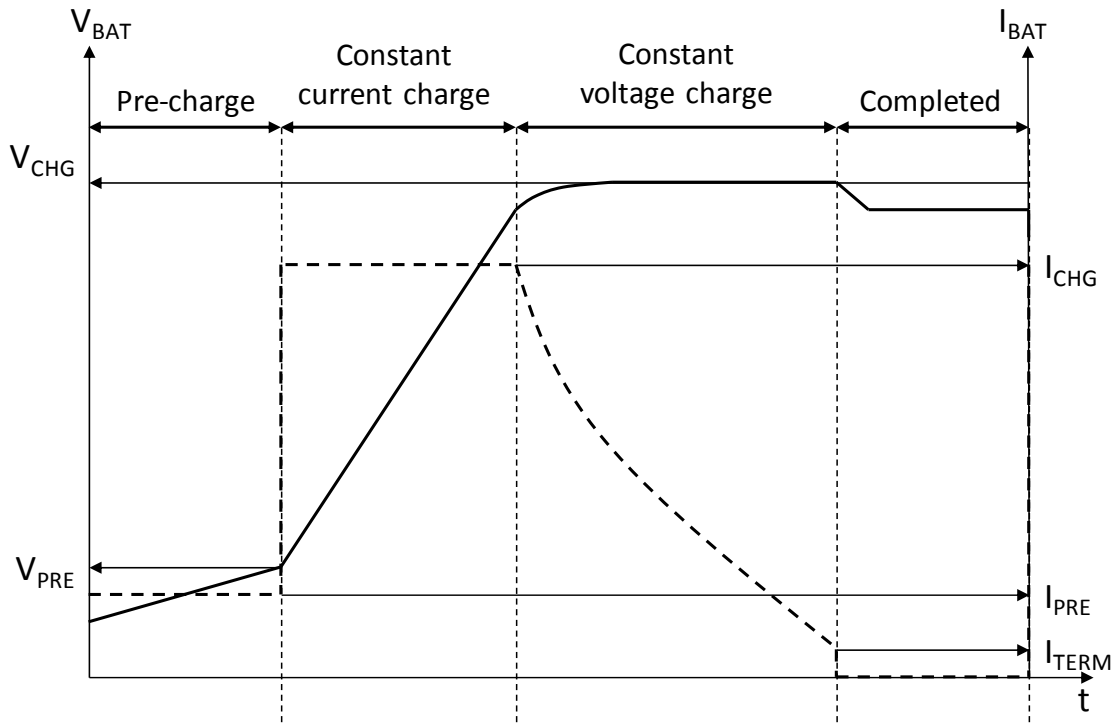


Figure 12: Buck charge states

The buck charge is configured by three states: pre-charge, constant current charge, and constant voltage charge. Figure 12 shows the flow of battery charge.

### Pre-charge mode

Pre-charge is executed when battery voltage is below  $V_{PRE}$  at the start of buck charge. In this case charging current is limited by  $I_{PRE}$ . If battery voltage exceeds  $V_{PRE}$ , it transitions to the constant current charge mode.

### Constant current charge mode

Charging with constant current. Charging current is limited by  $I_{CHG}$  and input current from USB port. (Refer “Input over current protection”) When battery voltage reaches  $V_{CHG}$ , it transitions to the Constant voltage charge mode.

### Constant voltage charge mode

Charging with constant voltage. Charging current will decrease as it gets closer to the full charge. When charge current decreases to the termination current, the charge operation will complete.

The termination current is set by  $I_{TERM}$ .

### Safety timer

If the continuous battery charging time exceeds  $T_{C_{MAX}}$ , it will force-quit the charging operation. It will start charging again by either detecting Re-connect at the supply source or push button is pressed long.

### Buck charge condition vs temperature

This device changes charge voltage and charge current according to the battery temperature measured by the external thermistor. Refer Figure 13. If the temperature exceeds  $T_{WARM}$ , Termination Battery Voltage decreases in  $V_{CHGH}$ . If the temperature exceeds  $T_{HOT}$ , it will stop charging. If the temperature drops below  $T_{COOL}$ , charge current will become a half of the constant charge current  $I_{CHG}$  value. If the temperature drops below  $T_{COLD}$ , charge stops. Buck charge does not re-start until the supply source is unplugged/plugged if even once the temperature is over  $T_{HOT}$  or below  $T_{COLD}$ .



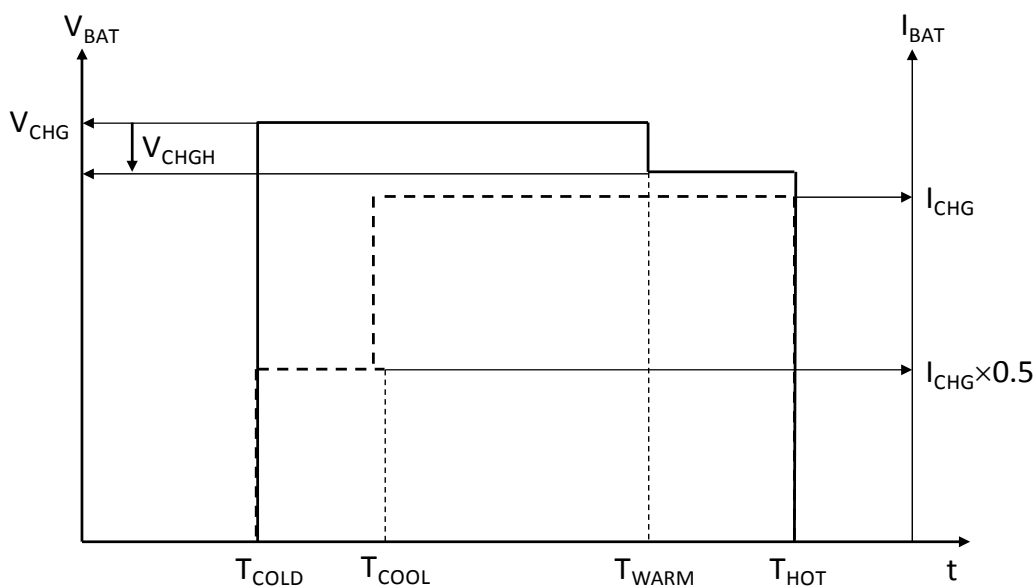


Figure 13: Charge voltage & current & battery temperature

## Boost charge

### Boost auto start-up

This device can detect USB Type-A plug insertion using VB2DET/VB3DET pins. Battery voltage through diode is supplied to VBUS. This device constantly monitors the VBUS voltage using VB2DET/VB3DET pins and judges a plug insertion from the voltage shift.

In the case of USB Type-C, Port control IC will detect the plug insertion. This device can accept the interrupt from Port control IC. If a plug insertion is detected and Buck charge does not run, Boost charge will start.

### Boost manual start-up

When the external push button is depressed for more than  $T_{LBOT}$  the device will wake up and begin Boost charge.

### End of boost charge

Boost charge to VBUS that the output current falls below  $I_{BTERM}$  will stop. If all boost charge stops, this device transitions to the Low power mode. It is necessary that the stopped VBUS are unplugged or Push button is long pressed for re-start of boost charge.

### Boost charge prohibition for empty battery

When the battery level is 0% or the no-load battery voltage is under 3.3 V, boost charge will not start. If the battery level becomes 0% or the battery voltage drops under 3 V while executing the boost charge, boost charge will stop and transition to the Low power mode.

### Boost charge vs temperature

This device stops Boost charge according to the battery temperature measured by the external thermistor. If the

temperature exceeds  $T_{HOT2}$  or drops below  $T_{COLD2}$ , it will stop Boost charge to all VBUS and transition to the Low power mode.

## Protection

### Thermal shut down

This device has a built-in thermometer. If device's internal temperature exceeds the THD, it will stop all Buck charge and Boost charge. It cannot restart charging if device's internal temperature is above THD.

### Over/Under voltage protection

VCC pin can detect under voltage, VBAT pin can detect over-voltage, VBUS1 and VBUS2 can detect over-voltage as well as under-voltage. It will stop charging to the port that over-voltage or under-voltage is detected.

### Exceeding the output current limit

In boost charge mode, if the output current exceeds  $I_{OUTMAX}$ , it will stop boost charge to the VBUS.

### Input over current protection

The set maximum input current limits the charge current in Buck charge mode. This device controls the charge current so that it doesn't exceed the limit.

The maximum input current limit will be the lowest value of the following three:

- $I_{INMAX}$ : Value determined by the Buck mode
- $I_{CHG}$ : Constant Charge Current
- USB Detection Max current (Refer to Table 9)

**Interface**

**Push button**

The IINSEL/PBT pin can be connected to an external push button and must be pulled-down by an external resistor when inactive. When the IINSEL/PBT pin is driven to a logic level high (“H”) by pressing the push button, the device recognizes that the push button was pressed. Furthermore if the “H” level time exceeds the  $T_{LBOT}$  value, it is recognized as long-press, and if it is below the  $T_{LBOT}$  value, it is recognized as short-press.

**USB HOST (FW01: Planning)**

This device has 2 host controller ports (USB2+/-). They support Full-Speed (12 Mbps) operation and 4 transfer types (control, bulk, interrupt, and isochronous transfer).

Table 7 shows the OS and their versions that are supported by this device.

**Table 7 USB HOST OS Version**

OS	Version
Android	4.1.x/4.2.x/4.3.x (Jelly Bean), 4.4.0-4.4.4 (KitKat), 5.0.0-5.0.2/5.1.x (Lollipop)

**Power Bank information (FW01: Planning)**

Through USB HOST communication, this device can transfer the data shown in Table 8 to a device.

The “Cycle count” is used to detect the number of

**Table 8 Power Bank information**

Parameter	Range	Unit	Description
Battery temperature	0x09E4 to 0x0D04 (-20.0°C to 60.0°C)	0.1K	Displays battery temperature.
Battery level	0x0000 to 0x0064 (0% - 100%)	%	Displays battery remaining level.
Cycle count	0x0000 - 0xFFFF	Cycle	Displays the number of charging and discharging cycles of a battery

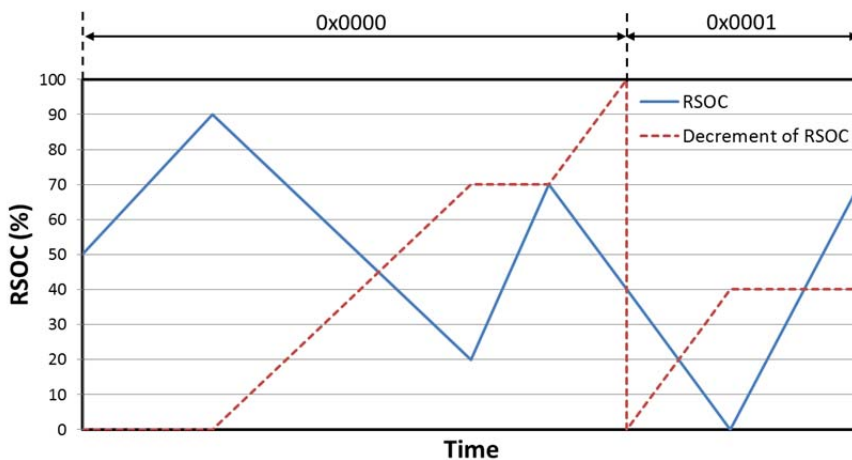


Figure 15: Number of cycle

charging and discharging cycles of a battery. It is counted as “1” when the total decrement of battery level reaches 100%. Please refer to Figure 15.

**Crystal oscillation (FW01: Planning)**

This device has oscillation ports for Crystal resonator. The characteristics of sample oscillator circuit is shown in Figure 14.

A clock generated by this resonator is used for USB HOST communication. PLL and regulator are built-in for this function. Appropriate capacitors must be connected to REG33 and UFILT pins for these circuits.

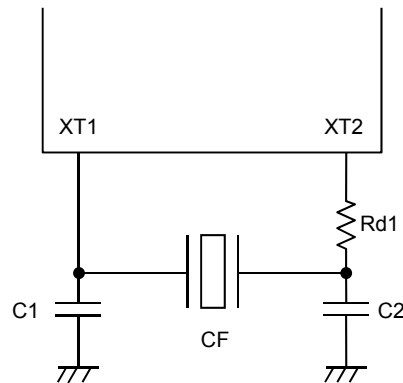


Figure 14: Crystal Oscillator Circuit

### Single-master I<sup>2</sup>C

This device has single-master I<sup>2</sup>C with 1 port that can support up to 400 kHz frequency. I<sup>2</sup>C can be connected to a Port control IC. It also has INT pin to accept interrupts from the Port control IC.

### USB Detection function

USB1+/- has USB Detection function. This function limits input current in Buck charge mode. The supported modes are shown in Tables 9. If the connected device is DCP, the limit is defined by only I<sub>INMAX</sub> or I<sub>CHG</sub>.

**Table 9 USB1+/- Detectable mode**

Mode	Maximum charge current
SDP	0.5 A
CDP	1.5 A
DCP	-
HVDCP	-
Divided Mode 1	1 A
Divided Mode 2	2.1 A
Divided Mode 3	2.4 A

### Quick Charge 3.0 HVDCP

This device supports Quick Charge 3.0 HVDCP Class A. USB2+/- ports receives the request of Quick Charge 3.0 from Portable device. USB2+ and USB2- is shorted with RDCP\_DAT. If the negotiation between Portable device and this device is successful, this device opens USB2+ and USB2-, and D- is pulled down with RDM\_DWN. It monitors D+ and D- voltage and change the output voltage according to D+ and D- status that is the Potable device request. (Table 10) The output range is shown in Figure 16.

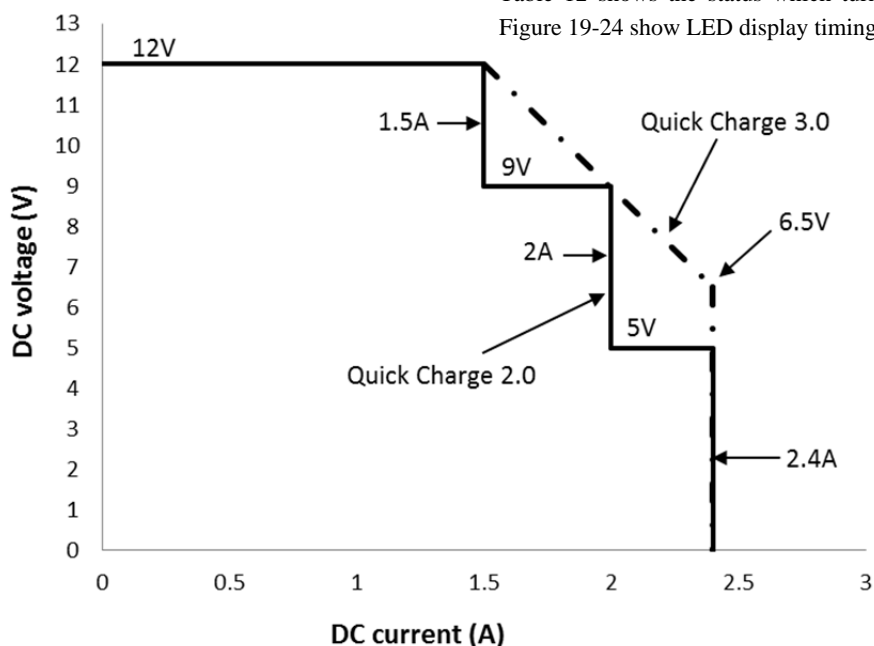


Figure 16: Quick Charge 2.0 / 3.0 HVDCP operating range

**Table 10 D+/- vs Output voltage**

Portable device		Output voltage
D+	D-	
0.6 V	0.6 V	12 V
3.3 V	0.6 V	9 V
0.6 V	3.3 V	Continuous mode
3.3 V	3.3 V	Previous voltage
0.6 V	GND	5 V

### LED

#### Battery level

A short-press of the push button will turn on LED drive port to indicate the battery level for T<sub>LBAT</sub> period. At this time, LEDs light up in the order from LED1 with T<sub>LDELAY</sub> delay after each light up. Table 11 shows the relationship between battery levels and LEDs. Figure 17 and 18 show the timing.

**Table 11 Battery level vs LEDs**

LED	Battery level
LED1-4 on	76%-100%
LED1-3 on	51%-75%
LED1-2 on	26%-50%
LED1 on	11%-25%
LED1 flashing	1%-10%
LED off	0%

#### Status indicator

Table 12 shows the status which turn on LED drive port. Figure 19-24 show LED display timing in each status.

Table 12 Status vs LED timing

Status	LED timing	Condition
Buck charge start	Figure 19	VBUS1 plug insertion is detected, and Buck charge is started.
Boost charge start	Figure 20	Output plug insertion is detected or push button is depressed, and Boost charge is started.
Over temperature in Buck charge	Figure 21	In Buck charge temperature which is measured by thermistor exceeds $T_{HOT}$ or $T_{COLD}$ .
Over temperature in Boost charge	Figure 22	In Boost charge temperature which is measured by thermistor exceeds $T_{HOT2}$ or $T_{COLD2}$ .
Thermal shutdown	Figure 23	Thermal shutdown occurs.
Thermistor disconnection	Figure 24	The disconnection of thermistor is detected.

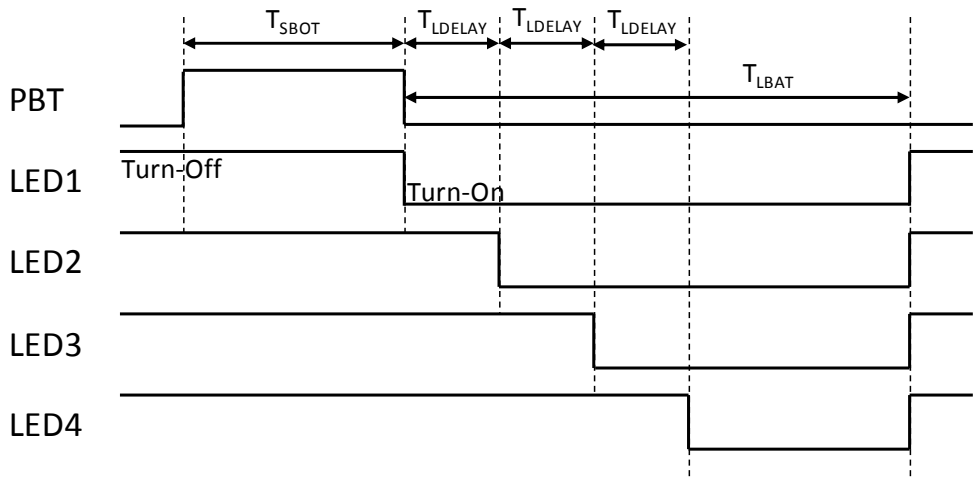


Figure 17: LED display timing chart of battery level by a short-press (Battery level: 76-100%)

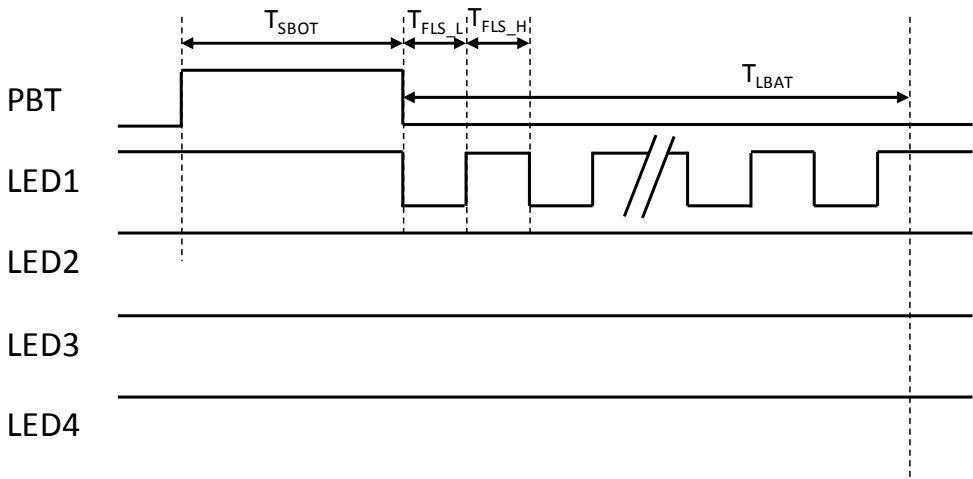


Figure 18: LED display timing chart of battery level by a short-press (Battery level: 1-10%)

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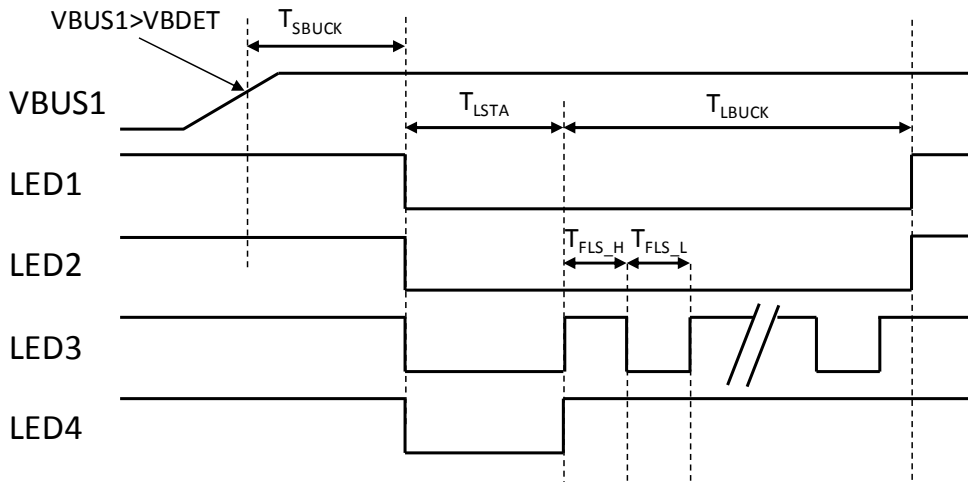


Figure 19: LED display timing chart at Buck charge start (Battery level: 51-75%)

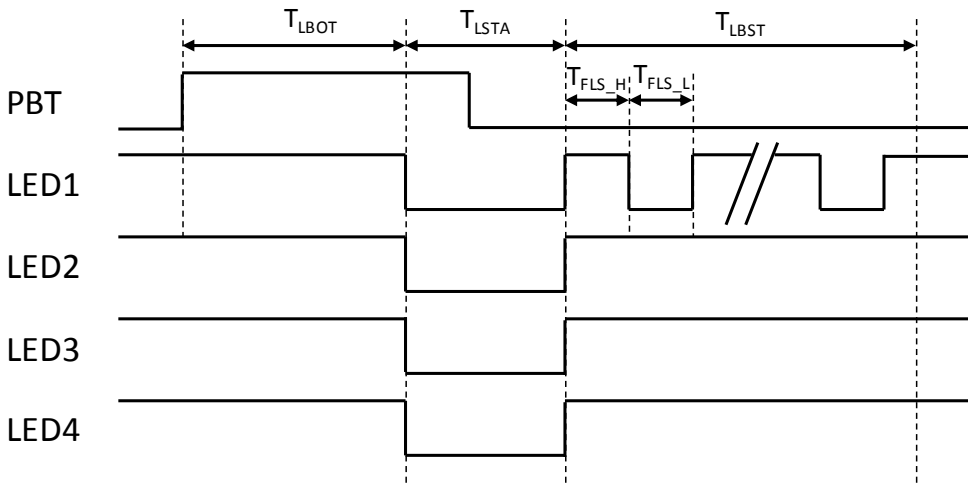


Figure 20: LED display timing chart at Boost charge start by a long-press

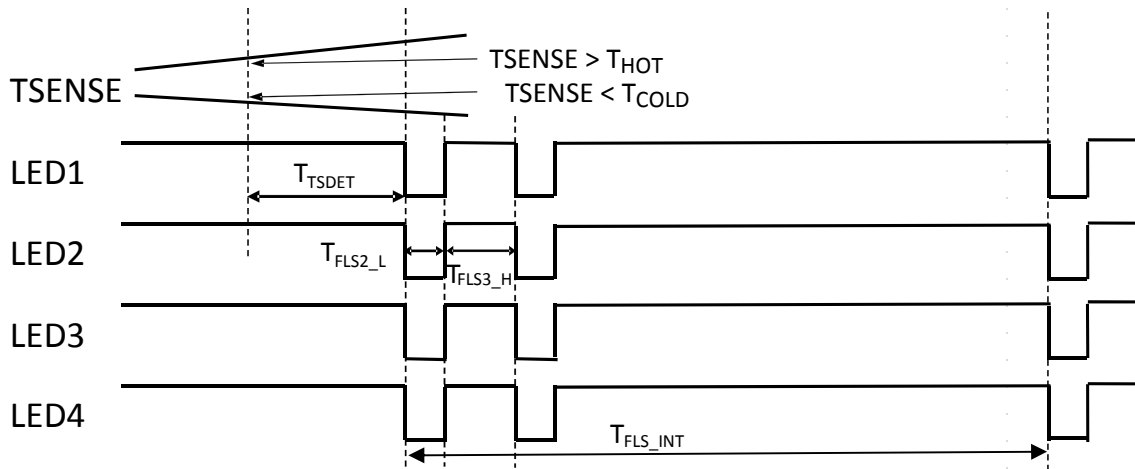


Figure 21: LED display timing chart when over temperature is detected in Buck charge

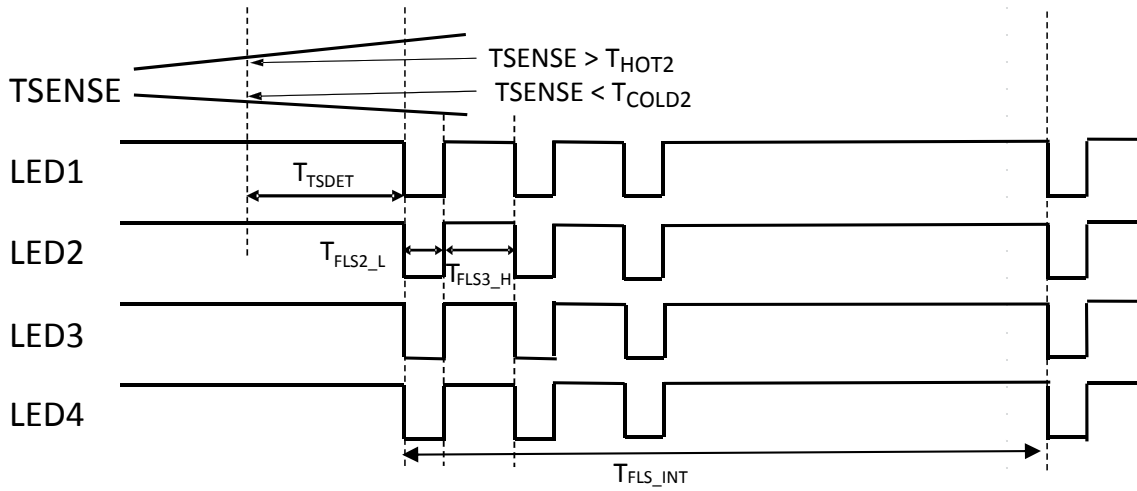


Figure 22: LED display timing chart when over temperature is detected in Boost charge

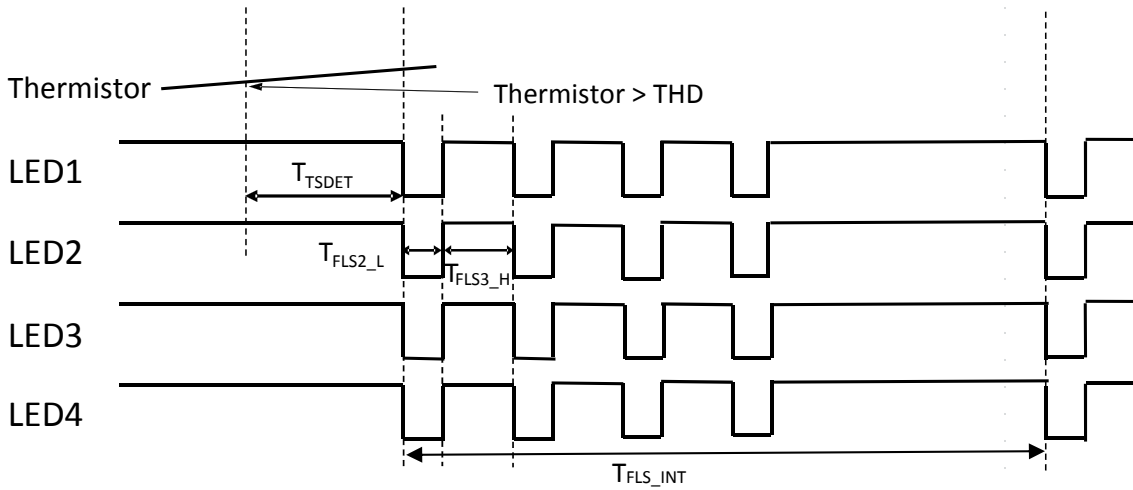


Figure 23: LED display timing chart when thermal shutdown occurs

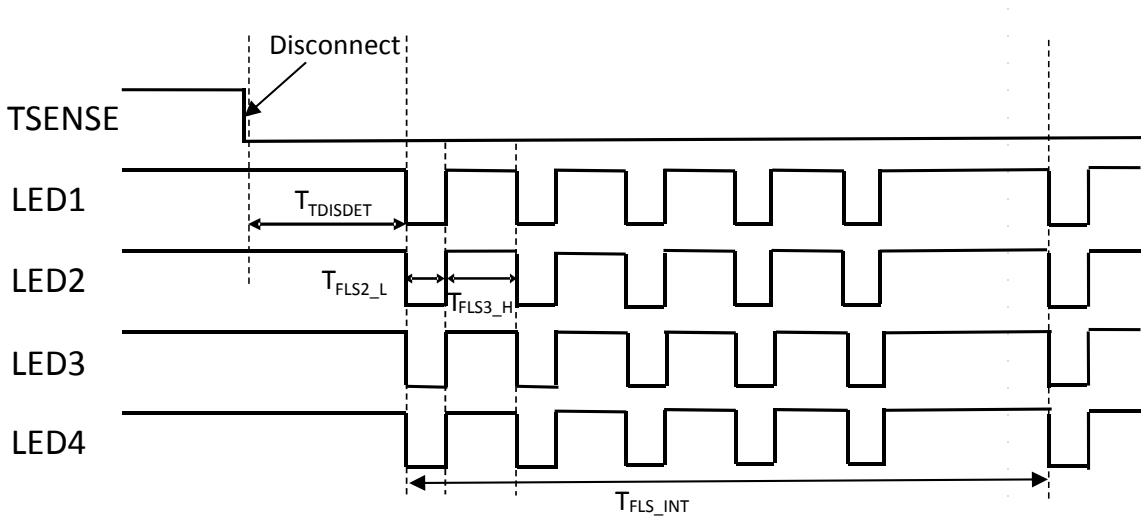


Figure 24: LED display timing chart when the disconnection of thermistor is detected.

## Boost Efficiency

Appropriate parts of converter and PWM frequency for the maximum boost power can be selected. Table 13 shows an example. Figure 25, 26 and 27 show the result of Boost Efficiency for the example. Refer an application note for the result of the other example.

**Table 13 Parts example around converter**

Inductor	L	PWM freq.	Switching FET
Coilcraft	2.2 $\mu$ H	300 kHz	ECH8310 x 2 NTTFS4H05N x 2

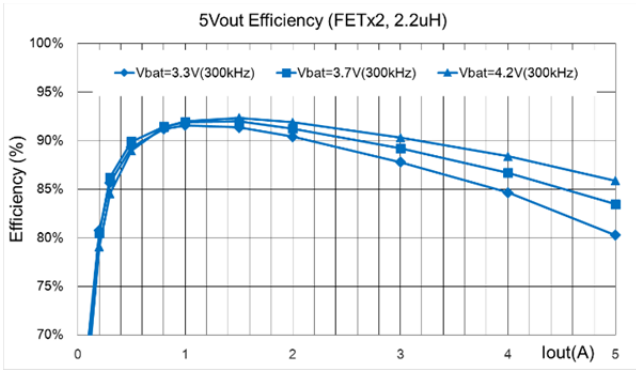


Figure 25: Boost efficiency (VBAT = 3.7 V, VOUT = 5 V)

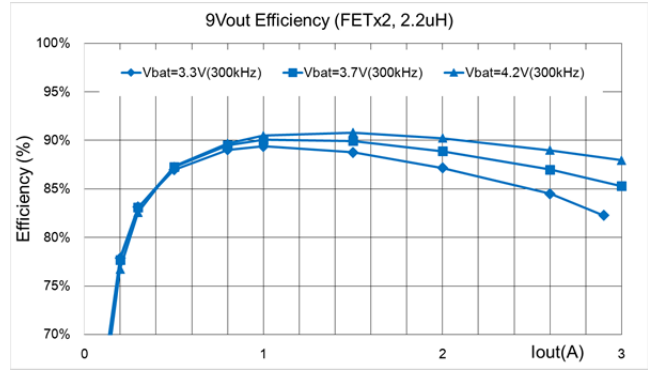


Figure 26: Boost efficiency (VBAT = 3.7 V, VOUT = 9 V)

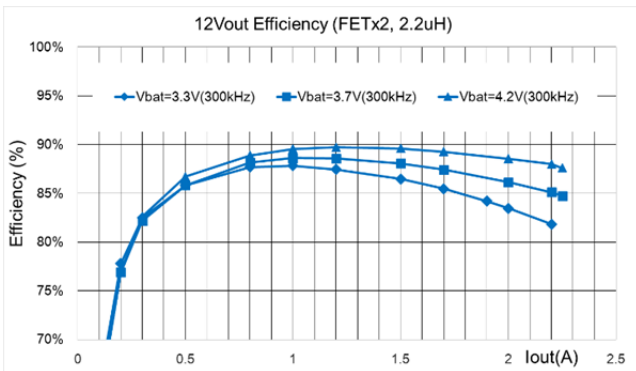


Figure 27: Boost efficiency (VBAT = 3.7 V, VOUT = 12 V)

## Adjustable parameters

This device can adjust the parameters with Port configuration or Firmware configuration. Adjustable parameters with Port configuration are limited. Firmware configuration can adjust more parameters than Port configuration.

### Port configuration

Port configuration can adjust parameters according to the resistance of connected resistor to the dedicated port. Refer Table 14-15. The parameters which can't set in Port configuration follow to the default value of Firmware configuration.

### Firmware configuration

Firmware configuration change the Firmware to adjust parameters. Refer Table 16 about adjustable parameters. When Firmware configuration is implemented, FGADJ port resistor is invalid. Please contact ON Semi-conductor about how to change Firmware.

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**Table 14 Port configuration**

Parameter	Symbol	Unit	Parameter range	Description
Design capacity	–	mAh	2000 - 24400	Sets the Design capacity of battery. It follows the resistance of connected resistor to the FGADJ port. Refer Table 13. It is used for Battery level gauging.
Constant charge current	I <sub>CHG</sub>	mA	2000 - 6000	Constant charge current is equal to 1C current of set Design capacity. If the current exceeds the range, the lower or upper value is set. (ex. Design capacity = 4,000 mAh -> Constant charge current = 4,000 mA, Design capacity = 10,000 mAh -> Constant charge current = 6,000 mA)
Pre-charge current	I <sub>PRE</sub>	mA	200 - 500	Pre-charge current is equal to 0.07C current of set Design capacity. If the current exceeds the range, the lower or upper value is set. (ex. Design capacity = 4,000 mAh -> Pre-charge current = 280 mA, Design capacity = 2,000 mAh -> Pre-charge current = 200 mA)
Termination current	I <sub>TERM</sub>	mA	200 - 800	Termination current is equal to 0.05C current of set Design capacity. If the current exceeds the range, the lower or upper value is set. (ex. Design capacity = 4,000 mAh -> Termination current = 200 mA, Design capacity = 20,000 mAh -> Termination current = 800 mA)

**Table 15 Resistance vs Design capacity in Port configuration**

Resistance (kΩ)	Design capacity (mAh)	Resistance (kΩ)	Design capacity (mAh)	Resistance (kΩ)	Design capacity (mAh)	Resistance (kΩ)	Design capacity (mAh)
4.7	2000	18	4100	68	8600	270	17800
5.6	2200	22	4600	82	9500	330	19800
6.8	2400	27	5100	100	10600	390	22000
8.2	2700	33	5600	120	11700	470	24400
10	3000	39	6300	150	13000		
12	3300	47	6900	180	14500		
15	3700	56	7700	220	16100		

**Table 16 Firmware configuration**

Parameter	Symbol	Unit	Parameter range	Default value	Description
Battery Profile	–	mV	4200 or 4350	4200	Select either 4.2 V or 4.35 V Termination Battery Voltage.
Design capacity	–	mAh	2000 - 24400	9600	
Termination boost current	I <sub>BTERM</sub>	mA	50 - 1000	200	
VBUS under voltage detection	V <sub>BUVP</sub>	mV	4400 - 4750	4400	
Maximum output current (V <sub>out</sub> ≤ 7.5 V)	I <sub>OUTMAX</sub>	mA	1500 - 3000	3000	
Maximum output current (7.5 V < V <sub>out</sub> ≤ 10.5 V)	I <sub>OUTMAX</sub>	mA	1500 - 3000	2300	
Maximum output current (10.5 V < V <sub>out</sub> )	I <sub>OUTMAX</sub>	mA	1500 - 2500	1800	
Maximum input current	I <sub>INMAX</sub>	mA	1500 - 3000	2400	FW02: For Micro-B input
				3000	FW05: For Type-C input
Pre-charge current	I <sub>PRE</sub>	mA	200 - 500	400	
Termination current	I <sub>TERM</sub>	mA	200 - 800	288	
Continuous battery charging time	T <sub>CMAX</sub>	min	120 - 1440	900	
Constant charge current	I <sub>CHG</sub>	mA	1000 - 6000	3000	
Constant B	–	K	2600 - 4700	3300	Set the B-constant of NTC thermistor. Refer the specification of thermistor to fix the value.



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## BILL OF MATERIAL

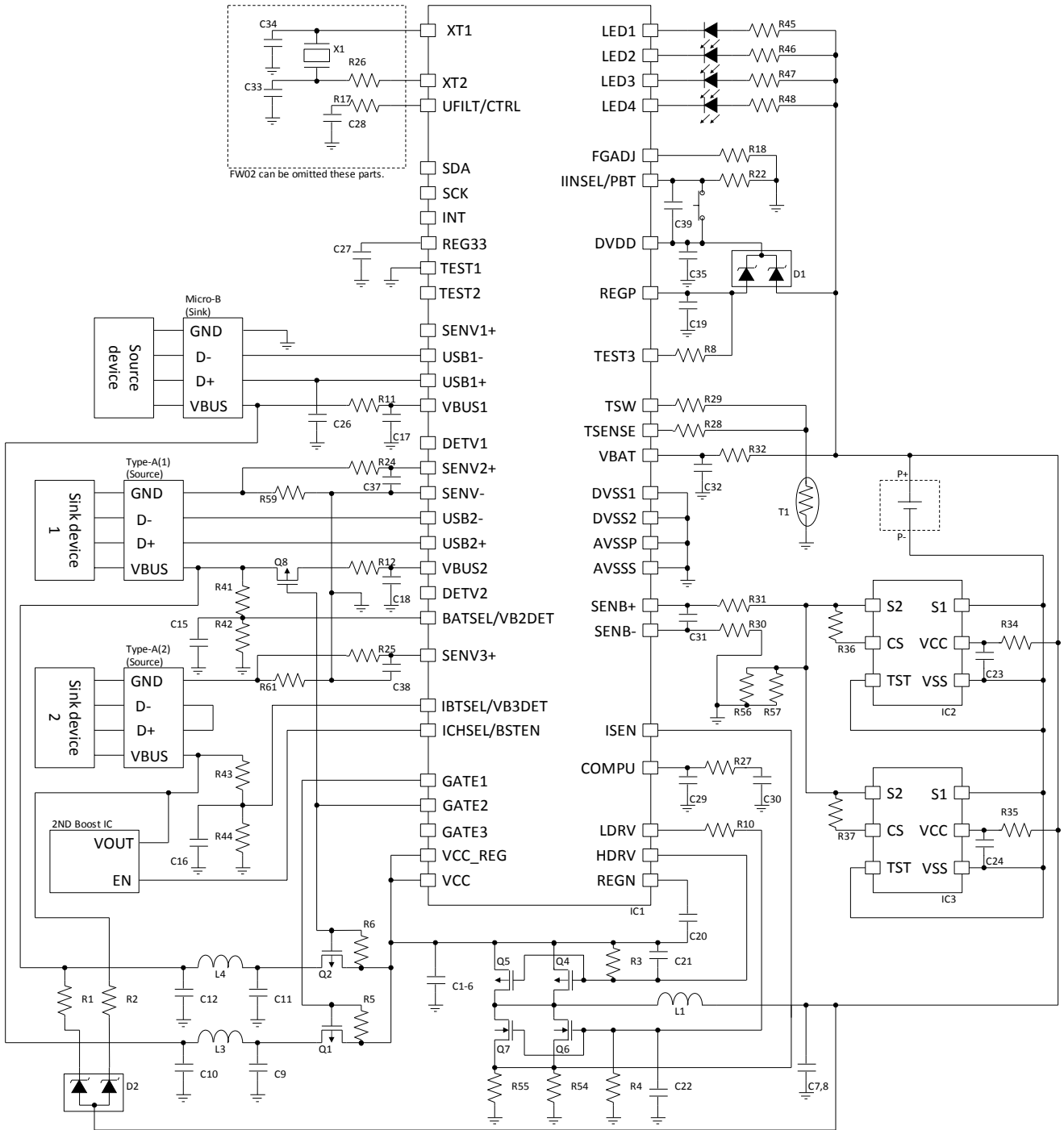


Figure 28: Firmware: FW01/FW02 Parts example

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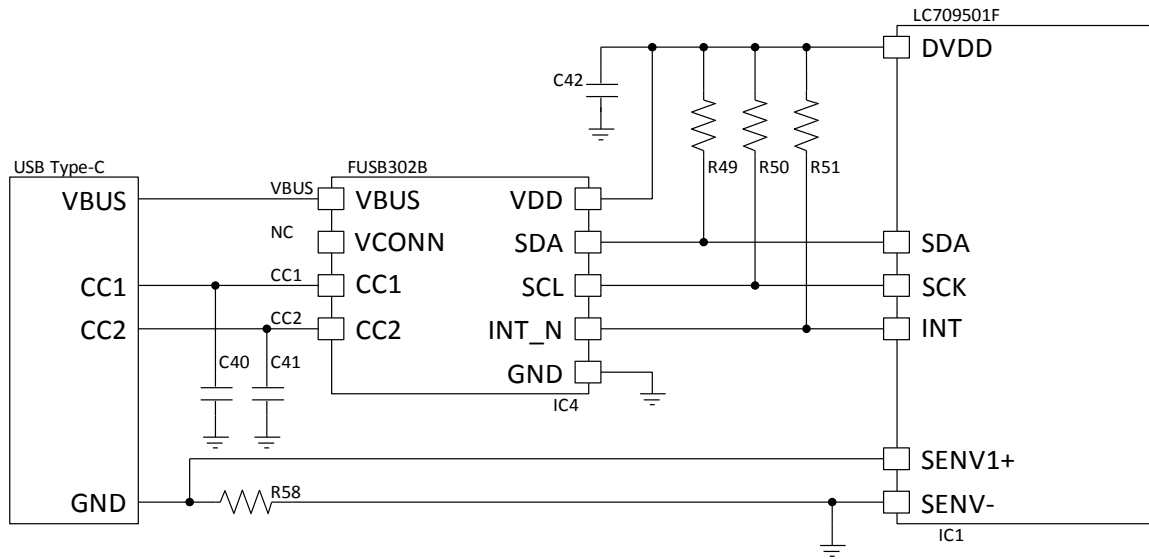


Figure 29: Firmware: FW05 Parts example around Port control IC

## LC709501F

Designator	Description	Value	Tolerance	Manufacturer	Manufacturer Part Number
IC1	Charge control LSI	-	-	ON Semiconductor	LC709501F
IC2, 3	Lib Protection	-	-	ON Semiconductor	LC06111TMT
IC4	Port Control IC	-	-	ON Semiconductor	FUSB302B
Q6, 7	Nch FET	-	-	ON Semiconductor	NTTFS4H05N
Q8	Pch FET	-	-	ON Semiconductor	MCH3375
Q1, 2, 4, 5	Pch FET	-	-	ON Semiconductor	ECH8310
D1	Schottky diode (Note 1)	-	-	ON Semiconductor	BAT54CL
D2	Schottky diode (Note 1)	-	-	ON Semiconductor	BAT54AL
L1	INDUCTOR COIL	2.2 $\mu$ H	-	Coilcraft	XAL7070-222MEC
L3, 4	Ferrite Bead	30 $\Omega$	-	MURATA	BLM21PG300SN1
X1	12 MHz X'tal OSC	12 MHz	-	RIVER ELETEC	FCX-05
T1	NTC Thermistor	10 k $\Omega$		SEMITEC	103JT-025
C21, 22	Ceramic Capacitor 16 V	1 p			
C33, 34	Ceramic Capacitor 10 V	8 p	-		
C40, 41	Ceramic Capacitor 10 V	390 p			
C39	Ceramic Capacitor 10 V	1000 p	-		
C29	Ceramic Capacitor 16 V	1000 p			
C30	Ceramic Capacitor 16 V	22000 p	-		
C36-38	Ceramic Capacitor 10 V	0.01 $\mu$			
C23, 24, 31	Ceramic Capacitor 10 V	0.1 $\mu$			
C10,12, 15, 16	Ceramic Capacitor 16 V	0.1 $\mu$			
C19, 26, 27, 32, 35, 42	Ceramic Capacitor 10 V	1 $\mu$	-		
C17, 18, 20	Ceramic Capacitor 16 V	1 $\mu$	-		
C28	Ceramic Capacitor 10 V	2.2 $\mu$	-		
C1-6, 9, 11	Ceramic Capacitor 16 V	22 $\mu$		MURATA	GRM32EB31C226ME16
C7, 8	Ceramic Capacitor 10 V	47 $\mu$		MURATA	GRM32ER61C476KE15
R11, 12, 17, 23-25, 28, 30-32	Chip resistor	100 $\Omega$	$\pm$ 5%		
R45-48	Chip resistor	330 $\Omega$	$\pm$ 5%		
R26, 36, 37	Chip resistor	1 k $\Omega$	$\pm$ 5%		
R27	Chip resistor	2.2 k $\Omega$	$\pm$ 5%		
R8, 29, 49-51	Chip resistor	10 k $\Omega$	$\pm$ 5%		
R22	Chip resistor	51 k $\Omega$	$\pm$ 5%		
R3, 4	Chip resistor	100 k $\Omega$	$\pm$ 5%		
R1, 2	Chip resistor	150 k $\Omega$	$\pm$ 5%		
R42, 44	Chip resistor	180 k $\Omega$	$\pm$ 1%		
R5, 6	Chip resistor	510 k $\Omega$	$\pm$ 5%		
R41, 43	Chip resistor	910 k $\Omega$	$\pm$ 1%		
R18	Chip resistor	4.7 k $\Omega$ - 470 k $\Omega$	$\pm$ 1%		
R54-57	Chip resistor 1 W	10 m $\Omega$	$\pm$ 1%	Panasonic	ERJ8BWFR010V
R58, 59, 61	Chip resistor 1 W	20 m $\Omega$	$\pm$ 1%	Panasonic	ERJ8BWFR020V

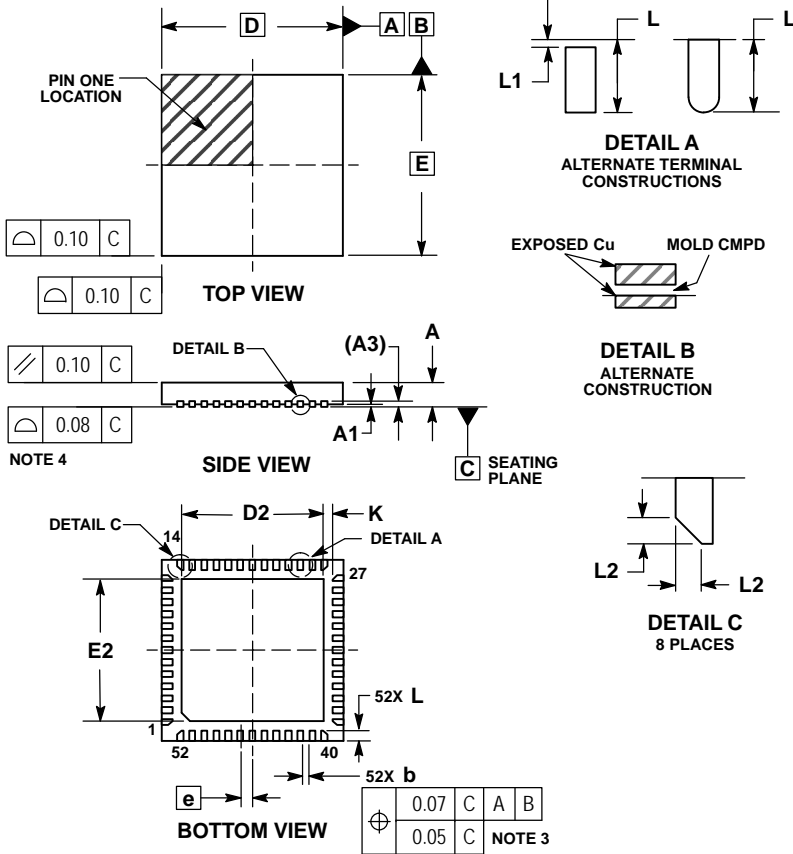
(Note 1) Forward voltage of Schottky diode must be under 0.3 V with 5 mA at 25°C.

# LC709501F

## PACKAGE DIMENSIONS

unit : mm

QFN52 6x6, 0.4P  
CASE 485BE-01  
ISSUE B

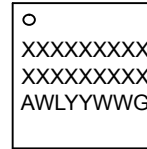


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.60	4.80
E	6.00 BSC	
E2	4.60	4.80
e	0.40 BSC	
K	0.30 REF	
L	0.25	0.45
L1	0.00	0.15
L2	0.15 REF	

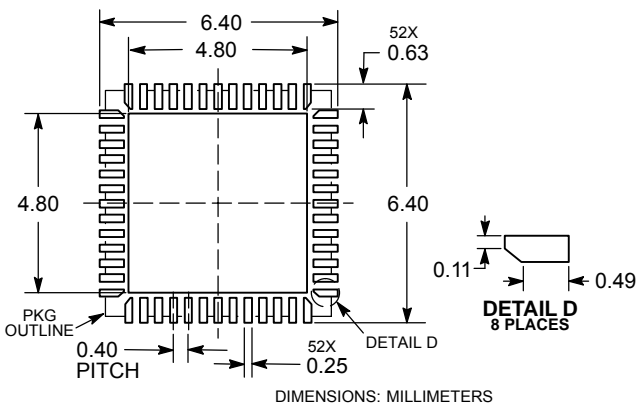
**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# LC709501F

## ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC709501FQD-A00TXG	QFN52 6x6, 0.4P (Pb-Free / Halogen Free)	2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. [http://www.onsemi.com/pub\\_link/Collateral/BRD8011-D.PDF](http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF)

Quick Charge is a trademark of Qualcomm Incorporated.

### <Caution>

This device is made for power applications.

Please execute appropriate test and take safety measures on your board.

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