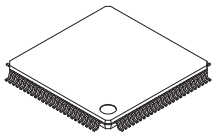
LC75812PT

1/8, 1/9-Duty Dot Matrix LCD Controller / Driver with Key Input Function

ON Semiconductor®

www.onsemi.com



TQFP100 14x14 / TQFP100

Overview

The LC75812PT is 1/8, 1/9 duty dot matrix LCD display controllers/drivers that support the display of characters, numbers, and symbols. In addition to generating dot matrix LCD drive signals based on data transferred serially from a microcontroller, the LC75812PT also provide on-chip character display ROM and RAM to allow display systems to be implemented easily. These products also provide up to 3 general-purpose output ports and incorporate a key scan circuit that accepts input from up to 35 keys to reduce printed circuit board wiring.

Features

- Key input function for up to 35 keys
  (A key scan is performed only when a key is pressed.)
- Controls and drives a 5×7 or 5×8 dot matrix LCD.
- Supports accessory display segment drive (up to 65 segments)
- Display technique: 1/8 duty 1/4 bias drive (5×7 dots)
  1/9 duty 1/4 bias drive (5×8 dots)
- Display digits: 13 digits×1 line (5×7 dots), 12 digits×1 line (5×8 dots)
- Display control memory
  - CGROM: 240 characters (5×7 or 5×8 dots)
  - CGRAM: 16 characters (5×7 or 5×8 dots)
  - ADRAM: 13×5 bits
  - DCRAM: 52×8 bits
- Instruction function
  - Display on/off control
  - Display shift function
- Sleep mode can be used to reduce current drain.
- Built-in display contrast adjustment circuit
- Switching between key scan output and general-purpose output ports can be controlled with instructions.
- PWM output for adjusting the LED backlight brightness
- The frame frequency of the common and segment output waveforms can be controlled by instructions.
- Serial data control of switching between the RC oscillator operating mode and external clock operating mode.
- Independent LCD driver block power supply V_{LCD}
- A voltage detection type reset circuit is provided to initialize the IC and prevent incorrect display.
- The $\overline{INH}$ pin is provided. This pin turns off the display, disables key scanning, and forces the general-purpose output ports to the low level.
- RC oscillator circuit

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 55 of this data sheet.

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +4.2	V
	V_{LCD} max	V_{LCD}	−0.3 to +11.0	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	−0.3 to +4.2	V
		CE, CL, DI, $\overline{INH}$ V_{DD}=2.7 to 3.6V	−0.3 to +6.5	
	$V_{IN}2$	OSC, KI1 to KI5, TEST	−0.3 to V_{DD} +0.3	
	$V_{IN}3$	$V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, $V_{LCD}4$	−0.3 to V_{LCD} +0.3	
Output voltage	$V_{OUT}1$	DO	-0.3 to +6.5	V
	$V_{OUT}2$	OSC, KS1 to KS7, P1 to P3	−0.3 to V_{DD} +0.3	
	$V_{OUT}3$	$V_{LCD}0$, S1 to S65, COM1 to COM9	−0.3 to V_{LCD} +0.3	
Output current	$I_{OUT}1$	S1 to S65	300	μA
	$I_{OUT}2$	COM1 to COM9	3	mA
	$I_{OUT}3$	KS1 to KS7	1	
	$I_{OUT}4$	P1 to P3	5	
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Range at Ta = −40°C to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		3.6	V
	V_{LCD}	V_{LCD} When the display contrast adjustment circuit is used.	7.0		10.0	
		V_{LCD} When the display contrast adjustment circuit is not used.	4.5		10.0	
Output voltage	$V_{LCD}0$	$V_{LCD}0$	$V_{LCD}4$ +4.5		V_{LCD}	V
Input voltage	$V_{LCD}1$	$V_{LCD}1$		3/4 ($V_{LCD}0$−$V_{LCD}4$)	$V_{LCD}0$	V
	$V_{LCD}2$	$V_{LCD}2$		2/4 ($V_{LCD}0$−$V_{LCD}4$)	$V_{LCD}0$	
	$V_{LCD}3$	$V_{LCD}3$		1/4 ($V_{LCD}0$−$V_{LCD}4$)	$V_{LCD}0$	
	$V_{LCD}4$	$V_{LCD}4$	0		1.5	
Input high level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.8V_{DD}		3.6	V
		CE, CL, DI, $\overline{INH}$ V_{DD} = 2.7 to 3.6 V	0.8V_{DD}		5.5	
	$V_{IH}2$	OSC external clock operating mode	0.8V_{DD}		V_{DD}	
	$V_{IH}3$	KI1 to KI5	0.6V_{DD}		V_{DD}	
Input low level voltage	$V_{IL}1$	CE, CL, DI, $\overline{INH}$, KI1 to KI5	0		0.2V_{DD}	V
	$V_{IL}2$	OSC external clock operating mode	0		0.2V_{DD}	

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Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Output pull-up voltage	V_{OUP}	DO	0		5.5	V
Recommended external resistor for RC oscillation	Rosc	OSC RC oscillator operating mode		10		kΩ
Recommended external capacitor for RC oscillation	Cosc	OSC RC oscillator operating mode		470		pF
Guaranteed range of RC oscillation	fosc	OSC RC oscillator operating mode	150	300	600	kHz
External clock operating frequency	f_{CK}	OSC external clock operating mode [Figure 4]	100	300	600	kHz
External clock duty cycle	D_{CK}	OSC external clock operating mode [Figure 4]	30	50	70	%
Data setup time	tds	CL, DI [Figure 2],[Figure 3]	160			ns
Data hold time	tdh	CL, DI [Figure 2],[Figure 3]	160			ns
CE wait time	tcp	CE, CL [Figure 2],[Figure 3]	160			ns
CE setup time	tcs	CE, CL [Figure 2],[Figure 3]	160			ns
CE hold time	tch	CE, CL [Figure 2],[Figure 3]	160			ns
High level clock pulse width	tϕH	CL [Figure 2],[Figure 3]	160			ns
Low level clock pulse width	tϕL	CL [Figure 2],[Figure 3]	160			ns
DO output delay time	tdc	DO R_{PU} = 4.7 kΩ C_L = 10 pF *1 [Figure 2],[Figure 3]			1.5	μs
DO rise time	tdr	DO R_{PU} = 4.7 kΩ C_L = 10 pF *1 [Figure 2],[Figure 3]			1.5	μs

Note: *1. Since the DO pin is an open-drain output, these times depend on the values of the pull-up resistor R_{PU} and the load capacitance C_L.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$, KI1 to KI5			$0.1V_{DD}$		V
Power-down detection voltage	V_{DET}			2.0	2.2	2.4	V
Input high level current	$I_{IH}1$	CE, CL, DI, $\overline{INH}$	V_I = 3.6 V			5.0	μA
			V_I = 5.5 V V_{DD} = 2.7 to 3.6 V			5.0	
	$I_{IH}2$	OSC	$V_I = V_{DD}$ external clock operating mode			5.0	
Input low level current	$I_{IL}1$	CE, CL, DI, $\overline{INH}$	V_I = 0 V	–5.0			μA
	$I_{IL}2$	OSC	V_I = 0 V external clock operating mode	–5.0			
Input floating voltage	V_{IF}	KI1 to KI5				$0.05V_{DD}$	V
Pull-down resistance	R_{PD}	KI1 to KI5	V_{DD} = 3.3 V	50	100	250	kΩ
Output off leakage current	I_{OFFH}	DO	V_O = 5.5 V			6.0	μA
Output high level voltage	$V_{OH}1$	S1 to S65	I_O = –20 μA	$V_{LCD}0$–0.6			V
	$V_{OH}2$	COM1 to COM9	I_O = –100 μA	$V_{LCD}0$–0.6			
	$V_{OH}3$	KS1 to KS7	I_O = –250 μA	V_{DD}–0.8	V_{DD}–0.4	V_{DD}–0.1	
	$V_{OH}4$	P1 to P3	I_O = –1 mA	V_{DD}–0.9			
Output low level voltage	$V_{OL}1$	S1 to S65	I_O = 20 μA			$V_{LCD}4$+0.6	V
	$V_{OL}2$	COM1 to COM9	I_O = 100 μA			$V_{LCD}4$+0.6	
	$V_{OL}3$	KS1 to KS7	I_O = 12.5 μA	0.1	0.4	1.2	
	$V_{OL}4$	P1 to P3	I_O = 1 mA			0.9	
	$V_{OL}5$	DO	I_O = 1 mA		0.1	0.3	

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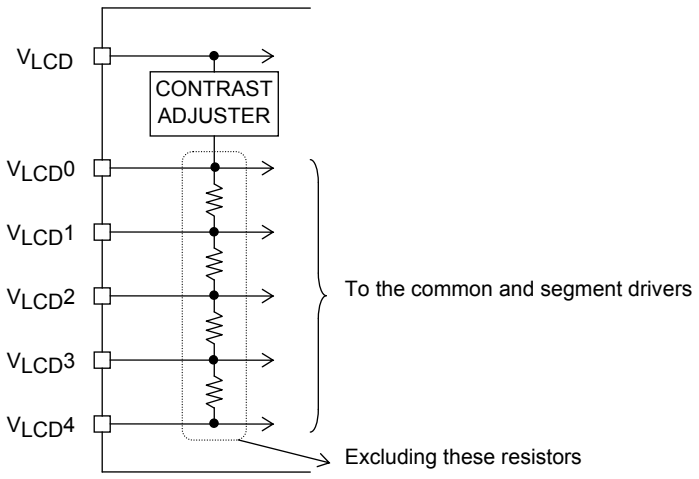
Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Output middle level voltage *2	$V_{MID}1$	S1 to S65	I_O = ±20 μA	2/4 ($V_{LCD}0$ −$V_{LCD}4$) −0.6		2/4 ($V_{LCD}0$ −$V_{LCD}4$) +0.6	V
	$V_{MID}2$	COM1 to COM9	I_O = ±100 μA	3/4 ($V_{LCD}0$ −$V_{LCD}4$) −0.6		3/4 ($V_{LCD}0$ −$V_{LCD}4$) +0.6	
	$V_{MID}3$	COM1 to COM9	I_O = ±100 μA	1/4 ($V_{LCD}0$ −$V_{LCD}4$) −0.6		1/4 ($V_{LCD}0$ −$V_{LCD}4$) +0.6	
Oscillator frequency	fosc	OSC	Rosc = 10 kΩ, Cosc = 470 pF	210	300	390	kHz
Current drain	$I_{DD}1$	V_{DD}	sleep mode			100	μA
	$I_{DD}2$	V_{DD}	V_{DD} = 3.6 V, output open, fosc = 300 kHz		500	1000	
	$I_{LCD}1$	V_{LCD}	sleep mode			15	
	$I_{LCD}2$	V_{LCD}	V_{LCD} = 10.0 V, output open, fosc = 300 kHz, When the display contrast adjustment circuit is used.		450	900	
	$I_{LCD}3$	V_{LCD}	V_{LCD} = 10.0 V, output open, fosc = 300 kHz, When the display contrast adjustment circuit is not used.		200	400	

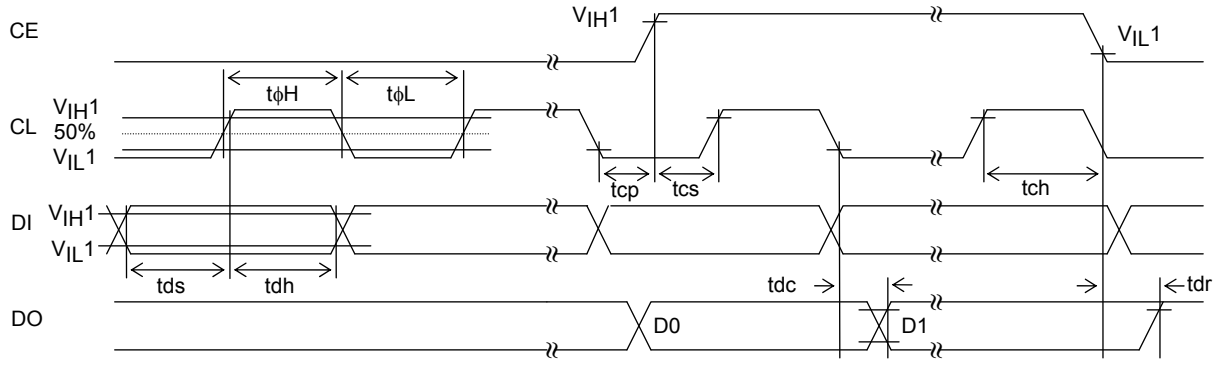
Note: *2. Excluding the bias voltage generation divider resistor built into the $V_{LCD}0$, $V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, and $V_{LCD}4$. (See Figure 1.)



[Figure 1]

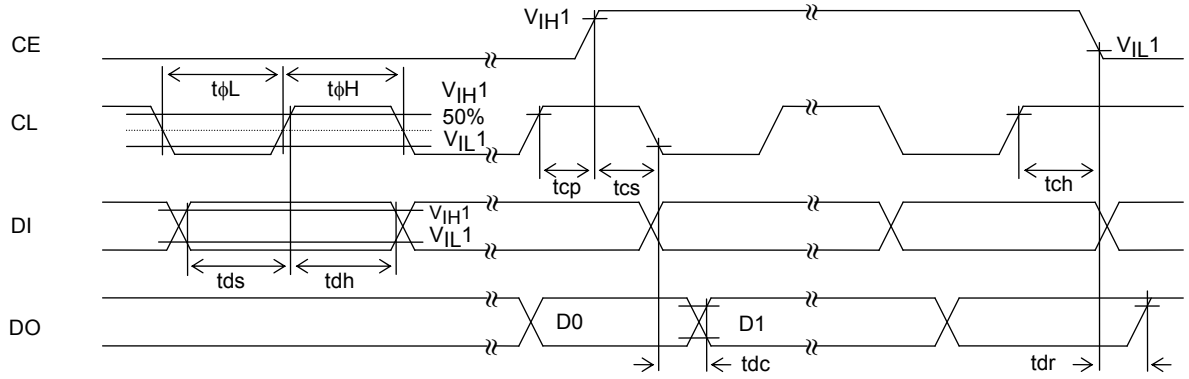
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

(1) When CL is stopped at the low level



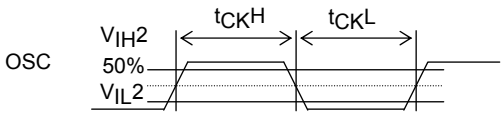
[Figure 2]

(2) When CL is stopped at the high level



[Figure 3]

(3) OSC pin clock timing in external clock operating mode



$$f_{CK} = \frac{1}{t_{CKH} + t_{CKL}} \text{ [kHz]}$$

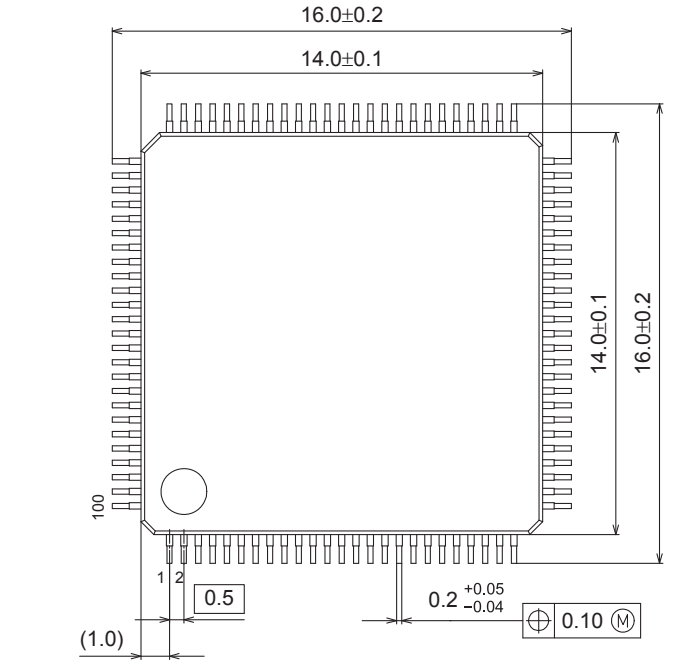
$$D_{CK} = \frac{t_{CKH}}{t_{CKH} + t_{CKL}} \times 100[\%]$$

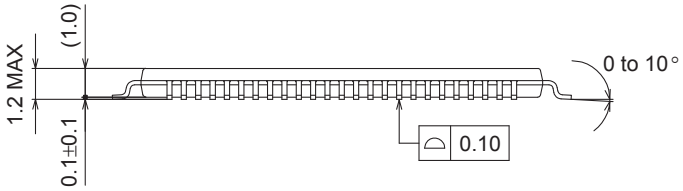
[Figure 4]

Package Dimensions

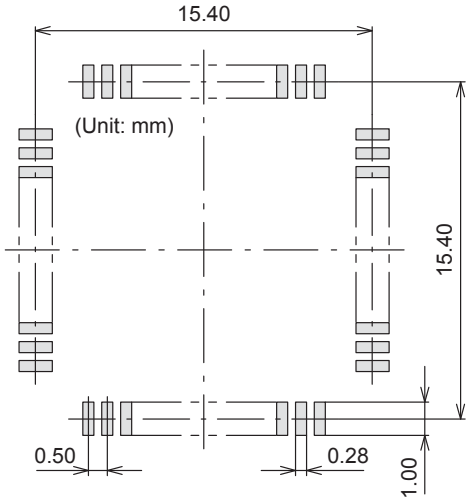
unit : mm

TQFP100 14x14 / TQFP100
CASE 932AY
ISSUE A

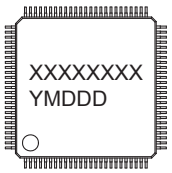




SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



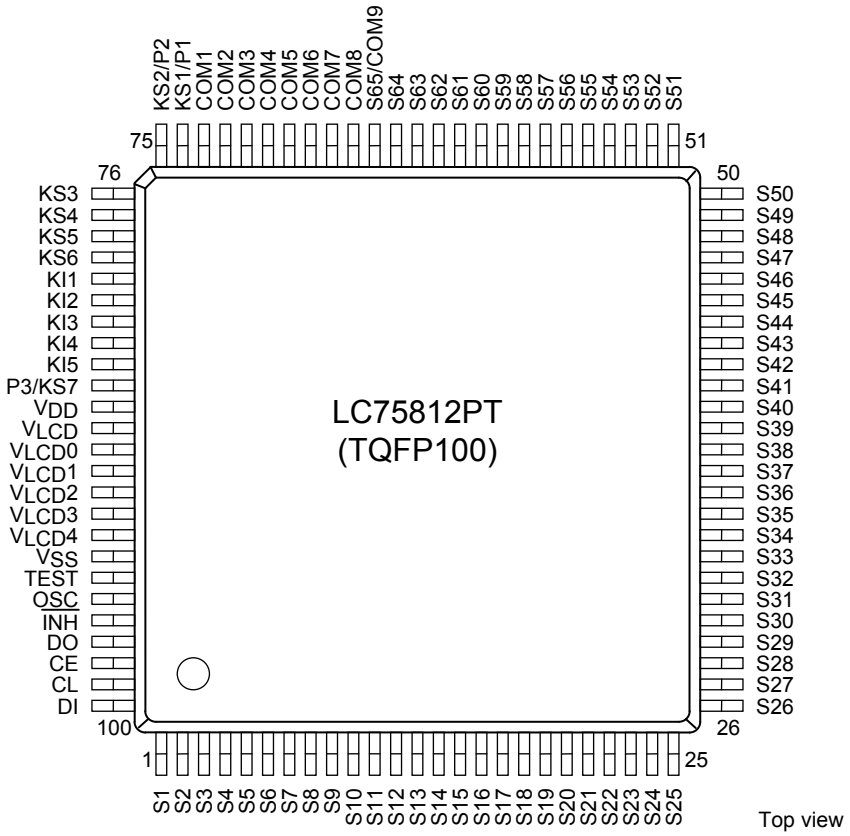
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

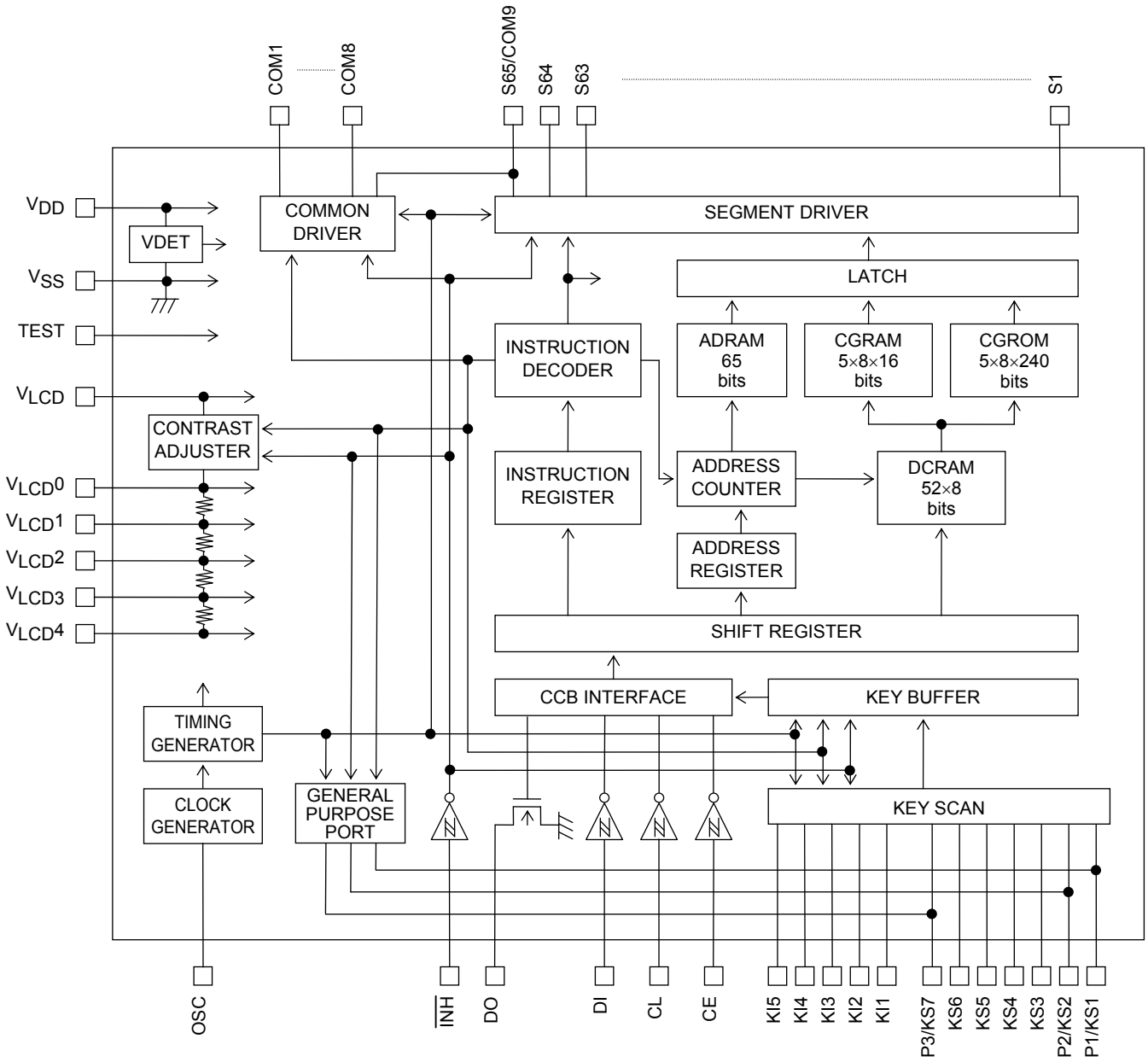
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignments



Top view

Block Diagram



Pin Functions

Pin	Pin No.	Function	Active	I/O	Handling when unused
S1 to S64 S65/COM9	1 to 64 65	Segment driver outputs. S65/COM9 can be used as common driver output pin under the "set display technique" instruction.	-	O	OPEN
COM1 to COM8	73 to 66	Common driver outputs.	-	O	OPEN
KS1/P1 KS2/P2 KS3 to KS6 KS7/P3	74 75 76 to 79 85	Key scan outputs. Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. KS1/P1, KS2/P2, and KS7/P3 can be used as general-purpose output ports under the "set key scan output port/general-purpose output port state" instruction.	-	O	OPEN
KI1 to KI5	80 to 84	Key scan inputs. These pins have built-in pull-down resistors.	H	I	GND
OSC	95	Oscillator connections. An oscillator circuit is formed by connecting an external resistor and capacitor to this pin. This pin can also be used as the external clock input pin with the "set display technique" instruction.	-	I/O	V_{DD}
CE	98	Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. CE: Chip enable CL: Synchronization clock DI: Transfer data DO: Output data	H	I	GND
CL	99		↑	I	
DI	100		-	I	
DO	97		-	O	OPEN
$\overline{INH}$	96	Input that turns the display off, disables key scanning, and forces the general-purpose output ports low. • When $\overline{INH}$ is low (V_{SS}): • Display off S1 to S64="L" ($V_{LCD}4$) S65/COM9="L" ($V_{LCD}4$) COM1 to COM8="L" ($V_{LCD}4$) • General-purpose output ports P1 to P3=low (V_{SS}) • Key scanning disabled: KS1 to KS7=low (V_{SS}) • All the key data is reset to low. • When $\overline{INH}$ is high (V_{DD}): • Display on • The state of the pins as key scan output pins or general-purpose output ports can be set with the "set key scan output port/general-purpose output port state" instruction. • Key scanning is enabled. However, serial data can be transferred when the $\overline{INH}$ pin is low.	L	I	V_{DD}
TEST	94	This pin must be connected to ground.	-	I	-
$V_{LCD}0$	88	LCD drive 4/4 bias voltage (high level) supply pin. The level on this pin can be changed by the display contrast adjustment circuit. However, ($V_{LCD}0$ - $V_{LCD}4$) must be greater than or equal to 4.5V. Also, external power must not be applied to this pin since the pin circuit includes the display contrast adjustment circuit.	-	O	OPEN
$V_{LCD}1$	89	LCD drive 3/4 bias voltage (middle level) supply pin. This pin can be used to supply the 3/4 (V_{LCD} - $V_{LCD}4$) voltage level externally.	-	I	OPEN
$V_{LCD}2$	90	LCD drive 2/4 bias voltage (middle level) supply pin. This pin can be used to supply the 2/4 ($V_{LCD}0$ - $V_{LCD}4$) voltage level externally.	-	I	OPEN

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Pin	Pin No.	Function	Active	I/O	Handling when unused
$V_{LCD}3$	91	LCD drive 1/4 bias voltage (middle level) supply pin. This pin can be used to supply the 1/4 ($V_{LCD}0$ - $V_{LCD}4$) voltage level externally.	-	I	OPEN
$V_{LCD}4$	92	LCD drive 0/4 bias voltage (low level) supply pin. Fine adjustment of the display contrast can be implemented by connecting an external variable resistor to this pin. However, ($V_{LCD}0$ - $V_{LCD}4$) must be greater than or equal to 4.5V, and $V_{LCD}4$ must be in the range 0V to 1.5V, inclusive.	-	I	GND
V_{DD}	86	Logic block power supply connection. Provide a voltage of between 2.7 to 3.6V.	-	-	-
V_{LCD}	87	LCD driver block power supply connection. Provide a voltage of between 7.0 to 10.0V when the display contrast adjustment circuit is used and provide a voltage of between 4.5 to 10.0V when the circuit is not used.	-	-	-
V_{SS}	93	Power supply connection. Connect to ground.	-	-	-

Block Functions

- AC (address counter)
  AC is a counter that provides the addresses used for DCRAM and ADRAM.
  The address is automatically modified internally, and the LCD display state is retained.

- DCRAM (data control RAM)
  DCRAM is RAM that is used to store display data expressed as 8-bit character codes. (These character codes are converted to 5×7 or 5×8 dot matrix character patterns using CGROM or CGRAM.) DCRAM has a capacity of 52×8 bits, and can hold 52 characters. The table below lists the correspondence between the 6-bit DCRAM address loaded into AC and the display position on the LCD panel.

- When the DCRAM address loaded into AC is 00H.

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
DCRAM address (hexadecimal)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C

However, when the display shift is performed by specifying MDATA, the DCRAM address shifts as shown below.

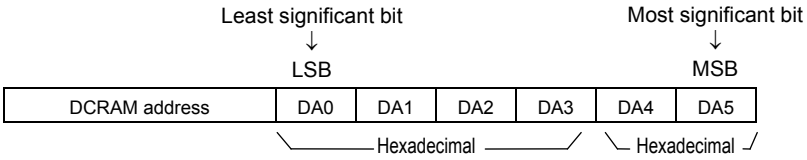
Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
DCRAM address (hexadecimal)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D

(shift left)

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
DCRAM address (hexadecimal)	33	00	01	02	03	04	05	06	07	08	09	0A	0B

(shift right)

Note: *3. The DCRAM address is expressed in hexadecimal.



Example: When the DCRAM address is 2EH.

DA0	DA1	DA2	DA3	DA4	DA5
0	1	1	1	0	1

Note: *4. 5×7 dots ····· 13th digit display 5×7 dots
5×8 dots ····· 13th digit display 4×8 dots

• ADRAM (Additional data RAM)
ADRAM is RAM that is used to store the ADATA display data. ADRAM has a capacity of 13×5 bits, and the stored display data is displayed directly without the use of CGROM or CGRAM. The table below lists the correspondence between the 4-bit ADRAM address loaded into AC and the display position on the LCD panel.

• When the ADRAM address loaded into AC is 0H. (Number of digit displayed: 13)

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
ADRAM address (hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C

However, when the display shift is performed by specifying ADATA, the ADRAM address shifts as shown below.

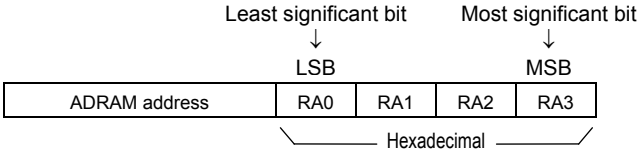
Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
ADRAM address (hexadecimal)	1	2	3	4	5	6	7	8	9	A	B	C	0

(shift left)

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
ADRAM address (hexadecimal)	C	0	1	2	3	4	5	6	7	8	9	A	B

(shift right)

Note: *5. The ADRAM address is expressed in hexadecimal.



Example: When the ADRAM address is AH.

RA0	RA1	RA2	RA3
0	1	0	1

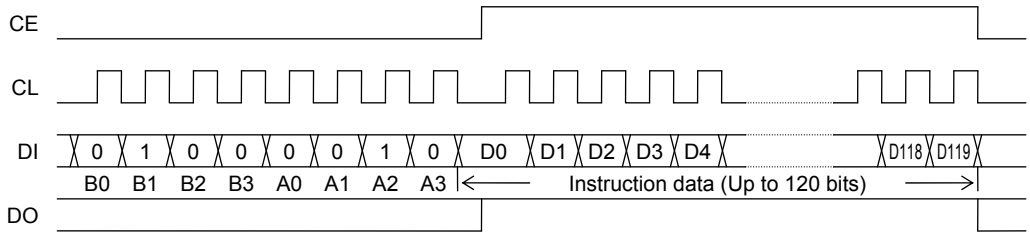
Note: *6. 5×7 dots ····· 13th digit display 5 dots
5×8 dots ····· 13th digit display 4 dots

• CGROM (Character generator ROM)
CGROM is ROM that is used to generate the 240 kinds of 5×7 or 5×8 dot matrix character patterns from the 8-bit character codes. CGROM has a capacity of 240×40 bits. When a character code is written to DCRAM, the character pattern stored in CGROM corresponding to the character code is displayed at the position on the LCD corresponding to the DCRAM address loaded into AC.

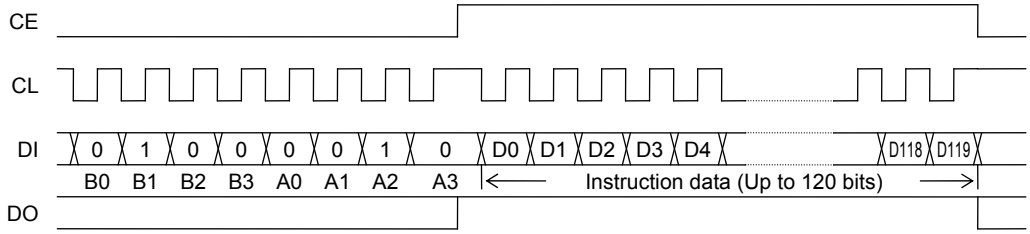
• CGRAM (Character generator RAM)
CGRAM is RAM to which user programs can freely write arbitrary character patterns. Up to 16 kinds of 5×7 or 5×8 dot matrix character patterns can be stored. CGRAM has a capacity of 16×40 bits.

Serial Data Input

(1) When CL is stopped at the low level



(2) When CL is stopped at the high level



- B0 to B3, A0 to A3: CCB address 42H
- D0 to D119: Instruction data

The data is acquired on the rising edge of the CL signal and latched on the falling edge of the CE signal. When transferring instruction data from the microcontroller, applications must assure that the time from the transfer of one set of instruction data until the next instruction data transfer is significantly longer than the instruction execution time.

Instruction Table

Instruction	D0…D56…D71	D72...D77 D78 D79	D80...D85 D86 D87	D88...D93 D94 D95	D96 D97 D98 D99 D100 D101 D102 D103	D104 D105 D106 D107 D108 D109 D110 D111	D112 D113 D114 D115	D116 D117 D118 D119	Execution time *11
Set display technique *7							DT FC0 FC1 OC	0 0 0 1	0μs/ 108μs *7
Display on/off control					DG1 DG2 DG3 DG4 DG5 DG6 DG7 DG8	DG9 DG10 DG11 DG12 DG13 X X X	M A SC SP	0 0 1 0	0μs/27μs *8
Display shift							M A R/L X	0 0 1 1	27μs
Set AC address						DA0 DA1 DA2 DA3 DA4 DA5 X X	RA0 RA1 RA2 RA3	0 1 0 0	27μs
DCRAM data write *9					AC0 AC1 AC2 AC3 AC4 AC5 AC6 AC7	DA0 DA1 DA2 DA3 DA4 DA5 X X	IM1 IM2 X X	0 1 0 1	27μs/tiμs *9
ADRAM data write *10					AD1 AD2 AD3 AD4 AD5 X X X	RA0 RA1 RA2 RA3 X X X X	IM1 IM2 X X	0 1 1 0	27μs/tiμs *10
CGRAM data write	... CD1...CD16	CD17 ... CD24	CD25 ... CD32	CD33 ... CD40	X X X X X X X X	CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7	X X X X	0 1 1 1	27μs
Set display contrast						CT0 CT1 CT2 CT3 X X X X	CTC X X X	1 0 0 0	0μs
Set key scan output port/ general-purpose output port state		W10...W15 W20 W21	W22...W25...W33	W34 W35 PC10...PC31	PC32 PF0 PF1 PF2 PF3 KC1 KC2 KC3	KC4 KC5 KC6 KC7 KP1 KP2 KP3 X	X X X X	1 0 0 1	0μs

X: don't care

Notes:
*7. Be sure to execute the "set display technique" instruction first after power-on (V_{DET}-based system reset). Note that the execution time of this first instruction is 108μs (fosc=300kHz, f_{CK}=300kHz).
*8.When the sleep mode (SP = 1) is set, the execution time is 27μs (when fosc = 300kHz, f_{CK} = 300kHz).
*9. The data format differs when the DCRAM data write instruction is executed in the normal increment mode (IM1=1, IM2=0) or in the super increment mode (IM1=0, IM2=1). Note that the execution time for the DCRAM data write instruction executed in the super increment mode is tiμs (fosc=300kHz, f_{CK}=300kHz). (See the detailed descriptions.)
*10. The data format differs when the ADRAM data write instruction is executed in the normal increment mode (IM1=1, IM2=0) or in the super increment mode (IM1=0, IM2=1). Note that the execution time for the ADRAM data write instruction executed in the super increment mode is tiμs (fosc=300kHz, f_{CK}=300kHz). (See the detailed descriptions.)
*11. The execution times listed here apply when fosc=300kHz, f_{CK}=300kHz. The execution times differ when the oscillator frequency fosc or the external clock frequency f_{CK} differs.
Example: When fosc = 210kHz, f_{CK} = 210kHz

$$27\mu s \times \frac{300}{210} = 39\mu s,\ 108\mu s \times \frac{300}{210} = 155\mu s,\ ti\mu s \times \frac{300}{210} = ti \times 1.43\mu s$$

Detailed Instruction Descriptions

• Set display technique ... <Sets the display technique>

(Display technique)

Code							
D112	D113	D114	D115	D116	D117	D118	D119
DT	FC0	FC1	OC	0	0	0	1

X: don't care

Note: Be sure to execute the "set display technique" instruction first after power-on (V_{DET}-based system reset).

DT: Sets the display technique

DT	Display technique	Output pins
		S65/COM9
0	1/8 duty, 1/4 bias drive	S65
1	1/9 duty, 1/4 bias drive	COM9

Note: *12. S65: Segment output
COM9: Common output

FC0, FC1: Sets the frame frequency of the common and segment output waveforms

FC0	FC1	Frame frequency	
		1/8 duty, 1/4 bias drive f8[Hz]	1/9 duty, 1/4 bias drive f9[Hz]
0	0	fosc/3072, f_{CK}/3072	fosc/3456, f_{CK}/3456
1	0	fosc/1536, f_{CK}/1536	fosc/1728, f_{CK}/1728
0	1	fosc/768, f_{CK}/768	fosc/864, f_{CK}/864

OC: Sets the RC oscillator operating mode and external clock operating mode.

OC	OSC pin function
0	RC oscillator operating mode
1	External clock operating mode

Note: *13. When selecting the RC oscillator operating mode, be sure to connect an external resistor Rosc and an external capacitor Cosc to the OSC pin.

• Display on/off control ... <Turns the display on or off>

(Display ON/OFF control)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
DG1	DG2	DG3	DG4	DG5	DG6	DG7	DG8	DG9	DG10	DG11	DG12	DG13	X	X	X	M	A	SC	SP	0	0	1	0

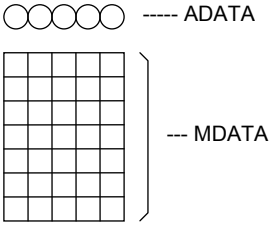
X: don't care

M, A: Specifies the data to be turned on or off

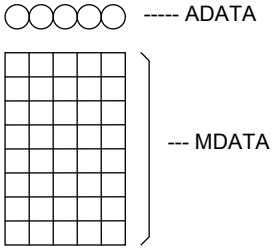
M	A	Display operating state
0	0	Both MDATA and ADATA are turned off (The display is forcibly turned off regardless of the DG1 to DG13 data.)
0	1	Only ADATA is turned on (The ADATA of display digits specified by the DG1 to DG13 data are turned on.)
1	0	Only MDATA is turned on (The MDATA of display digits specified by the DG1 to DG13 data are turned on.)
1	1	Both MDATA and ADATA are turned on (The MDATA and ADATA of display digits specified by the DG1 to DG13 data are turned on.)

Note: *14. MDATA, ADATA

5×7 dot matrix display



5×8 dot matrix display



DG1 to DG13: Specifies the display digit

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
Display digit data	DG1	DG2	DG3	DG4	DG5	DG6	DG7	DG8	DG9	DG10	DG11	DG12	DG13

For example, if DG1 to DG7 are 1, and DG8 to DG13 are 0, then display digits 1 to 7 will be turned on, and display digits 8 to 13 will be turned off (blanked).

SC: Controls the common and segment output pins

SC	Common and segment output pin states
0	Output of LCD drive waveforms
1	Fixed at the $V_{LCD}4$ level (all segments off)

Note: *15. When SC is 1, the S1 to S65 and COM1 to COM9 output pins are set to the $V_{LCD}4$ level, regardless of the M, A, and DG1 to DG13 data.

SP: Controls the normal mode and sleep mode

SP	Mode
0	Normal mode
1	Sleep mode The common and segment pins go to the $V_{LCD}4$ level and the oscillator on the OSC pin is stopped (although it operates during key scan operations) in RC oscillator operating mode (OC="0") and reception of the external clock is stopped (external clock is received during key scan operations) in external clock operating mode (OC="1"), to reduce current drain. Although the "display on/off control", "set display contrast" and "set key scan output port/general-purpose output port state" (disallowed to set pins P1 to P3 for PWM signal output and pin P3 for clock signal output) instructions can be executed in this mode, applications must return the IC to normal mode to execute any of the other instruction setting. When the IC is in external clock operating mode, be sure to stop the external clock input after the lapse of the instruction execution time (27μs: f_{CK}=300kHz).

- Display shift ... <Shifts the display>

(Display shift)

Code							
D112	D113	D114	D115	D116	D117	D118	D119
M	A	R/L	X	0	0	1	1

X: don’t care

M, A: Specifies the data to be shifted

M	A	Shift operating state
0	0	Neither MDATA nor ADATA is shifted
0	1	Only ADATA is shifted
1	0	Only MDATA is shifted
1	1	Both MDATA and ADATA are shifted

R/L: Specifies the shift direction

R/L	Shift direction
0	Shift left
1	Shift right

• Set AC address... <Specifies the DCRAM and ADRAM address for AC>
(Set AC)

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
DA0	DA1	DA2	DA3	DA4	DA5	X	X	RA0	RA1	RA2	RA3	0	1	0	0

X: don't care

DA0 to DA5: DCRAM address

DA0	DA1	DA2	DA3	DA4	DA5

LSB ↑ Least significant bit

MSB ↑ Most significant bit

RA0 to RA3: ADRAM address

RA0	RA1	RA2	RA3

LSB ↑ Least significant bit

MSB ↑ Most significant bit

This instruction loads the 6-bit DCRAM address DA0 to DA5 and the 4-bit ADRAM address RA0 to RA3 into the AC.

• DCRAM data write ... <Specifies the DCRAM address and stores data at that address>
(Write data to DCRAM)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	IM1	IM2	X	X	0	1	0	1

X: don't care

DA0 to DA5: DCRAM address

DA0	DA1	DA2	DA3	DA4	DA5

LSB ↑ Least significant bit

MSB ↑ Most significant bit

AC0 to AC7: DCRAM data (character code)

AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7

LSB ↑ Least significant bit

MSB ↑ Most significant bit

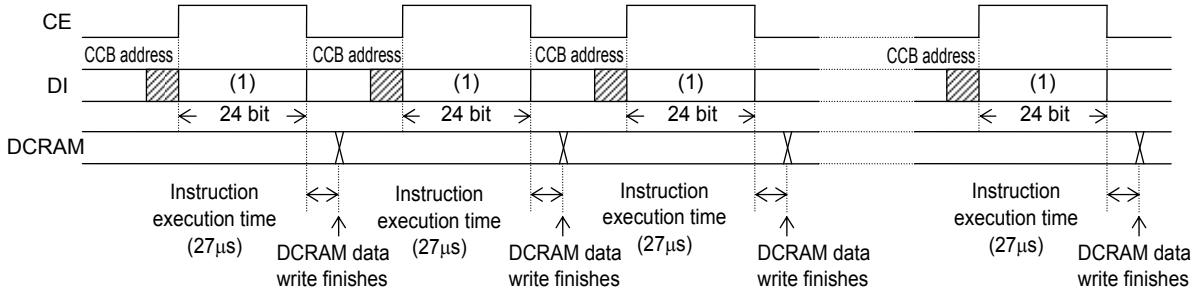
This instruction writes the 8 bits of data AC0 to AC7 to DCRAM. This data is a character code, and is converted to a 5×7 or 5×8 dot matrix display data using CGROM or CGRAM.

IM1, IM2: Sets the method of writing data to DCRAM

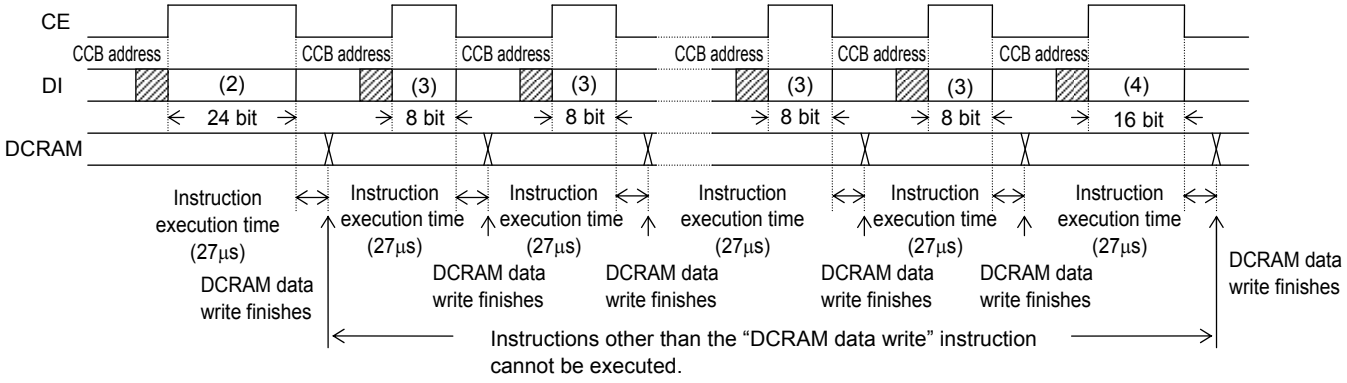
IM1	IM2	DCRAM data write method
0	0	Normal DCRAM data write (Specifies the DCRAM address and writes the DCRAM data.)
1	0	Normal increment mode DCRAM data write (Increments the DCRAM address by +1 each time data is written to DCRAM.)
0	1	Super increment mode DCRAM data write (Writes 2 to 13 characters of DCRAM data in single operation.)

Notes: *16.

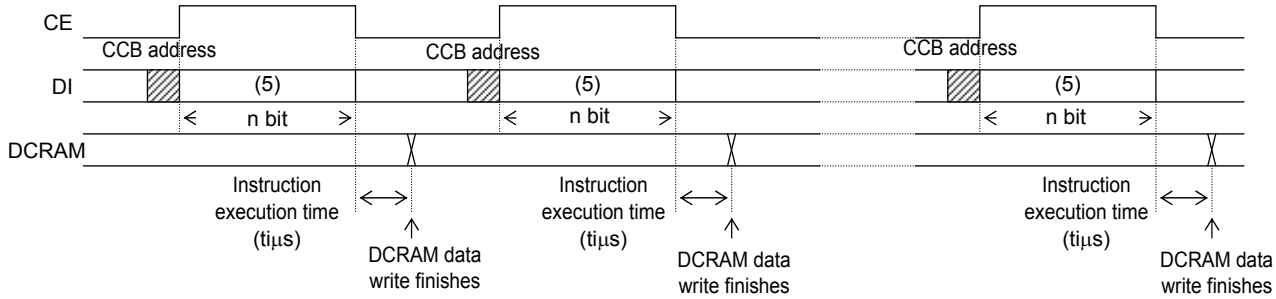
• DCRAM data write method when IM1 = 0, IM2 = 0



• DCRAM data write method when IM1 = 1, IM2 = 0
(Instructions other than the "DCRAM data write" instruction cannot be executed.)



• DCRAM data write method when IM1 = 0, IM2 = 1



$ti=13.5\mu s\times(\frac{n}{8}-1)$
(n=8m+16, m is an integer between 2 and 13 that is the number of characters written as DCRAM data.)
For example

When n= 32 bits (m=2): ti= 40.5μs (fosc=300kHz, f_{CK}=300kHz)
When n= 80 bits (m=8) : ti=121.5μs (fosc=300kHz, f_{CK}=300kHz)
When n=120 bits (m=13): ti=189.0μs (fosc=300kHz, f_{CK}=300kHz)

Note that the instruction execution time of 27μs and ti values in μs apply when fosc=300kHz and f_{CK}=300kHz, and that these execution times will differ when the CR oscillator frequency fosc and external clock frequency f_{CK} differ.

Data format at (1) (24 bits)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	0	0	X	X	0	1	0	1

X: don’t care

Data format at (2) (24 bits)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	1	0	X	X	0	1	0	1

X: don’t care

Data format at (3) (8 bits)

Code							
D112	D113	D114	D115	D116	D117	D118	D119
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7

Data format at (4) (16 bits)

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	0	0	X	X	0	1	0	1

Data format at (5) (n bit)

Code																			
Dz	Dz+1	Dz+2	Dz+3	Dz+4	Dz+5	Dz+6	Dz+7	•••••••••••••••••••••••••••							D88	D89	D90	D91	D92	D93	D94	D95
$AC0_1$	$AC1_1$	$AC2_1$	$AC3_1$	$AC4_1$	$AC5_1$	$AC6_1$	$AC7_1$	•••••••••••••••••••••••••••							$AC0_{m-1}$	$AC1_{m-1}$	$AC2_{m-1}$	$AC3_{m-1}$	$AC4_{m-1}$	$AC5_{m-1}$	$AC6_{m-1}$	$AC7_{m-1}$

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
$AC0_m$	$AC1_m$	$AC2_m$	$AC3_m$	$AC4_m$	$AC5_m$	$AC6_m$	$AC7_m$	$DA0_1$	$DA1_1$	$DA2_1$	$DA3_1$	$DA4_1$	$DA5_1$	X	X	0	1	X	X	0	1	0	1

X: don’t care

Here, n=8m+16, z=104-8m (m is an integer between 2 and 13 that is the number of characters written as DCRAM data.)

Correspondence between the DCRAM address and the DCRAM data

DCRAM address	DCRAM data
$DA0_1$ to $DA5_1$	$AC0_1$ to $AC7_1$
($DA0_1$ to $DA5_1$)+1	$AC0_2$ to $AC7_2$
($DA0_1$ to $DA5_1$)+2	$AC0_3$ to $AC7_3$
⋮	⋮
($DA0_1$ to $DA5_1$)+(m-3)	$AC0_{m-2}$ to $AC7_{m-2}$
($DA0_1$ to $DA5_1$)+(m-2)	$AC0_{m-1}$ to $AC7_{m-1}$
($DA0_1$ to $DA5_1$)+(m-1)	$AC0_m$ to $AC7_m$

Example 1: When n=32 bits (m=2: 2 characters DCRAM data write operation)

Code															
D88	D89	D90	D91	D92	D93	D94	D95	D96	D97	D98	D99	D100	D101	D102	D103
$AC0_1$	$AC1_1$	$AC2_1$	$AC3_1$	$AC4_1$	$AC5_1$	$AC6_1$	$AC7_1$	$AC0_2$	$AC1_2$	$AC2_2$	$AC3_2$	$AC4_2$	$AC5_2$	$AC6_2$	$AC7_2$

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
$DA0_1$	$DA1_1$	$DA2_1$	$DA3_1$	$DA4_1$	$DA5_1$	X	X	0	1	X	X	0	1	0	1

X: don’t care

Correspondence between the DCRAM address and the DCRAM data

DCRAM address	DCRAM data
$DA0_1$ to $DA5_1$	$AC0_1$ to $AC7_1$
($DA0_1$ to $DA5_1$)+1	$AC0_2$ to $AC7_2$

Example 2: When n=80 bits (m=8: 8 characters DCRAM data write operation)

Code															
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55
$AC0_1$	$AC1_1$	$AC2_1$	$AC3_1$	$AC4_1$	$AC5_1$	$AC6_1$	$AC7_1$	$AC0_2$	$AC1_2$	$AC2_2$	$AC3_2$	$AC4_2$	$AC5_2$	$AC6_2$	$AC7_2$

Code															
D56	D57	D58	D59	D60	D61	D62	D63	D64	D65	D66	D67	D68	D69	D70	D71
$AC0_3$	$AC1_3$	$AC2_3$	$AC3_3$	$AC4_3$	$AC5_3$	$AC6_3$	$AC7_3$	$AC0_4$	$AC1_4$	$AC2_4$	$AC3_4$	$AC4_4$	$AC5_4$	$AC6_4$	$AC7_4$

Code															
D72	D73	D74	D75	D76	D77	D78	D79	D80	D81	D82	D83	D84	D85	D86	D87
$AC0_5$	$AC1_5$	$AC2_5$	$AC3_5$	$AC4_5$	$AC5_5$	$AC6_5$	$AC7_5$	$AC0_6$	$AC1_6$	$AC2_6$	$AC3_6$	$AC4_6$	$AC5_6$	$AC6_6$	$AC7_6$

Code															
D88	D89	D90	D91	D92	D93	D94	D95	D96	D97	D98	D99	D100	D101	D102	D103
$AC0_7$	$AC1_7$	$AC2_7$	$AC3_7$	$AC4_7$	$AC5_7$	$AC6_7$	$AC7_7$	$AC0_8$	$AC1_8$	$AC2_8$	$AC3_8$	$AC4_8$	$AC5_8$	$AC6_8$	$AC7_8$

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
$DA0_1$	$DA1_1$	$DA2_1$	$DA3_1$	$DA4_1$	$DA5_1$	X	X	0	1	X	X	0	1	0	1

X: don't care

Correspondence between the DCRAM address and the DCRAM data

DCRAM address	DCRAM data
$DA0_1$ to $DA5_1$	$AC0_1$ to $AC7_1$
($DA0_1$ to $DA5_1$)+1	$AC0_2$ to $AC7_2$
($DA0_1$ to $DA5_1$)+2	$AC0_3$ to $AC7_3$
($DA0_1$ to $DA5_1$)+3	$AC0_4$ to $AC7_4$
($DA0_1$ to $DA5_1$)+4	$AC0_5$ to $AC7_5$
($DA0_1$ to $DA5_1$)+5	$AC0_6$ to $AC7_6$
($DA0_1$ to $DA5_1$)+6	$AC0_7$ to $AC7_7$
($DA0_1$ to $DA5_1$)+7	$AC0_8$ to $AC7_8$

Example 3: When n=120 bits (m=13: 13 characters DCRAM data write operation)

Code															
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
$AC0_1$	$AC1_1$	$AC2_1$	$AC3_1$	$AC4_1$	$AC5_1$	$AC6_1$	$AC7_1$	$AC0_2$	$AC1_2$	$AC2_2$	$AC3_2$	$AC4_2$	$AC5_2$	$AC6_2$	$AC7_2$

Code															
D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
$AC0_3$	$AC1_3$	$AC2_3$	$AC3_3$	$AC4_3$	$AC5_3$	$AC6_3$	$AC7_3$	$AC0_4$	$AC1_4$	$AC2_4$	$AC3_4$	$AC4_4$	$AC5_4$	$AC6_4$	$AC7_4$

Code															
D32	D33	D34	D35	D36	D37	D38	D39	D40	D41	D42	D43	D44	D45	D46	D47
$AC0_5$	$AC1_5$	$AC2_5$	$AC3_5$	$AC4_5$	$AC5_5$	$AC6_5$	$AC7_5$	$AC0_6$	$AC1_6$	$AC2_6$	$AC3_6$	$AC4_6$	$AC5_6$	$AC6_6$	$AC7_6$

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
$AC0_7$	$AC1_7$	$AC2_7$	$AC3_7$	$AC4_7$	$AC5_7$	$AC6_7$	$AC7_7$	$AC0_8$	$AC1_8$	$AC2_8$	$AC3_8$	$AC4_8$	$AC5_8$	$AC6_8$	$AC7_8$

Code															
D64	D65	D66	D67	D68	D69	D70	D71	D72	D73	D74	D75	D76	D77	D78	D79
$AC0_9$	$AC1_9$	$AC2_9$	$AC3_9$	$AC4_9$	$AC5_9$	$AC6_9$	$AC7_9$	$AC0_{10}$	$AC1_{10}$	$AC2_{10}$	$AC3_{10}$	$AC4_{10}$	$AC5_{10}$	$AC6_{10}$	$AC7_{10}$

Code															
D80	D81	D82	D83	D84	D85	D86	D87	D88	D89	D90	D91	D92	D93	D94	D95
$AC0_{11}$	$AC1_{11}$	$AC2_{11}$	$AC3_{11}$	$AC4_{11}$	$AC5_{11}$	$AC6_{11}$	$AC7_{11}$	$AC0_{12}$	$AC1_{12}$	$AC2_{12}$	$AC3_{12}$	$AC4_{12}$	$AC5_{12}$	$AC6_{12}$	$AC7_{12}$

Code															
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111
$AC0_{13}$	$AC1_{13}$	$AC2_{13}$	$AC3_{13}$	$AC4_{13}$	$AC5_{13}$	$AC6_{13}$	$AC7_{13}$	$DA0_1$	$DA1_1$	$DA2_1$	$DA3_1$	$DA4_1$	$DA5_1$	X	X

Code								
D112	D113	D114	D115	D116	D117	D118	D119
0	1	X	X	0	1	0	1

X: don't care

Correspondence between the DCRAM address and the DCRAM data

DCRAM address	DCRAM data
$DA0_1$ to $DA5_1$	$AC0_1$ to $AC7_1$
($DA0_1$ to $DA5_1$)+1	$AC0_2$ to $AC7_2$
($DA0_1$ to $DA5_1$)+2	$AC0_3$ to $AC7_3$
($DA0_1$ to $DA5_1$)+3	$AC0_4$ to $AC7_4$
($DA0_1$ to $DA5_1$)+4	$AC0_5$ to $AC7_5$
($DA0_1$ to $DA5_1$)+5	$AC0_6$ to $AC7_6$
($DA0_1$ to $DA5_1$)+6	$AC0_7$ to $AC7_7$

DCRAM address	DCRAM data
($DA0_1$ to $DA5_1$)+7	$AC0_8$ to $AC7_8$
($DA0_1$ to $DA5_1$)+8	$AC0_9$ to $AC7_9$
($DA0_1$ to $DA5_1$)+9	$AC0_{10}$ to $AC7_{10}$
($DA0_1$ to $DA5_1$)+10	$AC0_{11}$ to $AC7_{11}$
($DA0_1$ to $DA5_1$)+11	$AC0_{12}$ to $AC7_{12}$
($DA0_1$ to $DA5_1$)+12	$AC0_{13}$ to $AC7_{13}$

• ADRAM data write ... <Specifies the ADRAM address and stores data at that address>
(Write data to ADRAM)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AD1	AD2	AD3	AD4	AD5	X	X	X	RA0	RA1	RA2	RA3	X	X	X	X	IM1	IM2	X	X	0	1	1	0

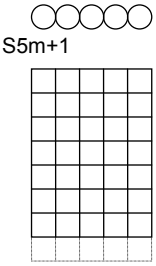
X: don't care

RA0 to RA3:ADRAM address

RA0	RA1	RA2	RA3

LSB MSB
↑ ↑
Least significant bit Most significant bit

AD1 to AD5: ADATA display data
In addition to the 5×7 or 5×8 dot matrix display data (MDATA), this IC supports direct display of the five accessory display segments provided in each digit as ADATA. This display function does not use CGROM or CGRAM. The figure below shows the correspondence between the data and the display. When ADn = 1(where n is an integer between 1 and 5) the segment corresponding to that data will be turned on.



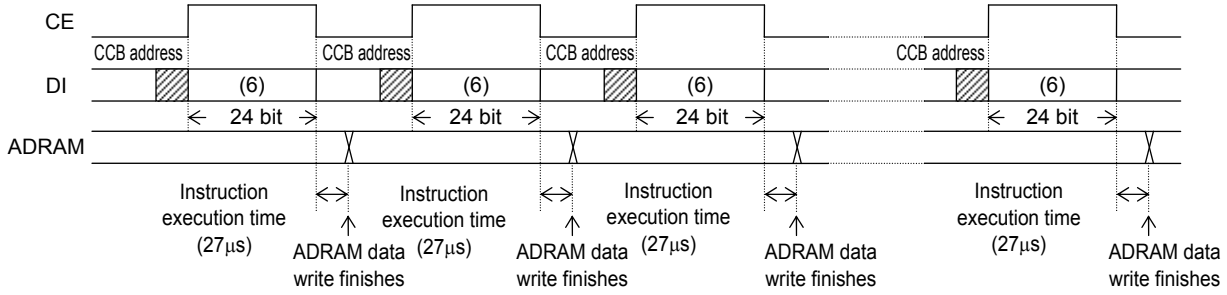
ADATA	Corresponding output pin
AD1	S5m+1 (m is an integer between 0 and 12)
AD2	S5m+2
AD3	S5m+3
AD4	S5m+4
AD5	S5m+5

IM1, IM2: Sets the method of writing data to ADRAM

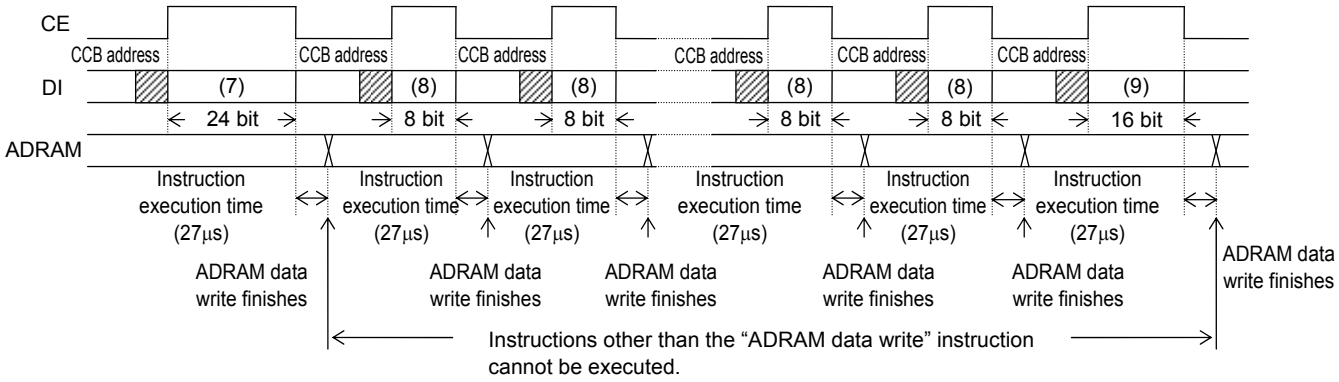
IM1	IM2	ADRAM data write method
0	0	Normal ADRAM data write (Specifies the ADRAM address and writes the ADRAM data.)
1	0	Nomal increment mode ADRAM data write (Increments the ADRAM address by +1 each time data is written to ADRAM.)
0	1	Super increment mode ADRAM data write (Writes 2 to 13 digits of ADRAM data in single operation.)

Notes: *17.

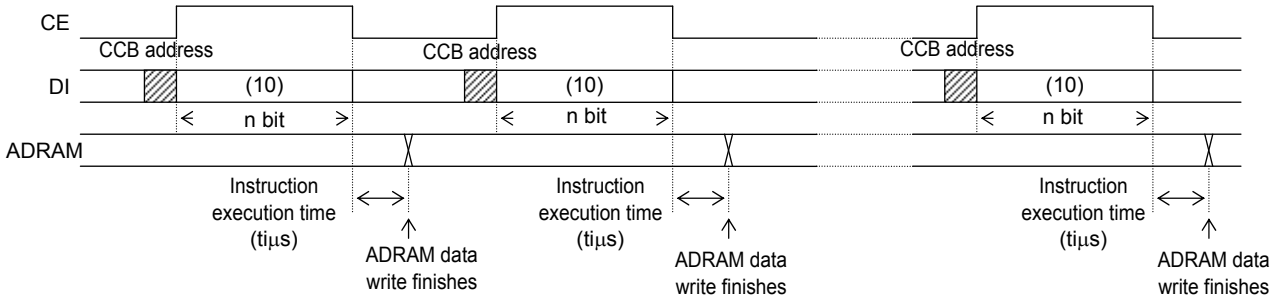
• ADRAM data write method when IM1 = 0, IM2 = 0



• ADRAM data write method when IM1 = 1, IM2 = 0
(Instructions other than the "ADRAM data write" instruction cannot be executed.)



• ADRAM data write method when IM1 = 0, IM2 = 1



$ti=13.5\mu s\times(\frac{n}{8}-1)$
(n=8m+16, m is an integer between 2 and 13 that is the number of characters written as ADRAM data.)
For example

When n= 32 bits (m=2): ti= 40.5μs (fosc=300kHz, f_{CK}=300kHz)
When n= 80 bits (m=8): ti=121.5μs (fosc=300kHz, f_{CK}=300kHz)
When n=120 bits (m=13): ti=189.0μs (fosc=300kHz, f_{CK}=300kHz)

Note that the instruction execution time of 27μs and ti values in μs apply when fosc=300kHz and f_{CK}=300kHz, and that these execution times will differ when the CR oscillator frequency fosc and external clock frequency f_{CK} differ.

Data format at (6) (24 bits)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AD1	AD2	AD3	AD4	AD5	X	X	X	RA0	RA1	RA2	RA3	X	X	X	X	0	0	X	X	0	1	1	0

X: don't care

Data format at (7) (24 bits)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AD1	AD2	AD3	AD4	AD5	X	X	X	RA0	RA1	RA2	RA3	X	X	X	X	1	0	X	X	0	1	1	0

X: don't care

Data format at (8) (8 bits)

Code							
D112	D113	D114	D115	D116	D117	D118	D119
AD1	AD2	AD3	AD4	AD5	X	X	X

Data format at (9) (16 bits)

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AD1	AD2	AD3	AD4	AD5	X	X	X	0	0	X	X	0	1	1	0

X: don't care

Data format at (10) (n bit)

Code																		
Dz	Dz+1	Dz+2	Dz+3	Dz+4	Dz+5	Dz+6	Dz+7	•••••••••••••••••••••••••••••	D88	D89	D90	D91	D92	D93	D94	D95
$AD1_1$	$AD2_1$	$AD3_1$	$AD4_1$	$AD5_1$	X	X	X	•••••••••••••••••••••••••••••	$AD1_{m-1}$	$AD2_{m-1}$	$AD3_{m-1}$	$AD4_{m-1}$	$AD5_{m-1}$	X	X	X

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
$AD1_m$	$AD2_m$	$AD3_m$	$AD4_m$	$AD5_m$	X	X	X	$RA0_1$	$RA1_1$	$RA2_1$	$RA3_1$	X	X	X	X	0	1	X	X	0	1	1	0

X: don't care

Here, n=8m+16, z=104-8m
(m is an integer between 2 and 13 that is the number of characters written as ADRAM data.)

Correspondence between the ADRAM address and theADRAM data

ADRAM address	ADRAM data
$RA0_1$ to $RA3_1$	$AD1_1$ to $AD5_1$
($RA0_1$ to $RA3_1$)+1	$AD1_2$ to $AD5_2$
($RA0_1$ to $RA3_1$)+2	$AD1_3$ to $AD5_3$
⋮	⋮
($RA0_1$ to $RA3_1$)+(m-3)	$AD1_{m-2}$ to $AD5_{m-2}$
($RA0_1$ to $RA3_1$)+(m-2)	$AD1_{m-1}$ to $AD5_{m-1}$
($RA0_1$ to $RA3_1$)+(m-1)	$AD1_m$ to $AD5_m$

Example 1: When n=32 bits (m=2: 2 characters ADRAM data write operation)

Code															
D88	D89	D90	D91	D92	D93	D94	D95	D96	D97	D98	D99	D100	D101	D102	D103
$AD1_1$	$AD2_1$	$AD3_1$	$AD4_1$	$AD5_1$	X	X	X	$AD1_2$	$AD2_2$	$AD3_3$	$AD4_4$	$AD5_5$	X	X	X

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
$RA0_1$	$RA1_1$	$RA2_1$	$RA3_1$	X	X	X	X	0	1	X	X	0	1	1	0

X: don’t care

Correspondence between the ADRAM address and the ADRAM data

ADRAM address	ADRAM data
$RA0_1$ to $RA3_1$	$AD1_1$ to $AD5_1$
($RA0_1$ to $RA3_1$)+1	$AD1_2$ to $AD5_2$

Example 2: When n=80 bits (m=8: 8 characters ADRAM data write operation)

Code															
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55
$AD1_1$	$AD2_1$	$AD3_1$	$AD4_1$	$AD5_1$	X	X	X	$AD1_2$	$AD2_2$	$AD3_2$	$AD4_2$	$AD5_2$	X	X	X

Code															
D56	D57	D58	D59	D60	D61	D62	D63	D64	D65	D66	D67	D68	D69	D70	D71
$AD1_3$	$AD2_3$	$AD3_3$	$AD4_3$	$AD5_3$	X	X	X	$AD1_4$	$AD2_4$	$AD3_4$	$AD4_4$	$AD5_4$	X	X	X

Code															
D72	D73	D74	D75	D76	D77	D78	D79	D80	D81	D82	D83	D84	D85	D86	D87
$AD1_5$	$AD2_5$	$AD3_5$	$AD4_5$	$AD5_5$	X	X	X	$AD1_6$	$AD2_6$	$AD3_6$	$AD4_6$	$AD5_6$	X	X	X

Code															
D88	D89	D90	D91	D92	D93	D94	D95	D96	D97	D98	D99	D100	D101	D102	D103
$AD1_7$	$AD2_7$	$AD3_7$	$AD4_7$	$AD5_7$	X	X	X	$AD1_8$	$AD2_8$	$AD3_8$	$AD4_8$	$AD5_8$	X	X	X

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
$RA0_1$	$RA1_1$	$RA2_1$	$RA3_1$	X	X	X	X	0	1	X	X	0	1	1	0

X: don't care

Correspondence between the ADRAM address and the ADRAM data

ADRAM address	ADRAM data
$RA0_1$ to $RA3_1$	$AD1_1$ to $AD5_1$
($RA0_1$ to $RA3_1$)+1	$AD1_2$ to $AD5_2$
($RA0_1$ to $RA3_1$)+2	$AD1_3$ to $AD5_3$
($RA0_1$ to $RA3_1$)+3	$AD1_4$ to $AD5_4$
($RA0_1$ to $RA3_1$)+4	$AD1_5$ to $AD5_5$
($RA0_1$ to $RA3_1$)+5	$AD1_6$ to $AD5_6$
($RA0_1$ to $RA3_1$)+6	$AD1_7$ to $AD5_7$
($RA0_1$ to $RA3_1$)+7	$AD1_8$ to $AD5_8$

Example 3: When n=120 bits (m=13: 13 characters ADRAM data write operation)

Code															
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
$AD1_1$	$AD2_1$	$AD3_1$	$AD4_1$	$AD5_1$	X	X	X	$AD1_2$	$AD2_2$	$AD3_2$	$AD4_2$	$AD5_2$	X	X	X

Code															
D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
$AD1_3$	$AD2_3$	$AD3_3$	$AD4_3$	$AD5_3$	X	X	X	$AD1_4$	$AD2_4$	$AD3_4$	$AD4_4$	$AD5_4$	X	X	X

Code															
D32	D33	D34	D35	D36	D37	D38	D39	D40	D41	D42	D43	D44	D45	D46	D47
$AD1_5$	$AD2_5$	$AD3_5$	$AD4_5$	$AD5_5$	X	X	X	$AD1_6$	$AD2_6$	$AD3_6$	$AD4_6$	$AD5_6$	X	X	X

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
$AD1_7$	$AD2_7$	$AD3_7$	$AD4_7$	$AD5_7$	X	X	X	$AD1_8$	$AD2_8$	$AD3_8$	$AD4_8$	$AD5_8$	X	X	X

Code															
D64	D65	D66	D67	D68	D69	D70	D71	D72	D73	D74	D75	D76	D77	D78	D79
$AD1_9$	$AD2_9$	$AD3_9$	$AD4_9$	$AD5_9$	X	X	X	$AD1_{10}$	$AD2_{10}$	$AD3_{10}$	$AD4_{10}$	$AD5_{10}$	X	X	X

Code															
D80	D81	D82	D83	D84	D85	D86	D87	D88	D89	D90	D91	D92	D93	D94	D95
$AD1_{11}$	$AD2_{11}$	$AD3_{11}$	$AD4_{11}$	$AD5_{11}$	X	X	X	$AD1_{12}$	$AD2_{12}$	$AD3_{12}$	$AD4_{12}$	$AD5_{12}$	X	X	X

Code															
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111
$AD1_{13}$	$AD2_{13}$	$AD3_{13}$	$AD4_{13}$	$AD5_{13}$	X	X	X	$RA0_1$	$RA1_1$	$RA2_1$	$RA3_1$	X	X	X	X

Code							
D112	D113	D114	D115	D116	D117	D118	D119
0	1	X	X	0	1	1	0

X: don't care

Correspondence between the ADRAM address and the ADRAM data

ADRAM address	ADRAM data
$RA0_1$ to $RA3_1$	$AD1_1$ to $AD5_1$
($RA0_1$ to $RA3_1$)+1	$AD1_2$ to $AD5_2$
($RA0_1$ to $RA3_1$)+2	$AD1_3$ to $AD5_3$
($RA0_1$ to $RA3_1$)+3	$AD1_4$ to $AD5_4$
($RA0_1$ to $RA3_1$)+4	$AD1_5$ to $AD5_5$
($RA0_1$ to $RA3_1$)+5	$AD1_6$ to $AD5_6$
($RA0_1$ to $RA3_1$)+6	$AD1_7$ to $AD5_7$

ADRAM address	ADRAM data
($RA0_1$ to $RA3_1$)+7	$AD1_8$ to $AD5_8$
($RA0_1$ to $RA3_1$)+8	$AD1_9$ to $AD5_9$
($RA0_1$ to $RA35_1$)+9	$AD1_{10}$ to $AD5_{10}$
($RA0_1$ to $RA3_1$)+10	$AD1_{11}$ to $AD5_{11}$
($RA0_1$ to $RA3_1$)+11	$AD1_{12}$ to $AD5_{12}$
($RA0_1$ to $RA3_1$)+12	$AD1_{13}$ to $AD5_{13}$

• CGRAM data write ... <Specifies the CGRAM address and stores data at that address>
(Write data to CGRAM)

Code															
D56	D57	D58	D59	D60	D61	D62	D63	D64	D65	D66	D67	D68	D69	D70	D71
CD1	CD2	CD3	CD4	CD5	CD6	CD7	CD8	CD9	CD10	CD11	CD12	CD13	CD14	CD15	CD16

Code															
D72	D73	D74	D75	D76	D77	D78	D79	D80	D81	D82	D83	D84	D85	D86	D87
CD17	CD18	CD19	CD20	CD21	CD22	CD23	CD24	CD25	CD26	CD27	CD28	CD29	CD30	CD31	CD32

Code															
D88	D89	D90	D91	D92	D93	D94	D95	D96	D97	D98	D99	D100	D101	D102	D103
CD33	CD34	CD35	CD36	CD37	CD38	CD39	CD40	X	X	X	X	X	X	X	X

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	X	X	X	X	0	1	1	1

X: don’t care

CA0 to CA7: CGRAM address

CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7

LSB ↑ Least significant bit

MSB ↑ Most significant bit

CD1 to CD40: CGRAM data (5×7 or 5×8 dot matrix display data)
The bit CDn (where n is an integer between 1 and 40) corresponds to the 5×7 or 5×8 dot matrix display data.
The figure below shows that correspondence. When CDn is 1 the dots which correspond to that data will be turned on.

CD1	CD2	CD3	CD4	CD5
CD6	CD7	CD8	CD9	CD10
CD11	CD12	CD13	CD14	CD15
CD16	CD17	CD18	CD19	CD20
CD21	CD22	CD23	CD24	CD25
CD26	CD27	CD28	CD29	CD30
CD31	CD32	CD33	CD34	CD35
CD36	CD37	CD38	CD39	CD40

Note: *18. CD1 to CD35: 5×7 dot matrix display data
CD1 to CD40: 5×8 dot matrix display data

• Set display contrast… <Sets the display contrast>

(Set display contrast)

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
CT0	CT1	CT2	CT3	X	X	X	X	CTC	X	X	X	1	0	0	0

X: don't care

CT0 to CT3: Sets the display contrast (11 steps)

CT0	CT1	CT2	CT3	LCD drive 4/4 bias voltage supply $V_{LCD}0$ level
0	0	0	0	$0.94V_{LCD}=V_{LCD}-(0.03V_{LCD}\times2)$
1	0	0	0	$0.91V_{LCD}=V_{LCD}-(0.03V_{LCD}\times3)$
0	1	0	0	$0.88V_{LCD}=V_{LCD}-(0.03V_{LCD}\times4)$
1	1	0	0	$0.85V_{LCD}=V_{LCD}-(0.03V_{LCD}\times5)$
0	0	1	0	$0.82V_{LCD}=V_{LCD}-(0.03V_{LCD}\times6)$
1	0	1	0	$0.79V_{LCD}=V_{LCD}-(0.03V_{LCD}\times7)$
0	1	1	0	$0.76V_{LCD}=V_{LCD}-(0.03V_{LCD}\times8)$
1	1	1	0	$0.73V_{LCD}=V_{LCD}-(0.03V_{LCD}\times9)$
0	0	0	1	$0.70V_{LCD}=V_{LCD}-(0.03V_{LCD}\times10)$
1	0	0	1	$0.67V_{LCD}=V_{LCD}-(0.03V_{LCD}\times11)$
0	1	0	1	$0.64V_{LCD}=V_{LCD}-(0.03V_{LCD}\times12)$

CTC: Sets the display contrast adjustment circuit state

CTC	Display contrast adjustment circuit state
0	The display contrast adjustment circuit is disabled, and the $V_{LCD}0$ pin level is forced to the V_{LCD} level.
1	The display contrast adjustment circuit operates, and the display contrast is adjusted.

Note that although the display contrast can be adjusted by operating the built-in display contrast adjustment circuit, it is also possible to apply fine adjustments to the contrast by connecting an external variable resistor to the $V_{LCD}4$ pin and modifying the $V_{LCD}4$ pin voltage. However, the following conditions must be met: $V_{LCD}0$-$V_{LCD}4\geq 4.5V$, and $1.5V\geq V_{LCD}4 \geq 0V$.

• Set key scan output port/general-purpose output port state

... <Sets the key scan output port and general-purpose output port states>

(Key scan output port and General-purpose output port control)

Code																							
D72	D73	D74	D75	D76	D77	D78	D79	D80	D81	D82	D83	D84	D85	D86	D87	D88	D89	D90	D91	D92	D93	D94	D95
W10	W11	W12	W13	W14	W15	W20	W21	W22	W23	W24	W25	W30	W31	W32	W33	W34	W35	PC10	PC11	PC20	PC21	PC30	PC31

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
PC32	PF0	PF1	PF2	PF3	KC1	KC2	KC3	KC4	KC5	KC6	KC7	KP1	KP2	KP3	X	X	X	X	X	1	0	0	1

X: don't care

KP1 to KP3: Set the output pins KS1/P1, KS2/P2, and KS7/P3 as either key scan output ports or general-purpose output ports.

KP1	KP2	KP3	Output pin			Max. Key Input Number	General-purpose Output Port Number
			KS1/P1	KS2/P2	KS7/P3		
0	0	0	KS1	KS2	KS7	35	0
1	0	0	P1	KS2	KS7	30	1
0	1	0	KS1	P2	KS7	30	1
0	0	1	KS1	KS2	P3	30	1
1	1	0	P1	P2	KS7	25	2
0	1	1	KS1	P2	P3	25	2
1	0	1	P1	KS2	P3	25	2
1	1	1	P1	P2	P3	20	3

*19) KSn(n=1,2,7): Key scan output port
Pn(n=1 to 3): General-purpose output port

KC1 to KC7: Sets the key scan output pin KS1 to KS7 state

Output pin	KS1	KS2	KS3	KS4	KS5	KS6	KS7
Key scan output state setting data	KC1	KC2	KC3	KC4	KC5	KC6	KC7

If, for example, the output pins KS1/P1, KS2/P2, and KS7/P3 are set as key scan output ports, the output pins KS1 to KS3 will go high (V_{DD}) and KS4 to KS7 go low (V_{SS}) in the key scan standby state when KC1 to KC3 are set to 1 and KC4 to KC7 are set to 0. Note that key scan output signals are not output from output pins that are set to the low level.

PC10, PC11: Sets the general-purpose output port P1 state

PC10	PC11	Output pin (P1) state
0	0	"L"(V_{SS})
1	0	"H"(V_{DD})
0	1	PWM signal output

PC20, PC21: Sets the general-purpose output port P2 state

PC20	PC21	Output pin (P2) state
0	0	"L"(V_{SS})
1	0	"H"(V_{DD})
0	1	PWM signal output

PC30 to PC32: Sets the general-purpose output port P3 state

PC30	PC31	PC32	Output pin (P3) state
0	0	0	"L"(V_{SS})
1	0	0	"H"(V_{DD})
0	1	0	PWM signal output
1	1	0	Clock signal output (fosc/2, f_{CK}/2)
0	0	1	Clock signal output (fosc/8, f_{CK}/8)

PF0 to PF3: Set the frame frequency of the PWM output waveforms.
(when general-purpose outout ports P1 to P3 are set to select the PWM signal generation function.)

PF0	PF1	PF2	PF3	PWM Output Waveform Frame Frequency fp[Hz]
0	0	0	0	fosc/1536, f_{CK}/1536
1	0	0	0	fosc/1408, f_{CK}/1408
0	1	0	0	fosc/1280, f_{CK}/1280
1	1	0	0	fosc/1152, f_{CK}/1152
0	0	1	0	fosc/1024, f_{CK}/1024
1	0	1	0	fosc/896, f_{CK}/896
0	1	1	0	fosc/768, f_{CK}/768
1	1	1	0	fosc/640, f_{CK}/640
0	0	0	1	fosc/512, f_{CK}/512
1	0	0	1	fosc/384, f_{CK}/384
0	1	0	1	fosc/256, f_{CK}/256

W10 to W15, W20 to W25, W30 to W35: Set the pulse width of the PWM output waveforms.
(when general-purpose outout ports P1 to P3 are set to select the PWM signal generation function.)

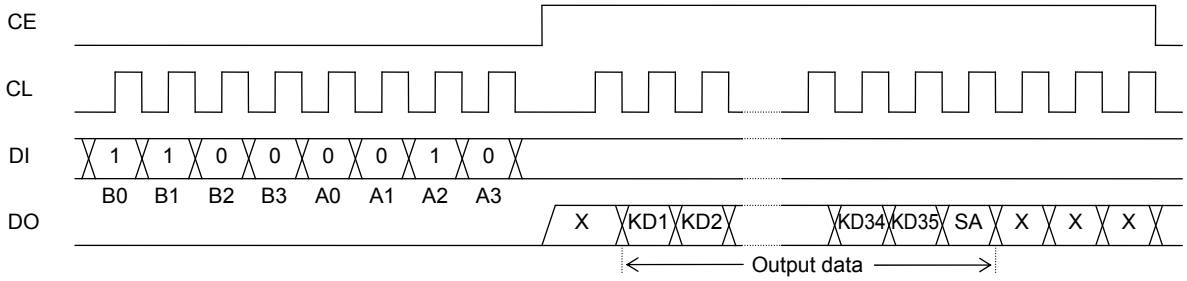
Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	PWM Signal Pn Pulse Width	Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	PWM Signal Pn Pulse Width
0	0	0	0	0	0	(1/64) ×Tp	0	0	0	0	0	1	(33/64) ×Tp
1	0	0	0	0	0	(2/64) ×Tp	1	0	0	0	0	1	(34/64) ×Tp
0	1	0	0	0	0	(3/64) ×Tp	0	1	0	0	0	1	(35/64) ×Tp
1	1	0	0	0	0	(4/64) ×Tp	1	1	0	0	0	1	(36/64) ×Tp
0	0	1	0	0	0	(5/64) ×Tp	0	0	1	0	0	1	(37/64) ×Tp
1	0	1	0	0	0	(6/64) ×Tp	1	0	1	0	0	1	(38/64) ×Tp
0	1	1	0	0	0	(7/64) ×Tp	0	1	1	0	0	1	(39/64) ×Tp
1	1	1	0	0	0	(8/64) ×Tp	1	1	1	0	0	1	(40/64) ×Tp
0	0	0	1	0	0	(9/64) ×Tp	0	0	0	1	0	1	(41/64) ×Tp
1	0	0	1	0	0	(10/64) ×Tp	1	0	0	1	0	1	(42/64) ×Tp
0	1	0	1	0	0	(11/64) ×Tp	0	1	0	1	0	1	(43/64) ×Tp
1	1	0	1	0	0	(12/64) ×Tp	1	1	0	1	0	1	(44/64) ×Tp
0	0	1	1	0	0	(13/64) ×Tp	0	0	1	1	0	1	(45/64) ×Tp
1	0	1	1	0	0	(14/64) ×Tp	1	0	1	1	0	1	(46/64) ×Tp
0	1	1	1	0	0	(15/64) ×Tp	0	1	1	1	0	1	(47/64) ×Tp
1	1	1	1	0	0	(16/64) ×Tp	1	1	1	1	0	1	(48/64) ×Tp
0	0	0	0	1	0	(17/64) ×Tp	0	0	0	0	1	1	(49/64) ×Tp
1	0	0	0	1	0	(18/64) ×Tp	1	0	0	0	1	1	(50/64) ×Tp
0	1	0	0	1	0	(19/64) ×Tp	0	1	0	0	1	1	(51/64) ×Tp
1	1	0	0	1	0	(20/64) ×Tp	1	1	0	0	1	1	(52/64) ×Tp
0	0	1	0	1	0	(21/64) ×Tp	0	0	1	0	1	1	(53/64) ×Tp
1	0	1	0	1	0	(22/64) ×Tp	1	0	1	0	1	1	(54/64) ×Tp
0	1	1	0	1	0	(23/64) ×Tp	0	1	1	0	1	1	(55/64) ×Tp
1	1	1	0	1	0	(24/64) ×Tp	1	1	1	0	1	1	(56/64) ×Tp
0	0	0	1	1	0	(25/64) ×Tp	0	0	0	1	1	1	(57/64) ×Tp
1	0	0	1	1	0	(26/64) ×Tp	1	0	0	1	1	1	(58/64) ×Tp
0	1	0	1	1	0	(27/64) ×Tp	0	1	0	1	1	1	(59/64) ×Tp
1	1	0	1	1	0	(28/64) ×Tp	1	1	0	1	1	1	(60/64) ×Tp
0	0	1	1	1	0	(29/64) ×Tp	0	0	1	1	1	1	(61/64) ×Tp
1	0	1	1	1	0	(30/64) ×Tp	1	0	1	1	1	1	(62/64) ×Tp
0	1	1	1	1	0	(31/64) ×Tp	0	1	1	1	1	1	(63/64) ×Tp
1	1	1	1	1	0	(32/64) ×Tp	1	1	1	1	1	1	(64/64) ×Tp

Note: *20. Wn0 to Wn5 (n=1 to 3): PWM data for the PWM output waveforms at general-purpose output ports Pn (n=1 to 3).

$$Tp = \frac{1}{fp}$$

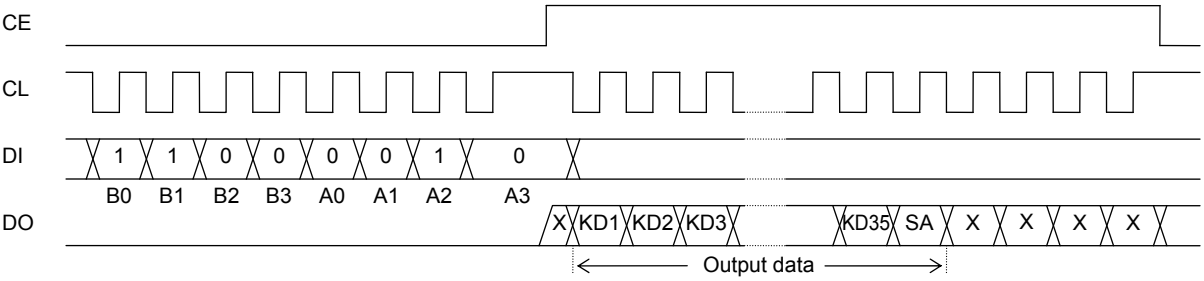
Serial Data Output

(1) When CL is stopped at the low level



X: don't care

(2) When CL is stopped at the high level



X: don't care

- B0 to B3, A0 to A3: CCB address 43H
- KD1 to KD35: Key data
- SA: Sleep acknowledge data

Note: *21. When key data read operation is executed with DO set high (no key data read request present), the key data (KD1 to KD35) and sleep acknowledge data (SA) are invalid.

Output Data

(1) KD1 to KD35: Key data

When a key matrix of up to 35 keys is formed from the KS1 to KS7 output pins and the KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

	KI1	KI2	KI3	KI4	KI5
KS1/P1	KD1	KD2	KD3	KD4	KD5
KS2/P1	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30
KS7/P3	KD31	KD32	KD33	KD34	KD35

KD1 to KD10 are all set to 0 when the output pins KS1/P1 and KS2/P2 are set as general-purpose output ports with the "set key scan output port/general-purpose output port state" instruction and a key matrix of maximum 25 keys is formed from the output pins KS3 to KS6 and KS7/P3 and the input pins KI1 to KI5.

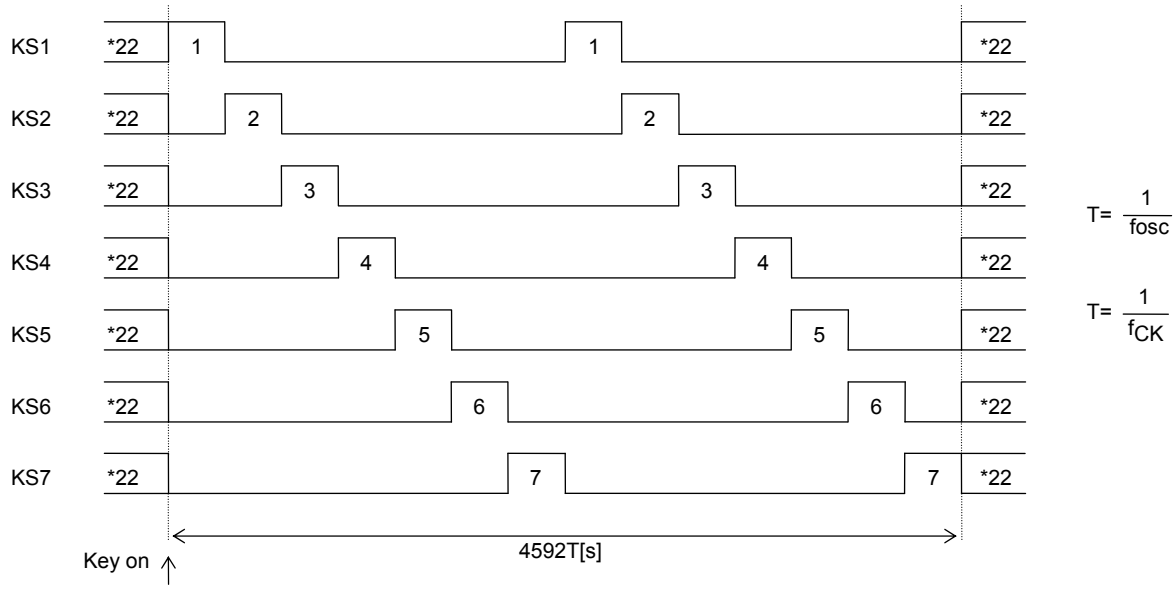
(2) SA: Sleep acknowledge data

This output data bit is set to the state when the key was pressed. Also, while DO will be low in this case, if serial data is input and the mode is set (to normal or sleep mode) during this period, that mode will be set. SA will be 1 in Sleep mode and 0 in normal mode.

Key Scan Operation Functions

(1) Key scan timing

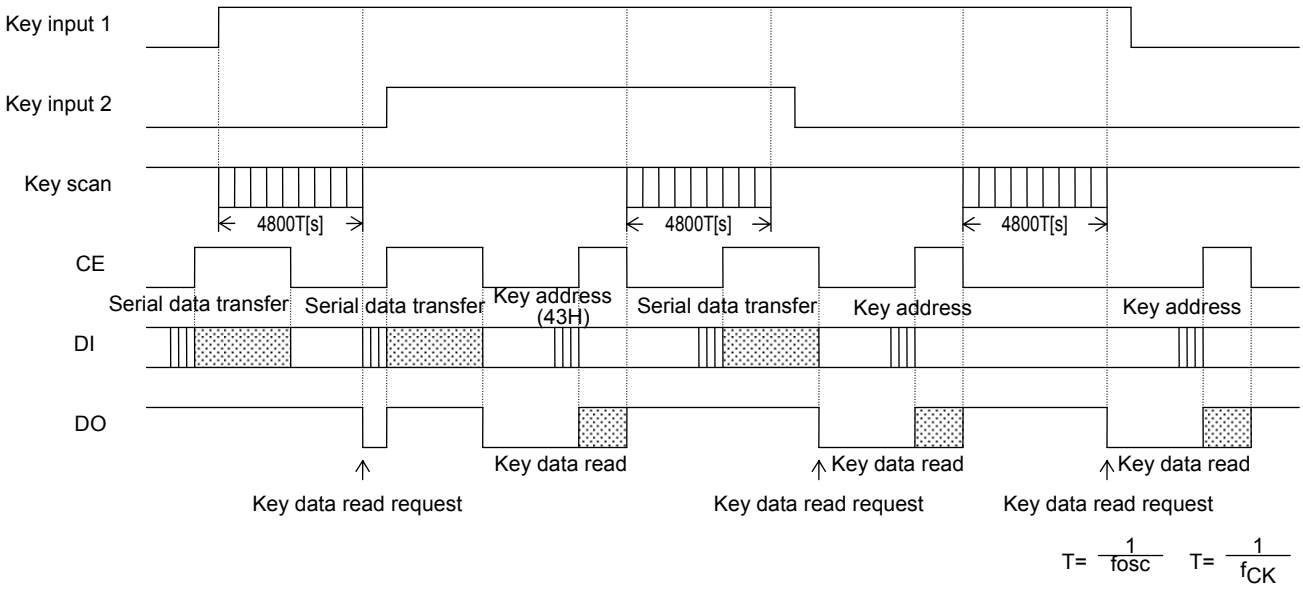
The key scan period is 2296T(s). To reliably determine the on/off state of the keys, the LC75812PT scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on DO) 4800T(s) after starting a key scan. If the key data dose not agree and a key was pressed at that point, it scans the keys again. Thus the LC75812PT cannot detect a key press shorter than 4800T(s).



Note: *22. Not that the high/low states of these pins are determined by the "set key scan output port/general-purpose output port state" instruction, and that key scan output signals are not output from pins that are set to low.

(2) In normal mode

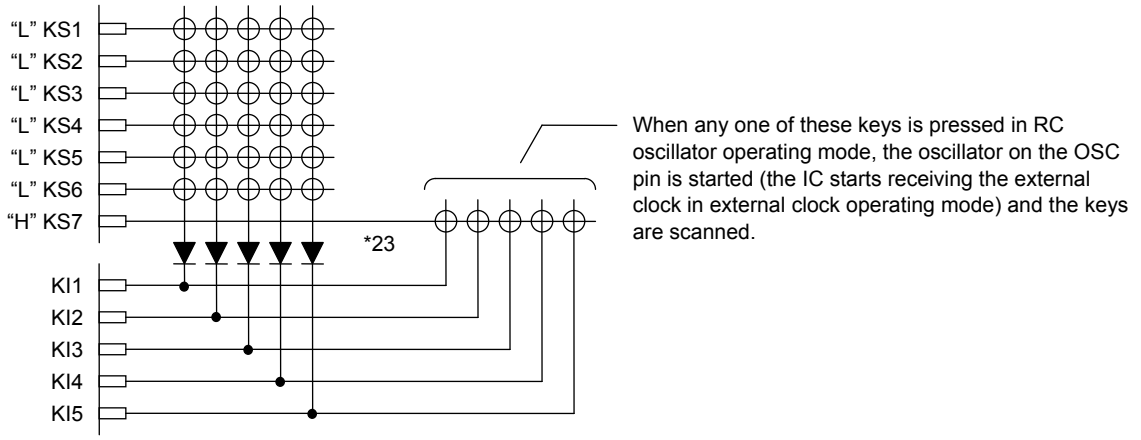
- The pins KS1 to KS7 are set to high or low with the "set key scan output port/general-purpose output port state" instruction.
- If a key on one of the lines corresponding to a KS1 to KS7 pin which is set high is pressed, a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than 4800T(s) (Where T=1/fosc, T=1/f_{CK}) the LC75812PT outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
- After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75812PT performs another key scan. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1kΩ and 10kΩ).



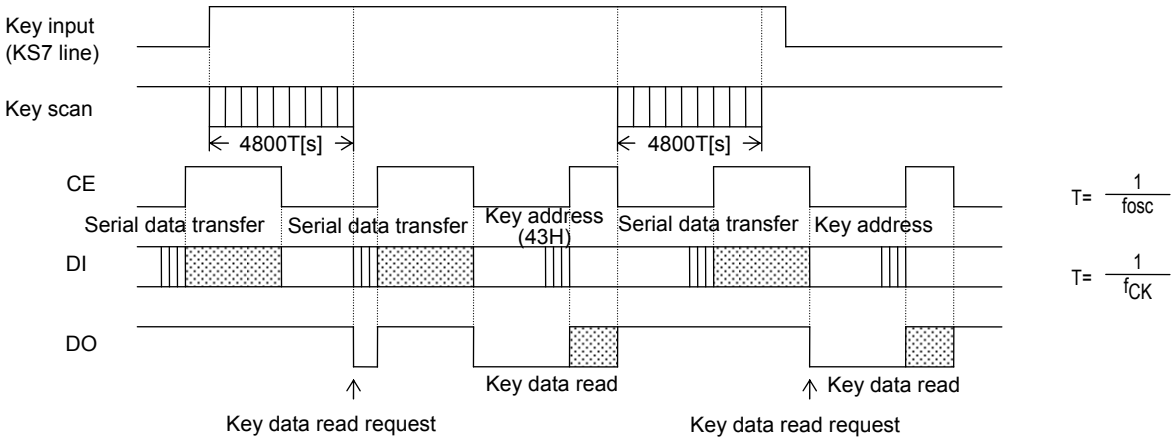
(3) In sleep mode

- The pins KS1 to KS7 are set to high or low with the "set key scan output port/general-purpose output port state" instruction.
- If a key on one of the lines corresponding to a KS1 to KS7 pin which is set high is pressed in the RC oscillator operating mode, the oscillator on the OSC pin is started (the IC starts receiving the external clock in external clock operating mode) and a key scan is performed . Keys are scanned until all keys released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than 4800T(s) (Where T=1/fosc, T=1/f_{CK}) the LC75812PT outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
- After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75812PT performs another key scan. However, this dose not clear sleep mode. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1kΩ and 10kΩ).
- Sleep mode key scan example

Example: When a "display on/off control (SP=1)" instruction and a "set key scan output port/general-purpose output port state (KP1 to KP3=0, KC1 to KC6= 0, KC7=1)" instruction are executed. (i.e. sleep mode with only KS7 high.)



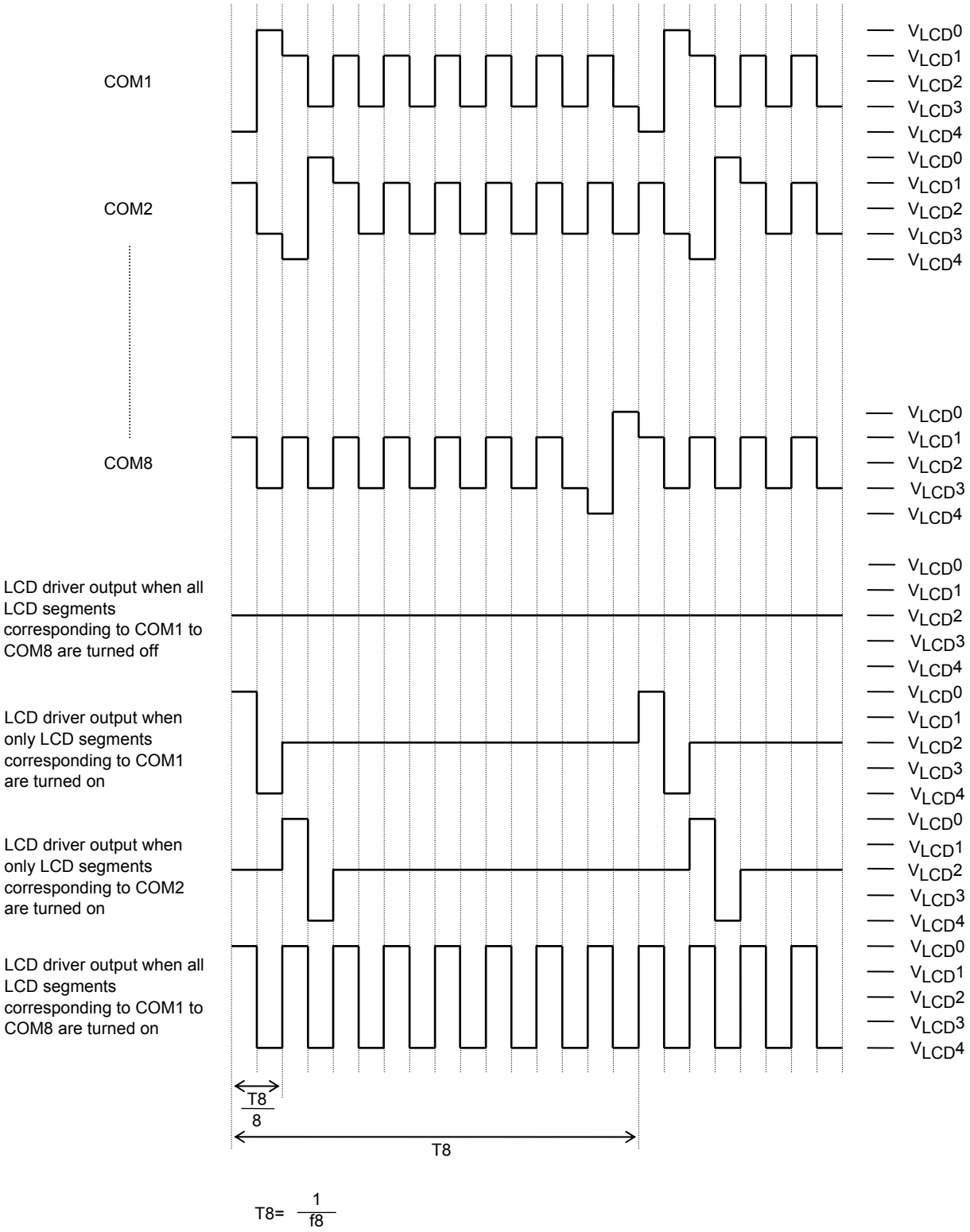
Note: *23. These diodes are required to reliably recognize multiple key presses on the KS7 line when sleep mode state with only KS7 high, as in the above example.
That is, these diodes prevent incorrect operations due to sneak currents in the KS7 key scan output signal when keys on the KS1 to KS6 lines are pressed at the same time.



Multiple Key Presses

Although the LC75812PT is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines, or multiple key presses on the KS1 to KS7 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed.
Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bits and ignore such data.

1/8 Duty, 1/4 Bias Drive Technique



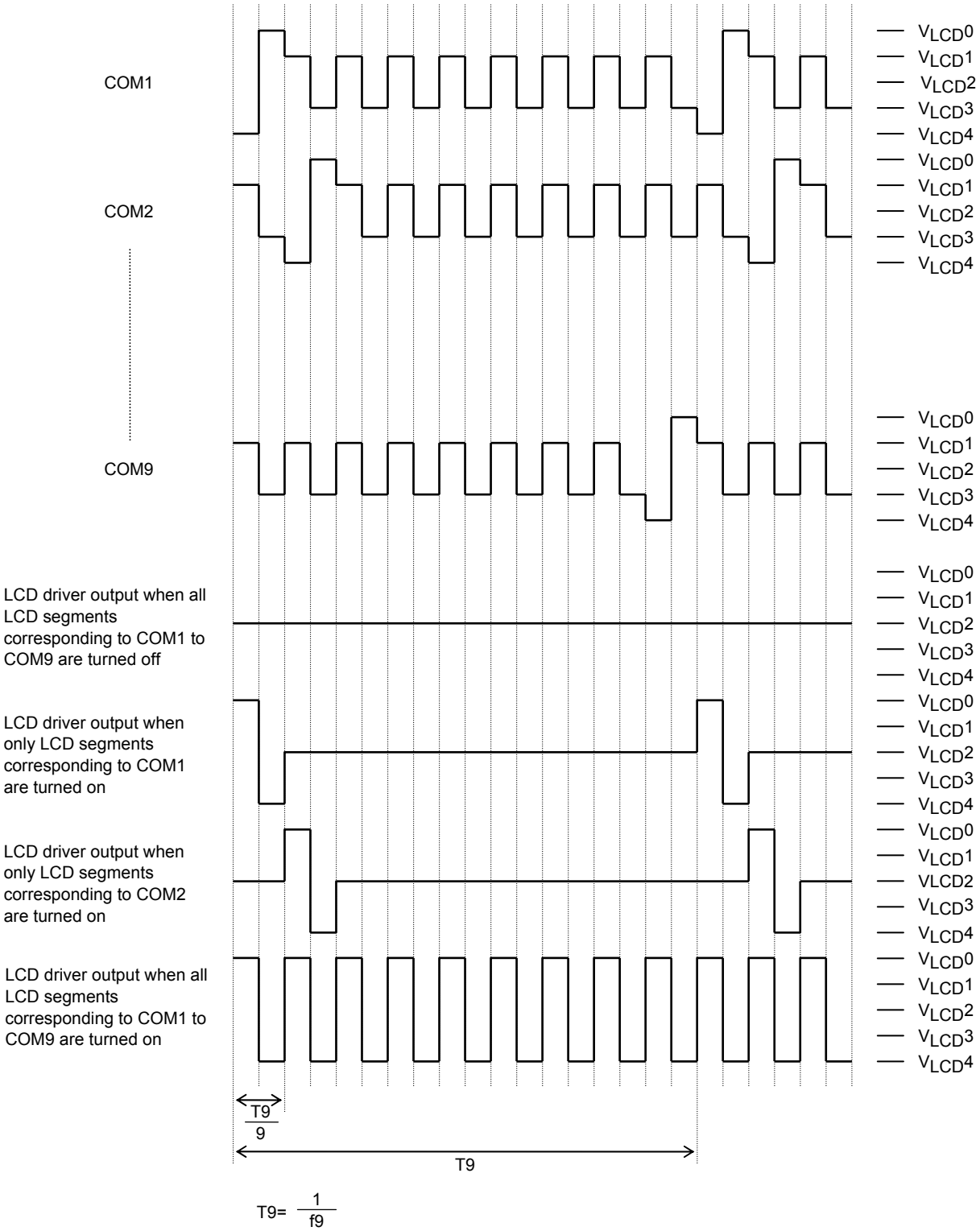
$$T8 = \frac{1}{f8}$$

When a "set display technique" instruction with FC0 = 0, FC1 = 0 are executed: $f8 = \frac{fosc}{3072}$, $f8 = \frac{f_{CK}}{3072}$

When a "set display technique" instruction with FC0 = 1, FC1 = 0 are executed: $f8 = \frac{fosc}{1536}$, $f8 = \frac{f_{CK}}{1536}$

When a "set display technique" instruction with FC0 = 0, FC1 =1 are executed: $f8 = \frac{fosc}{768}$, $f8 = \frac{f_{CK}}{768}$

1/9 Duty, 1/4 Bias Drive Technique

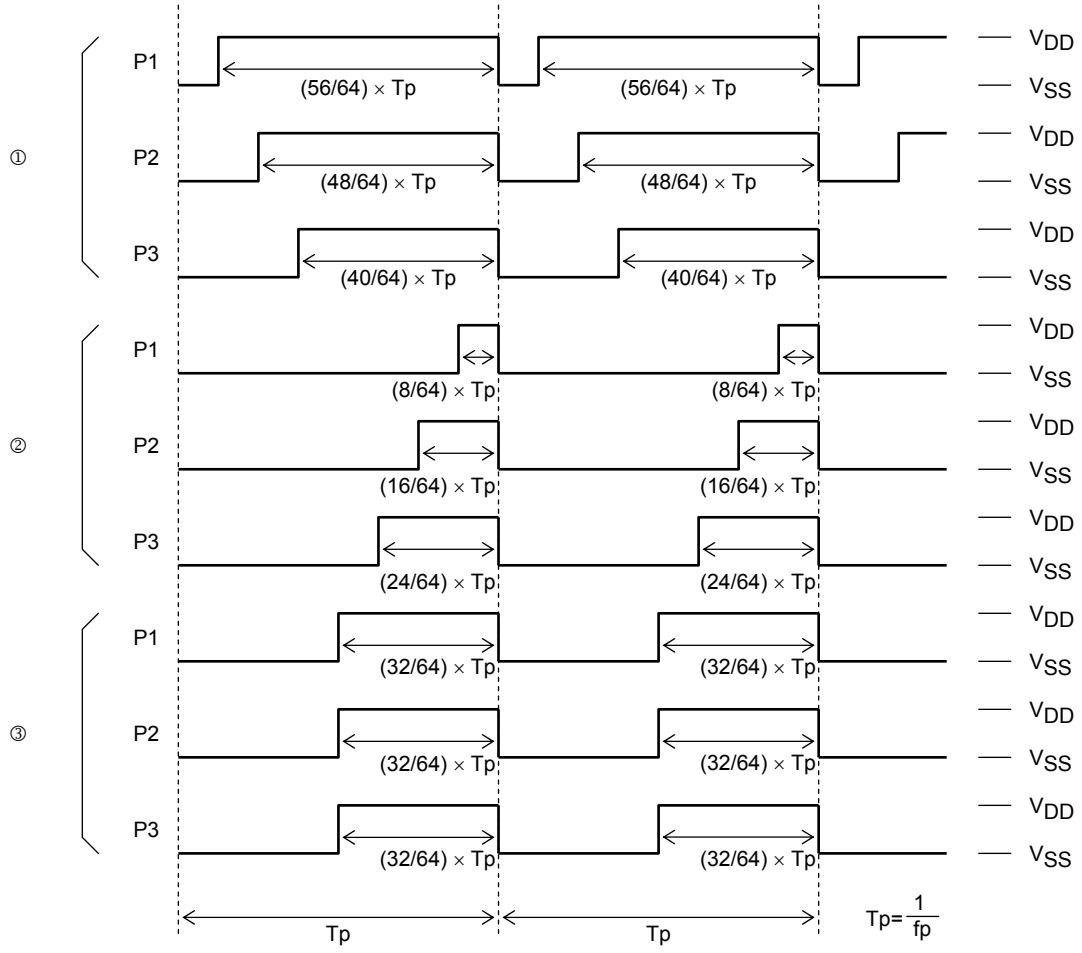


When a "set display technique" instruction with FC0 = 0, FC1 = 0 are executed: $f9 = \frac{fosc}{3456}$, $f9 = \frac{f_{CK}}{3456}$

When a "set display technique" instruction with FC0 = 1, FC1 = 0 are executed: $f9 = \frac{fosc}{1728}$, $f9 = \frac{f_{CK}}{1728}$

When a "set display technique" instruction with FC0 = 0, FC1 =1 are executed: $f9 = \frac{fosc}{864}$, $f9 = \frac{f_{CK}}{864}$

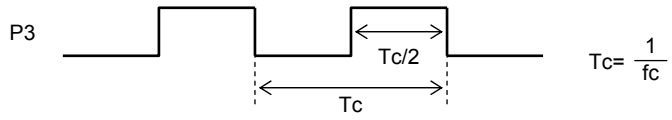
PWM Output Waveform



"Set key scan output port/general-purpose output port state" Instruction Data																		PWM Output Waveform of General-purpose Output Ports P1 to P3
W10	W11	W12	W13	W14	W15	W20	W21	W22	W23	W24	W25	W30	W31	W32	W33	W34	W35	
1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	0	0	1	①
1	1	1	0	0	0	1	1	1	1	0	0	1	1	1	0	1	0	②
1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	0	③

"Set key scan output port/general-purpose output port state" Instruction Data				PWM Output Waveform Frame Frequency fp[Hz]
PF0	PF1	PF2	PF3	
0	0	0	0	fosc/1536, fCK/1536
1	0	0	0	fosc/1408, fCK/1408
0	1	0	0	fosc/1280, fCK/1280
1	1	0	0	fosc/1152, fCK/1152
0	0	1	0	fosc/1024, fCK/1024
1	0	1	0	fosc/896, fCK/896
0	1	1	0	fosc/768, fCK/768
1	1	1	0	fosc/640, fCK/640
0	0	0	1	fosc/512, fCK/512
1	0	0	1	fosc/384, fCK/384
0	1	0	1	fosc/256, fCK/256

Clock Signal Output Waveform



"Set Key Scan Output Port/ General-purpose Port State" Instruction Data			General-purpose port P3 clock signal frequency fc (=1/Tc) [Hz]
PC30	PC31	PC32	
1	1	0	Clock signal output (fosc/2, f_{CK}/2)
0	0	1	Clock signal output (fosc/8, f_{CK}/8)

Voltage Detection Type Reset Circuit (V_{DET})

This circuit generates an output signal and resets the system when logic block power is first applied and when the voltage drops, i.e., when the logic block power supply voltage is less than or equal to the power down detection voltage V_{DET},which is 2.2 V, typical. To assure that this function operates reliably, a capacitor must be added to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when the logic block power is first applied and the logic block power supply voltage V_{DD} fall time when the voltage drops are both at least 1ms. (See Figure 5.)

Power Supply Sequence

The following sequences must be observed when power is turned on and off. (See Figure 5.)

- Power on: Logic block power supply(V_{DD}) on → LCD driver block power supply (V_{LCD}) on
- Power off: LCD driver block power supply(V_{LCD}) off → Logic block power supply (V_{DD}) off When 5 V signal is applied to the CE, CL, DI, and $\overline{INH}$ pins which are to be connected to the controller and if the logic block power supply (V_{DD}) is off, set the input voltage at the CE, CL, DI, and $\overline{INH}$ pins to 0 V and apply the 5 V signal to these pins after turning on the logic block power supply (V_{DD}).

System Reset

1. Reset function

The LC75812PT performs a system reset with the V_{DET}. When a system reset is applied, the display is turned off, key scanning is disabled, the key data is reset, and the general-purpose output ports are set to and held at the low level (V_{SS}).

These states that are created as a result of the system reset can be cleared by executing the instruction described below. (See Figure 5.)

- Clearing the display off state

Display operation can be enabled by executing a “display on/off control” instruction. However, since the contents of the DCRAM, ADRAM, and CGRAM are undefined, applications must set the contents of these memories before turning on display with the “display on/off control” instruction. That is, applications must execute the following instructions.

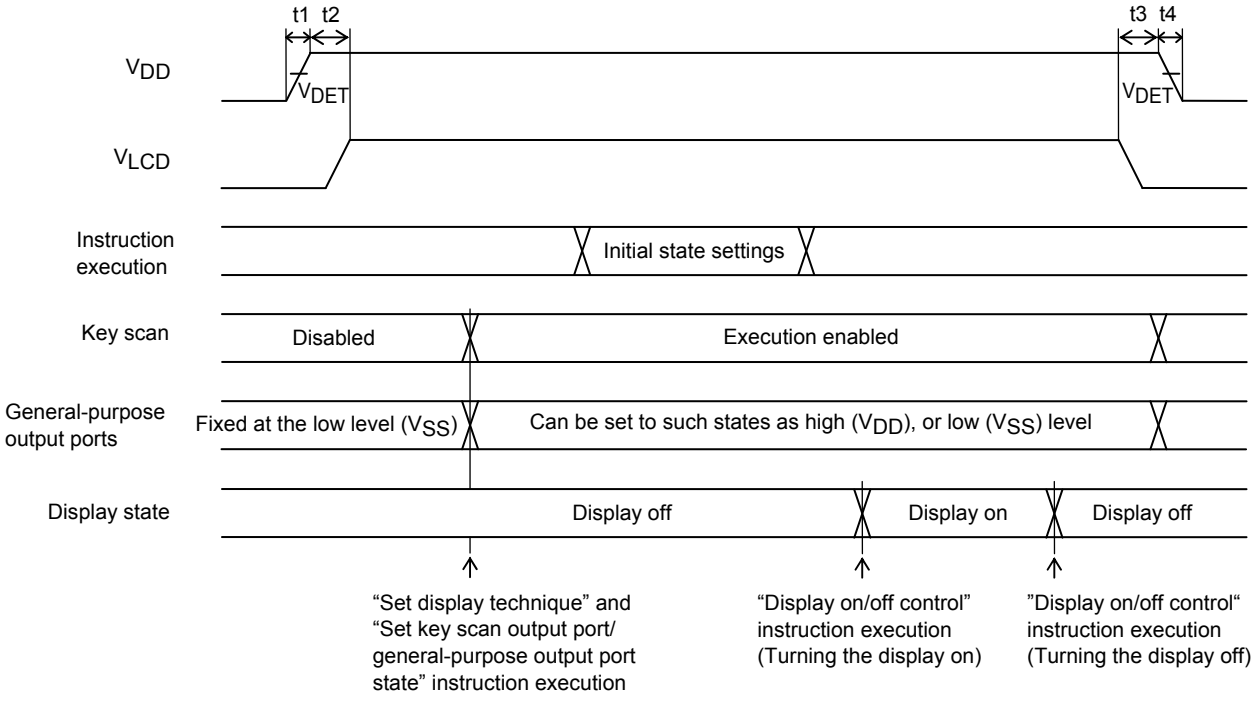
- Set display technique (The "set display technique" instruction must be executed first.)
- DCRAM data write
- ADRAM data write (If the ADRAM is used.)
- CGRAM data write (If the CGRAM is used.)
- Set AC address
- Set display contrast (If the display contrast adjustment circuit is used.)

After executing the above instructions, applications must turn on the display with a “display on/off control” instruction.

Note that when applications turn off in the normal mode, applications must turn off the display with a “display on/off control” instruction or the $\overline{INH}$ pin.

- Clearing the key scan disable and key data reset states
  By executing the following instructions not only create a state in which key scanning can be performed, but also clear the key data reset.
  - Set display technique (The "set display technique" instruction must be executed first.)
  - Set key scan output port/general-purpose output port state

- Clearing the general-purpose output ports locked at the low level (V_{SS}) state
  By executing the following instructions clear the general-purpose output ports locked at the low level (V_{SS}) state and set the states of the general-purpose output ports.
  - Set display technique (The "set display technique" instruction must be executed first.)
  - Set key scan output port/general-purpose output port state



- $t1 \geq 1$ [ms] (Logic block power supply voltage V_{DD} rise time)
- $t2 \geq 0$
- $t3 \geq 0$
- $t4 \geq 1$ [ms] (Logic block power supply voltage V_{DD} fall time)
- Initial state settings
  Set display technique (The "set display technique" instruction must be executed first.)
  DCRAM data write
  ADRAM data write (If the ADRAM is used.)
  CGRAM data write (If the CGRAM is used.)
  Set AC address
  Set display contrast (If the display contrast adjustment circuit is used.)

[Figure 5]

2. Block states during a system reset

(1) CLOCK GENERATOR,TIMING GENERATOR

When a reset is applied, these circuits are forcibly initialized internally. Then, when the "set display technique" instruction is executed, oscillation of the OSC pin starts in RC oscillator operating mode (the IC starts receiving the external clock in external clock operating mode), execution of the instruction is enabled.

(2) INSTRUCTION REGISTER, INSTRUCTION DECODER

When a reset is applied, these circuits are forcibly initialized internally. Then, when instruction execution starts, the IC operates according to those instructions.

(3) ADDRESS REGISTER, ADDRESS COUNTER

When a reset is applied, these circuits are forcibly initialized internally. Then, the DCRAM and the ADRAM addresses are set when “Set AC address” instruction is executed.

(4) DCRAM, ADRAM, CGRAM

Since the contents of the DCRAM, ADRAM, and CGRAM become undefined during a reset, applications must execute “DCRAM data write”, “ADRAM data write (If the ADRAM is used.)”, and “CGRAM data write (If the CGRAM is used.)” instructions before executing a “display on/off control” instruction.

(5) CGROM

Character patterns are stored in this ROM.

(6) LATCH

Although the value of the data in the latch is undefined during a reset, the ADRAM, CGROM, and CGRAM data is stored by executing a “display on/off control” instruction.

(7) COMMON DRIVER, SEGMENT DRIVER

These circuits are forced to the display off state when a reset is applied.

(8) CONTRAST ADJUSTER

Display contrast adjustment circuit operation is disabled when a reset is applied. After that, the display contrast can be set by executing a “set display contrast” instruction.

(9) KEY SCAN, KEY BUFFER

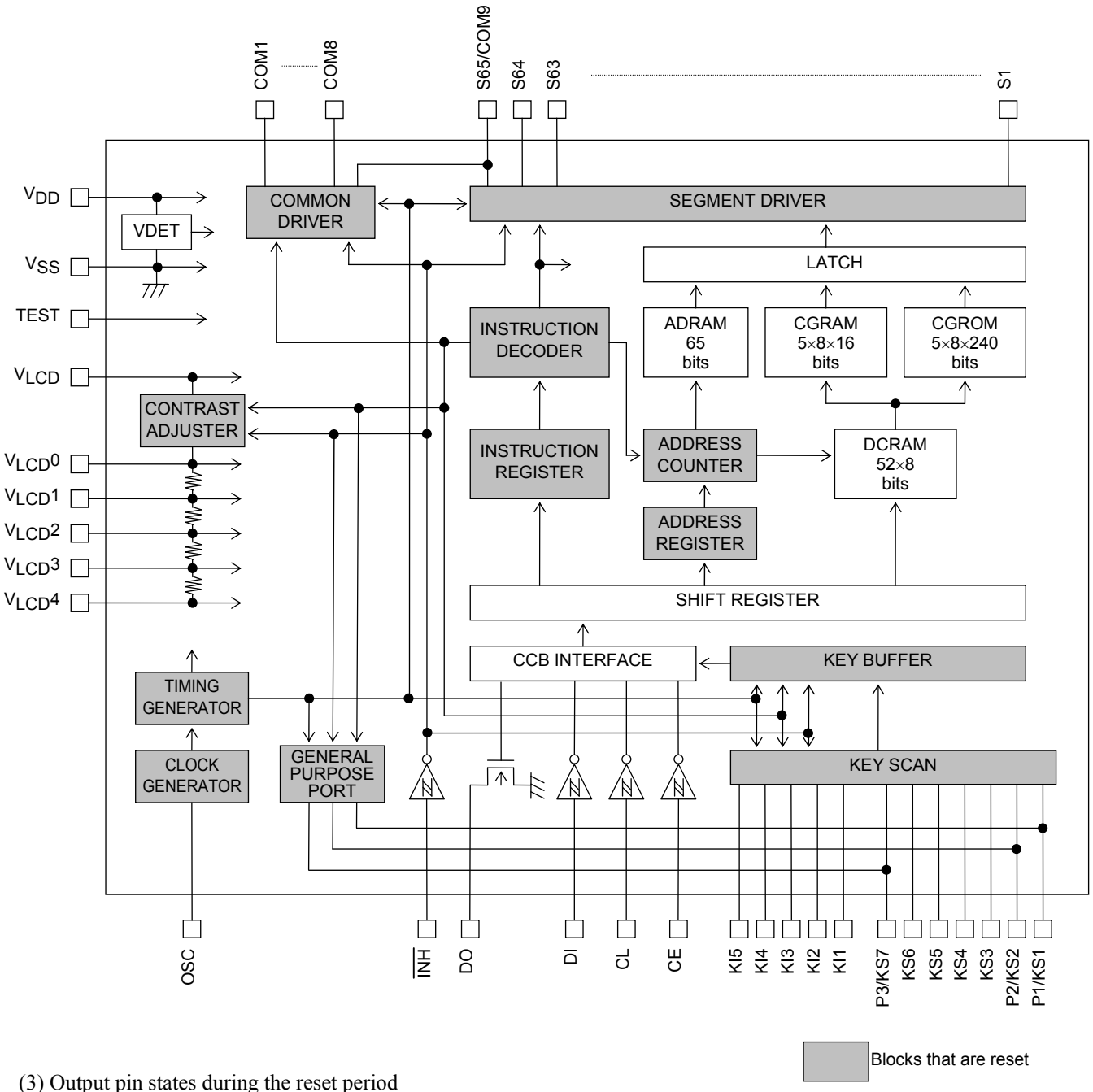
When a reset is applied, these circuits are forcibly initialized internally, and key scan operation is disabled. Also, the key data is all set to 0. After that, key scanning can be performed by executing a "set key scan output port/general-purpose output port state" instruction.

(10) GENERAL PURPOSE PORT

When a reset is applied, the general-purpose output port state is locked at the low level (V_{SS}).

(11) CCB INTERFACE, SHIFT REGISTER

These circuits go to the serial data input wait state.



(3) Output pin states during the reset period

Output pin	State during reset	
S1 to S64	L ($V_{LCD}4$)	
S65/COM9	L ($V_{LCD}4$)	*24
COM1 to COM8	L ($V_{LCD}4$)	
KS1/P1, KS2/P2	L (V_{SS})	*25
KS3 to KS6	L (V_{SS})	
KS7/P3	L (V_{SS})	*25
OSC	Z (high-impedance)	*26
DO	H	*27

*24 This output pin is forcibly set to the segment output function and held low ($V_{LCD}4$). If the "set display technique" instruction is executed, however, either segment output or common output is selected according to the instruction.

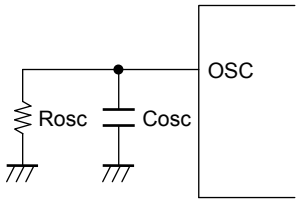
*25 This output pin is forcibly set to general-purpose output port and held low (V_{SS}). If the “set display technique” and the "set key scan output port/general-purpose output port state" instructions are executed, however, either key scan output port or general-purpose output port is selected according to the instructions.

*26 This I/O pin is forcibly set to the high-impedance state.

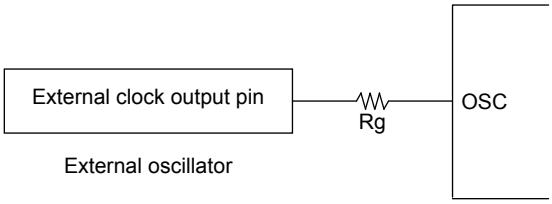
*27 Since this output pin is an open-drain output, a pull-up resistor (between 1 kΩ and 10 kΩ) is required. This pin is held at the high level even if a key data read operation is performed before executing the "set display technique" or "set key scan output port/general-purpose output port state" instruction.

OSC Pin Peripheral Circuit

(1) RC oscillator operating mode (when the "set display technique (OC=0)" instruction is executed)
When RC oscillator operating mode is selected, an external resistor Rosc and an external capacitor Cosc must be connected between the OSC pin and GND.



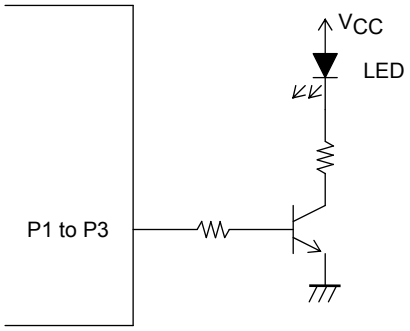
(2) External clock operating mode (when the "set display technique (OC=1)" instruction is executed)
When selecting the external clock operating mode, connect a current protection resistor Rg (2.2 to 22 kΩ) between the OSC pin and external clock output pin (external oscillator). Determine the value of the resistance according to the maximum allowable current value at the external clock output pin. Also make sure that the waveform of the external clock is not heavily distorted.



Note: *28. Allowable current value at external clock output pin > $\frac{V_{DD}}{Rg}$

Pins P1 to P3 peripheral circuit

It is recommended that the following circuit be used when adjusting the brightness of the LED backlight in PWM mode using the general-purpose output ports P1 to P3 (when PWM signal output function is selected with the general-purpose output ports P1 to P3 under the "set key scan output port/general-purpose output port state" instruction):

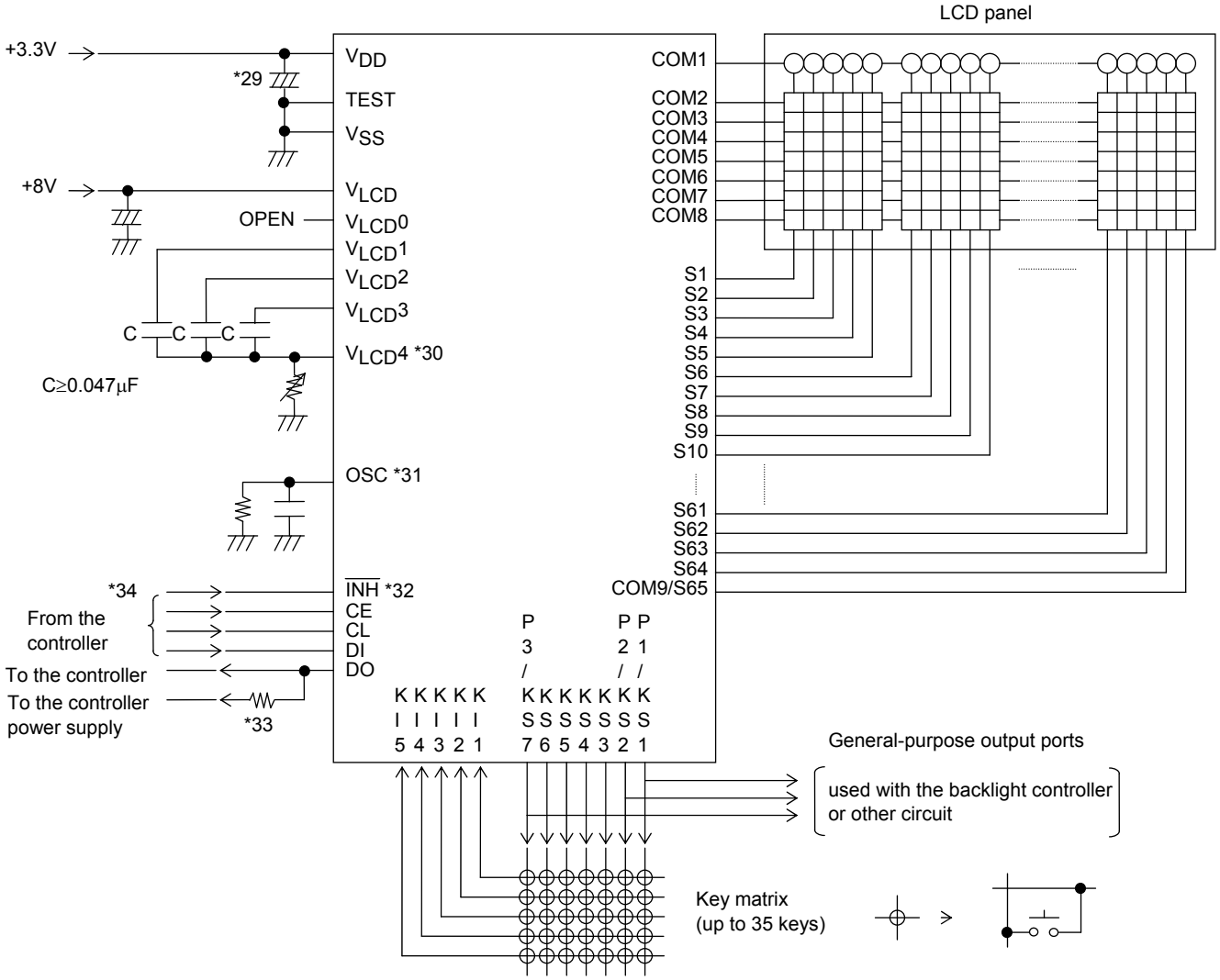


Note when applying a 5 V signal to the CE, CL, DI, and $\overline{INH}$ pins

When applying a 5V signal to the CE, CL, DI, and $\overline{INH}$ pins which are to be connected to the controller, set the input voltage to the CE, CL, DI, and $\overline{INH}$ pins to 0 V if the logic block power supply (V_{DD}) is off, and apply the 5 V signal to those pins after turning on the logic block power supply (V_{DD}).

Sample Application Circuit 1

1/8 duty, 1/4 bias drive technique (for use with normal panels)



Note *29. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75812PT is reset by the V_{DET}.

*30. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*31. In RC oscillator operating mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. When selecting the external clock operating mode, connect a current protection resistor Rg (2.2 to 22 kΩ) between the OSC pin and the external clock output pin (external oscillator). (See the "OSC Pin Peripheral Circuit" section.)

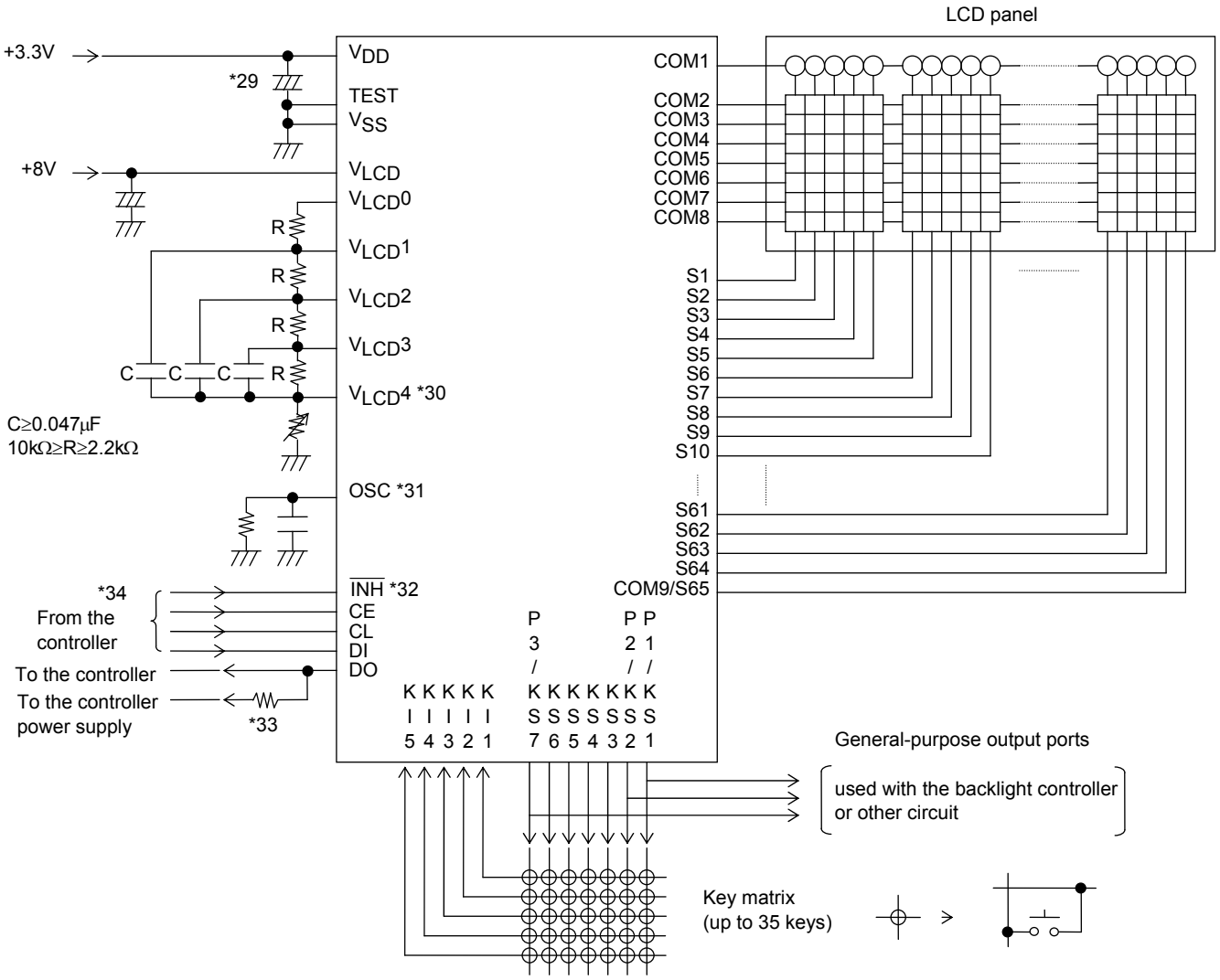
*32. If the function of $\overline{INH}$ pin is not used, the $\overline{INH}$ pin must be connected to the logic block power supply V_{DD}.

*33. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 kΩ and 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

*34 When applying a 5 V signal to the CE, CL, DI, and $\overline{INH}$ pins, set the input voltage to 0 V if the logic block power supply (V_{DD}) is off and apply the 5 V signal to those pins after turning on the logic block power supply (V_{DD}).

Sample Application Circuit 2

1/8 duty, 1/4 bias drive technique (for use with large panels)



Note *29. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75812PT is reset by the V_{DET}.

*30. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*31. In RC oscillator operating mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. When selecting the external clock operating mode, connect a current protection resistor Rg (2.2 to 22 kΩ) between the OSC pin and the external clock output pin (external oscillator). (See the "OSC Pin Peripheral Circuit" section.)

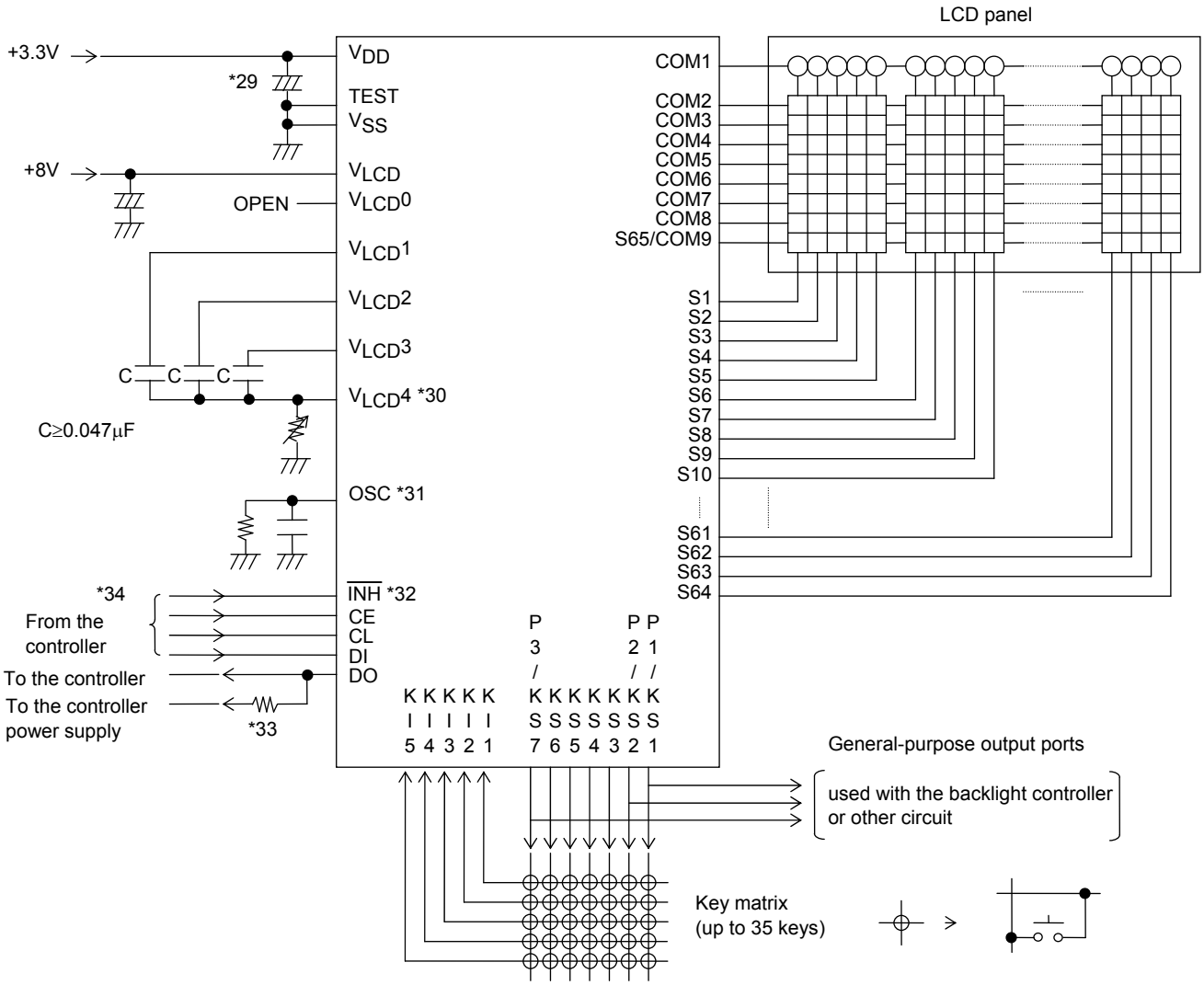
*32. If the function of $\overline{INH}$ pin is not used, the $\overline{INH}$ pin must be connected to the logic block power supply V_{DD}.

*33. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 kΩ and 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

*34 When applying a 5 V signal to the CE, CL, DI, and $\overline{INH}$ pins, set the input voltage to 0 V if the logic block power supply (V_{DD}) is off and apply the 5 V signal to those pins after turning on the logic block power supply (V_{DD}).

Sample Application Circuit 3

1/9 duty, 1/4 bias drive technique (for use with normal panels)



Note *29. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75812PT is reset by the V_{DET}.

*30. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*31. In RC oscillator operating mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. When selecting the external clock operating mode, connect a current protection resistor Rg (2.2 to 22 kΩ) between the OSC pin and the external clock output pin (external oscillator). (See the "OSC Pin Peripheral Circuit" section.)

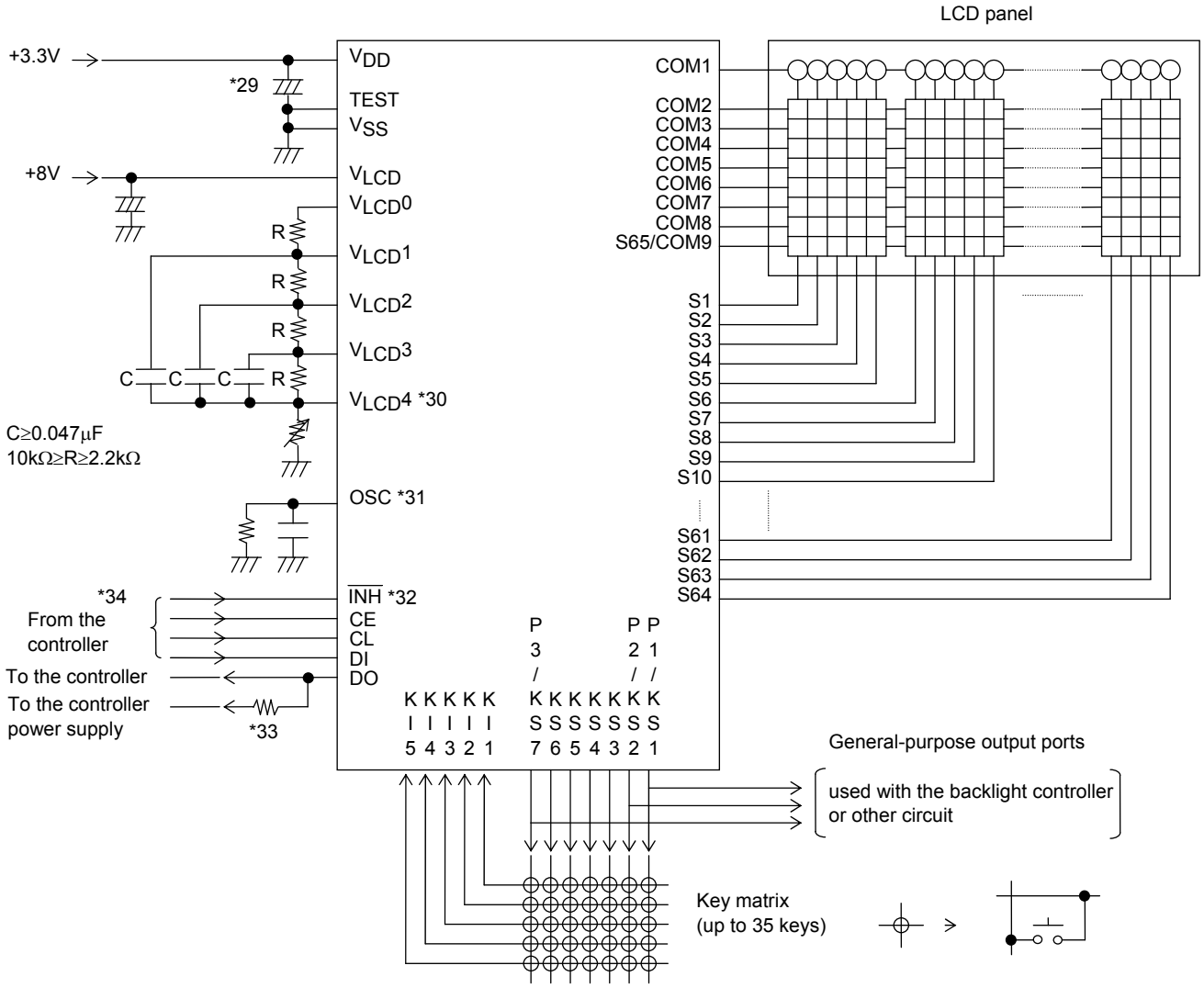
*32. If the function of $\overline{INH}$ pin is not used, the $\overline{INH}$ pin must be connected to the logic block power supply V_{DD}.

*33. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 kΩ and 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

*34 When applying a 5 V signal to the CE, CL, DI, and $\overline{INH}$ pins, set the input voltage to 0 V if the logic block power supply (V_{DD}) is off and apply the 5 V signal to those pins after turning on the logic block power supply (V_{DD}).

Sample Application Circuit 4

1/9 duty, 1/4 bias drive technique (for use with large panels)



Note *29. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75812PT is reset by the V_{DET}.

*30. If a variable resistor is not used for display contrast fine adjustment, the $V_{LCD}4$ pin must be connected to ground.

*31. In RC oscillator operating mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. When selecting the external clock operating mode, connect a current protection resistor Rg (2.2 to 22 kΩ) between the OSC pin and the external clock output pin (external oscillator). (See the "OSC Pin Peripheral Circuit" section.)

*32. If the function of $\overline{INH}$ pin is not used, the $\overline{INH}$ pin must be connected to the logic block power supply V_{DD}.

*33. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 kΩ and 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

*34 When applying a 5 V signal to the CE, CL, DI, and $\overline{INH}$ pins, set the input voltage to 0 V if the logic block power supply (V_{DD}) is off and apply the 5 V signal to those pins after turning on the logic block power supply (V_{DD}).

Sample Correspondence between Instructions and the Display (When the LC75812PT-8565 is used)

No.	LSB Instruction (hexadecimal) MSB D96 to D99	D100 to D103	D104 to D107	D108 to D111	D112 to D115	D116 to D119	Display	Operation
1	Power application (Initialization with the V_{DET})							Initializes the IC. The display is in the off state.
2	Set display technique				0	8		Sets to 1/8 duty 1/4 bias display drive technique
3	DCRAM data write (normal increment mode)							
	0	2	0	0	1	A		Writes the display data " " to DCRAM address 00H
4	DCRAM data write (normal increment mode)							
					3	5		Writes the display data "S" to DCRAM address 01H
5	DCRAM data write (normal increment mode)							
					1	4		Writes the display data "A" to DCRAM address 02H
6	DCRAM data write (normal increment mode)							
					E	4		Writes the display data "N" to DCRAM address 03H
7	DCRAM data write (normal increment mode)							
					9	5		Writes the display data "Y" to DCRAM address 04H
8	DCRAM data write (normal increment mode)							
					F	4		Writes the display data "O" to DCRAM address 05H
9	DCRAM data write (normal increment mode)							
					0	2		Writes the display data " " to DCRAM address 06H
10	DCRAM data write (normal increment mode)							
					C	4		Writes the display data "L" to DCRAM address 07H
11	DCRAM data write (normal increment mode)							
					3	5		Writes the display data "S" to DCRAM address 08H
12	DCRAM data write (normal increment mode)							
					9	4		Writes the display data "I" to DCRAM address 09H
13	DCRAM data write (normal increment mode)							
					0	2		Writes the display data " " to DCRAM address 0AH
14	DCRAM data write (normal increment mode)							
					C	4		Writes the display data "L" to DCRAM address 0BH
15	DCRAM data write (normal increment mode)							
					3	4		Writes the display data "C" to DCRAM address 0CH
16	DCRAM data write (normal increment mode)							
					7	3		Writes the display data "7" to DCRAM address 0DH
17	DCRAM data write (normal increment mode)							
					5	3		Writes the display data "5" to DCRAM address 0EH
18	DCRAM data write (normal increment mode)							
					8	3		Writes the display data "8" to DCRAM address 0FH
19	DCRAM data write (normal increment mode)							
					1	3		Writes the display data "1" to DCRAM address 10H
20	DCRAM data write (normal increment mode)							
					2	3		Writes the display data "2" to DCRAM address 11H
21	DCRAM data write (normal increment mode)							
		0	2	0	A			Writes the display data " " to DCRAM address 12H

Continued on next page.

Continued from preceding page.

No.	LSB D96 to D99	D100 to D103	D104 to D107	D108 to D111	D112 to D115	MSB D116 to D119	Display	Operation
	Instruction (hexadecimal)							
22	Set AC address							Loads the DCRAM address 00H and the ADRAM address 0H into AC
			0	0	0	2		
23	Display on/off control						SANYO LSI LC	Turns on the LCD for all digits (13 digits) in MDATA
	F	F	F	1	1	4		
24	Display shift						SANYO LSI LC7	Shifts the display (MDATA only) to the left
					1	C		
25	Display shift						ANYO LSI LC75	Shifts the display (MDATA only) to the left
					1	C		
26	Display shift						NYO LSI LC758	Shifts the display (MDATA only) to the left
					1	C		
27	Display shift						YO LSI LC7581	Shifts the display (MDATA only) to the left
					1	C		
28	Display shift						O LSI LC75812	Shifts the display (MDATA only) to the left
					1	C		
29	Display shift						LSI LC75812	Shifts the display (MDATA only) to the left
					1	C		
30	Display on/off control							Set to sleep mode, turns off the LCD for all digits
	0	0	0	0	8	4		
31	Display on/off control						LSI LC75812	Turns on the LCD for all digits (13 digits) in MDATA
	F	F	F	1	1	4		
32	Set AC address						SANYO LSI LC	Loads the DCRAM address 00H and the ADRAM address 0H into AC
			0	0	0	2		

*35) The sample correspondence between the instructions and the display assumes the use of 13 digits×1 row 5×7 dot matrix LCD. Neither CGRAM nor ADRAM are used.

*36) Given below are the data formats of the "DCRAM data write" instructions (No. 3 to No. 21) for the sample correspondence between the instructions and the display executed in the super increment mode. In the super increment mode processing example shown below, 19 characters of DCRAM data is divided and written into DCRAM in two operations.

No.	Instruction (HEX) LSB											MSB
	D0 to D3	D4 to D7	D8 to D11	D12 to D15	D16 to D19	D20 to D23	D24 to D27	D28 to D31	D32 to D35	D36 to D39	D40 to D43	D44 to D47
3 to 15	DCRAM data write (Super increment mode)											
	0	2	3	5	1	4	E	4	9	5	F	4
16 to 21	DCRAM data write (Super increment mode)											

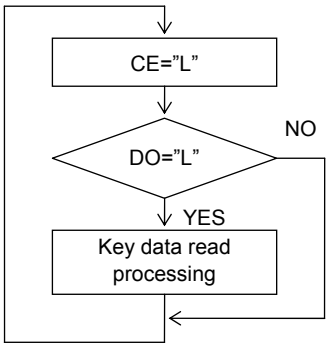
No.	Instruction (HEX) LSB											MSB
	D48 to D51	D52 to D55	D56 to D59	D60 to D63	D64 to D67	D68 to D71	D72 to D75	D76 to D79	D80 to D83	D84 to D87	D88 to D91	D92 to D95
3 to 15	DCRAM data write (Super increment mode)											
	0	2	C	4	3	5	9	4	0	2	C	4
16 to 21	DCRAM data write (Super increment mode)											
			7	3	5	3	8	3	1	3	2	3

No.	Instruction (HEX) LSB					MSB	Operation
	D96 to D99	D100 to D103	D104 to D107	D108 to D111	D112 to D115	D116 to D119	
3 to 15	DCRAM data write (Super increment mode)						Display data " " "S" "A" "N" "Y" "O" " " "L" "S" "I" " " "L" "C" are written sequentially to DCRAM addresses 00H to 0CH.
	3	4	0	0	2	A	
16 to 21	DCRAM data write (Super increment mode)						Display data "7" "5" "8" "1" "2" " " are written sequentially to DCRAM addresses 0DH to 12H.
	0	2	D	0	2	A	

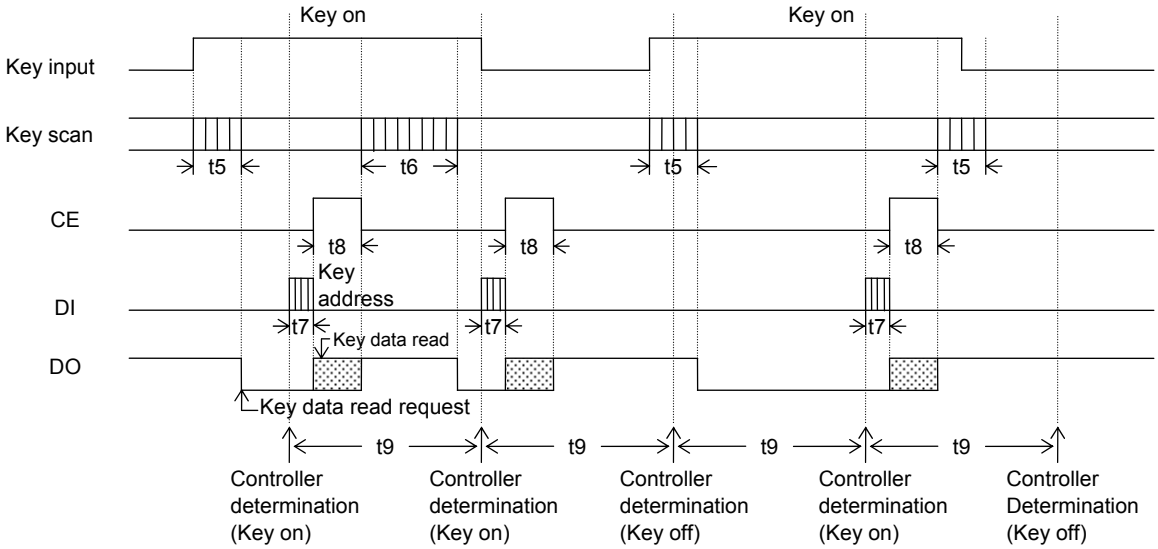
Notes on the controller key data read techniques

1. Timer based key data acquisition

- Flowchart



- Timing chart



t5: Key scan execution time when the key data agreed for two key scans. (4800T(s))
t6: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (9600T(s))
t7: Key address (43H) transfer time
t8: Key data read time

$T=\frac{1}{fosc}$ $T=\frac{1}{f_{CK}}$

- Explanation

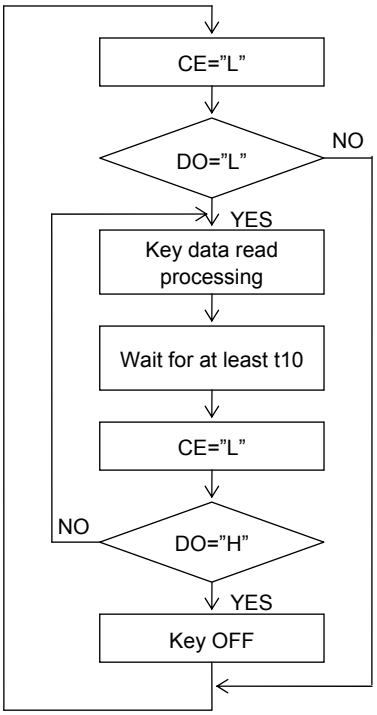
In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the DO state when CE is low every t9 period without fail. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation.
The period t9 in this technique must satisfy the following condition.

t9>t6+t7+t8

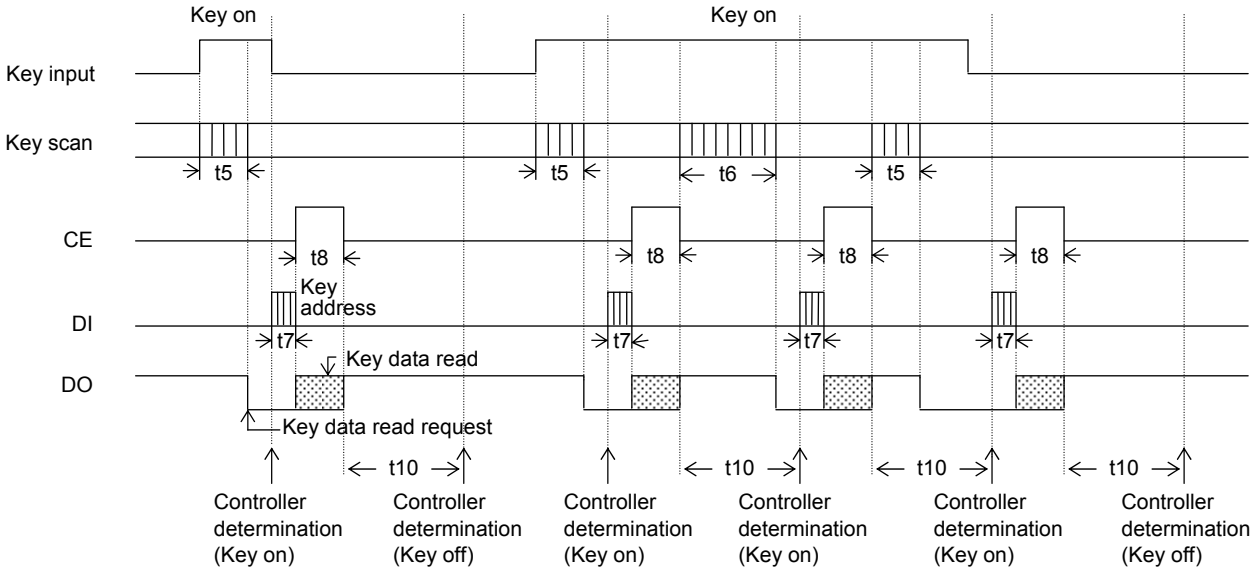
When key data read operation is executed with DO set high (no key data read request present), the key data (KD1 to KD35) and sleep acknowledge data (SA) are invalid.

2. Interrupt based key data acquisition

- Flowchart



- Timing chart



t5: Key scan execution time when the key data agreed for two key scans. (4800T(s))
t6: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (9600T(s))
t7: Key address (43H) transfer time
t8: Key data read time

$T=\frac{1}{fosc}$ $T=\frac{1}{f_{CK}}$

- Explanation

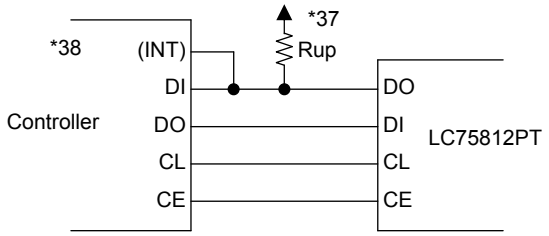
In this technique, the controller uses interrupts to determine key on/off states and read the key data. The controller must check the DO state when CE is low. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time t10 has elapsed by checking the DO state when CE is low and reading the key data. The period t10 in this technique must satisfy the following condition.

t10 > t6

When key data read operation is executed with DO set high (no key data read request present), the key data (KD1 to KD35) and sleep acknowledge data (SA) are invalid.

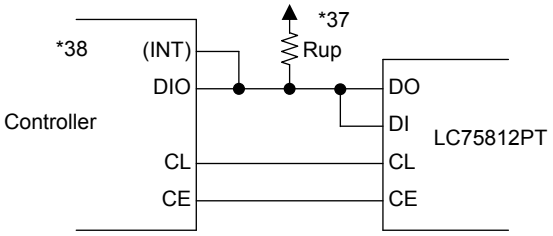
About Data Communication Method with The Controller

1. About data communication method of 4 line type CCB format
   The 4 line type CCB format is the data communication method of before. The LC75812PT must connect to the controller as followings.



Note: *37. Connect the pull-up resistor Rup. Select a resistance (between 1 to 10kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.
*38. The (INT) pin is an input port for the key data read request signal (a low level on DO) detection.

2. About data communication method of 3 line type CCB format
   The 3 line type CCB format is the data communication method that made a common use of the data input DI in the data output DO. The LC75812PT must connect to the controller as followings.

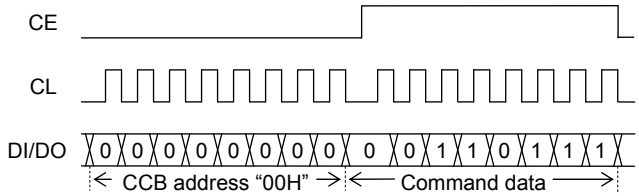


Note: *37. Connect the pull-up resistor Rup. Select a resistance (between 1 to 10kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.
*38. The (INT) pin is an input port for the key data read request signal (a low level on DO) detection.

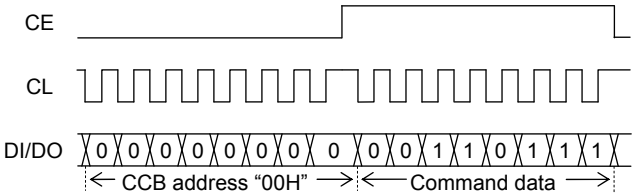
In this case, Applications must transfer the data communication start command before the serial data input (CCB address “42H”, display data and control data transfer) or serial data output (CCB address “43H” transfer, key data read) to avoid the collision of the data input signal DI and the data output signal DO.
Then applications must transfer the data communication stop command when the controller wants to detect the key data read request signal (a low level on DO) during a movement stop of the serial data input and the serial data output.

<1> Data communication start command

(1) When CL is stoped at the low level

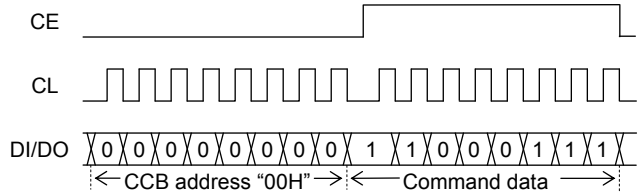


(2) When CL is stoped at the high level

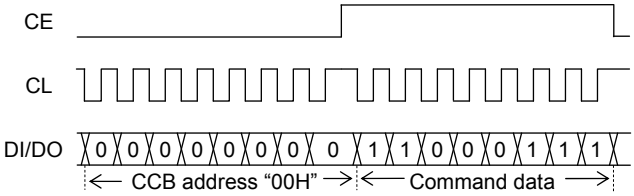


<2> Data communication stop command

(1) When CL is stoped at the low level

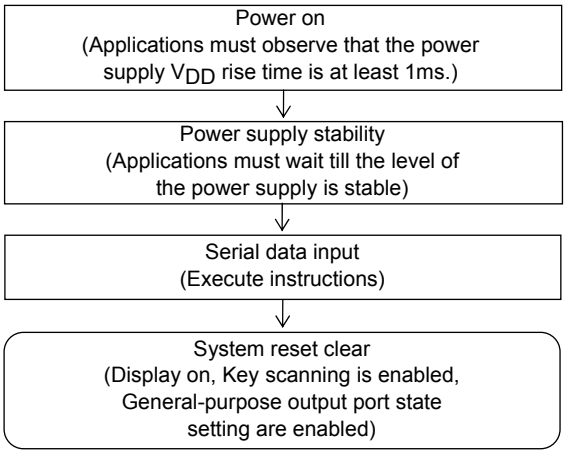


(2) When CL is stoped at the high level



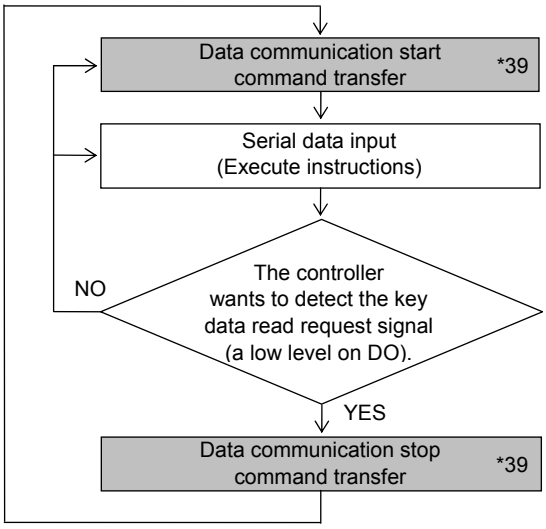
Data Communication Flowchart of 4 Line Type or 3 Line Type CCB Format

1. Flowchart of the initial setting when power is turned on.



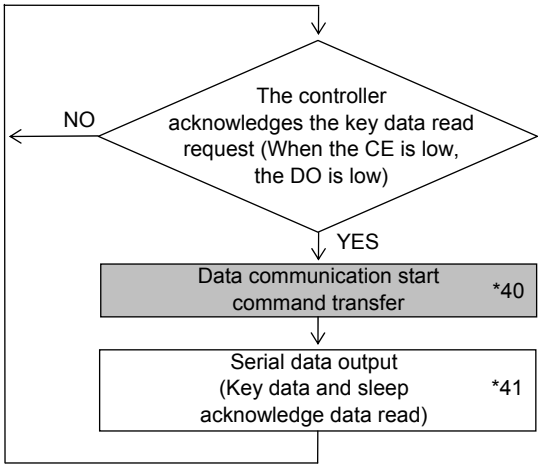
Note: The flowchart for power-on time initialization is the same for the 4- and 3-wire CCB formats. See "Power Supply Sequence" and "System Reset."

2. Flowchart of the serial data input



Note: *39. In the case of the 4 line type CCB format, the transfers of data communication start command and data communication stop command are unnecessary, and, in the case of the 3 line type CCB format, these transfers are necessary.

3. Flowchart of the serial data output



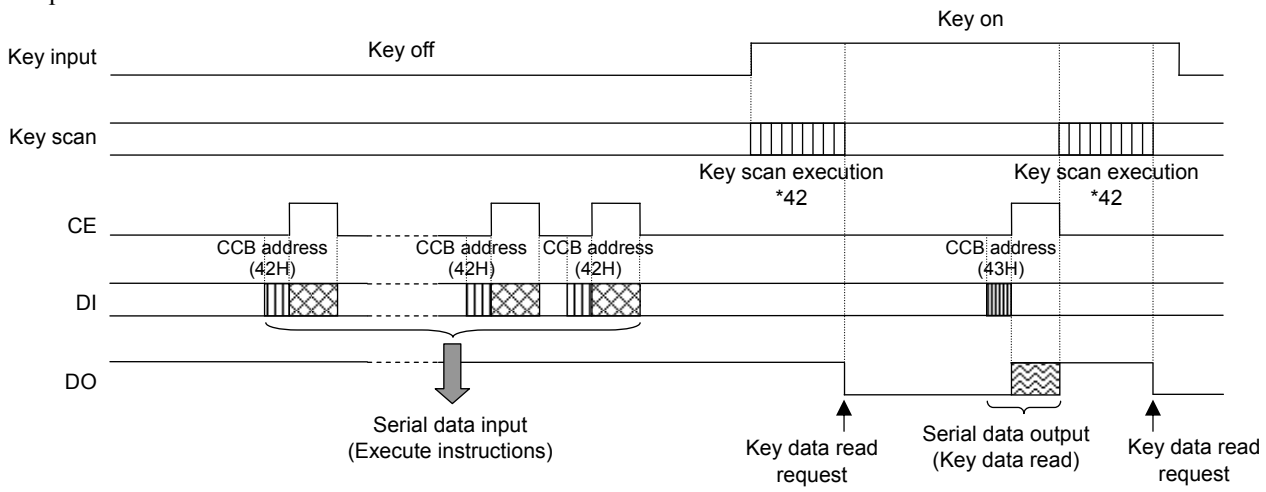
Note: *40. In the case of the 4 line type CCB format, the transfer of data communication start command is unnecessary, and, in the case of the 3 line type CCB format, the transfer is necessary.

*41. Because the serial data output has the role of the data communication stop command, it is not necessary to transfer the data communication stop command some other time.

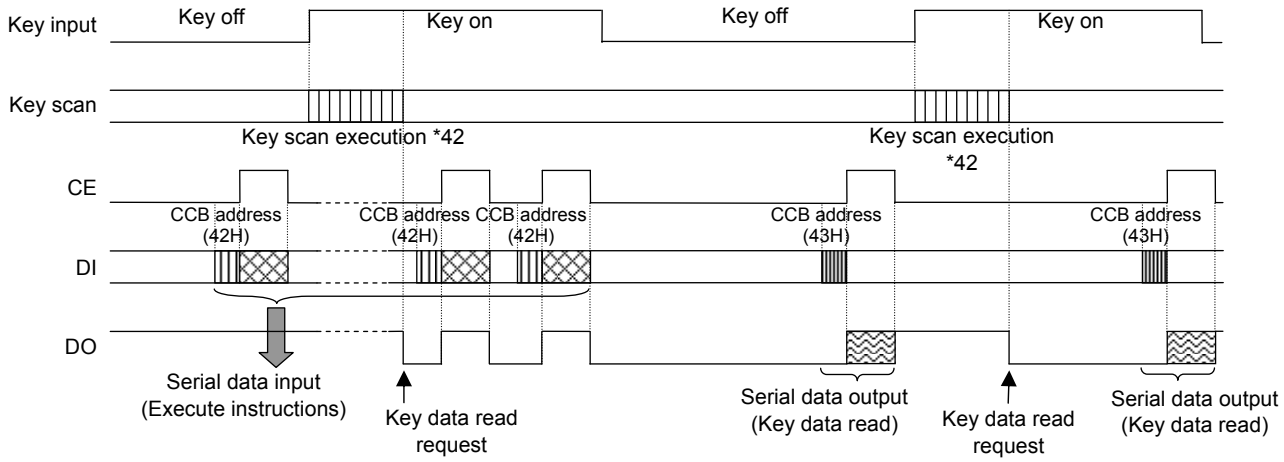
Timing Chart of 4 Line Type and 3 Line Type CCB Format

1. Timing chart of 4 line type CCB format

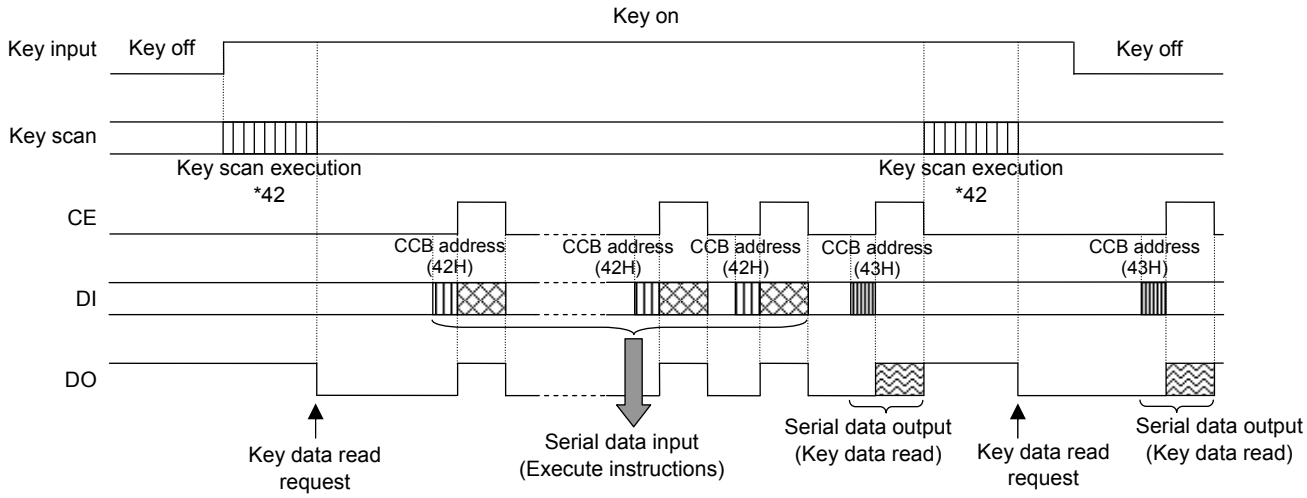
<Example 1>



<Example 2>



<Example 3>

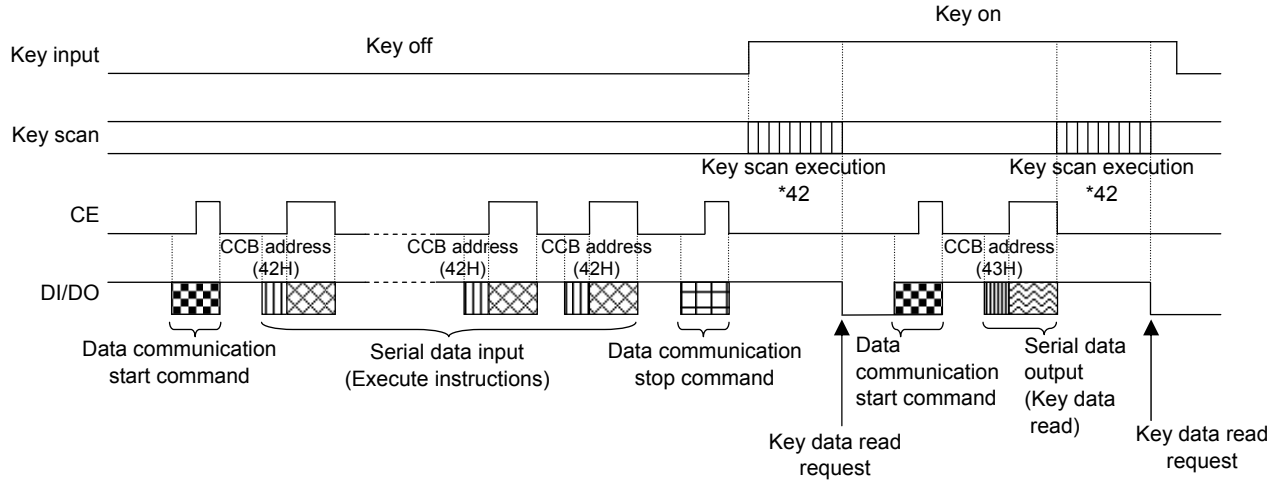


Note: *42. When the key data agrees for two key scans, the key scan execution time is 4800T[s].
And, when the key data does not agree for two key scans and the key scan is executed again, the key scan execution time is 9600T[s].

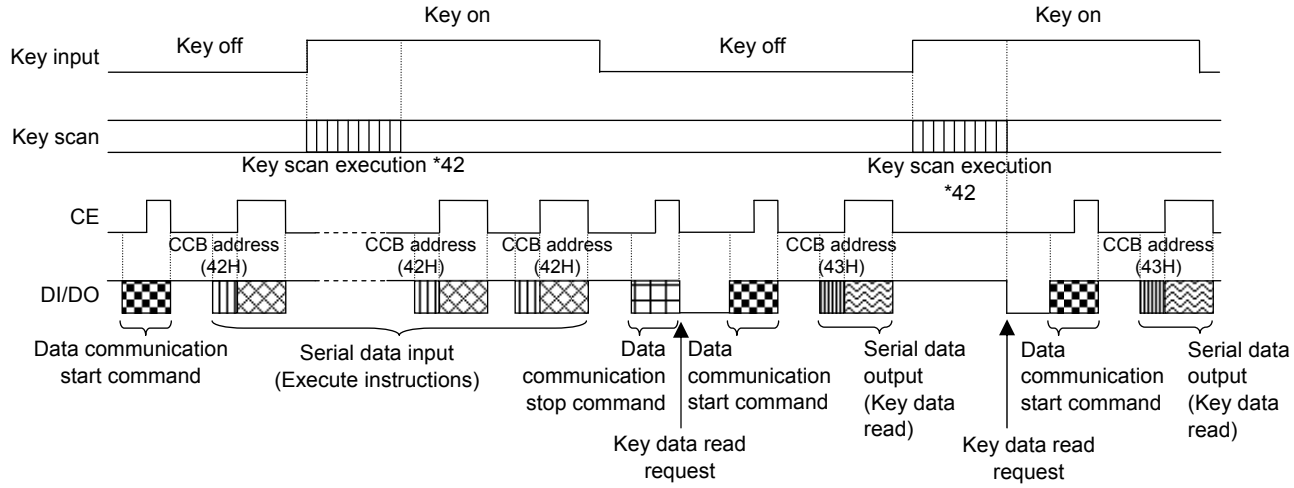
$T = \frac{1}{fosc}$ $T = \frac{1}{f_{CK}}$

2. Timing chart of 3 line type CCB format

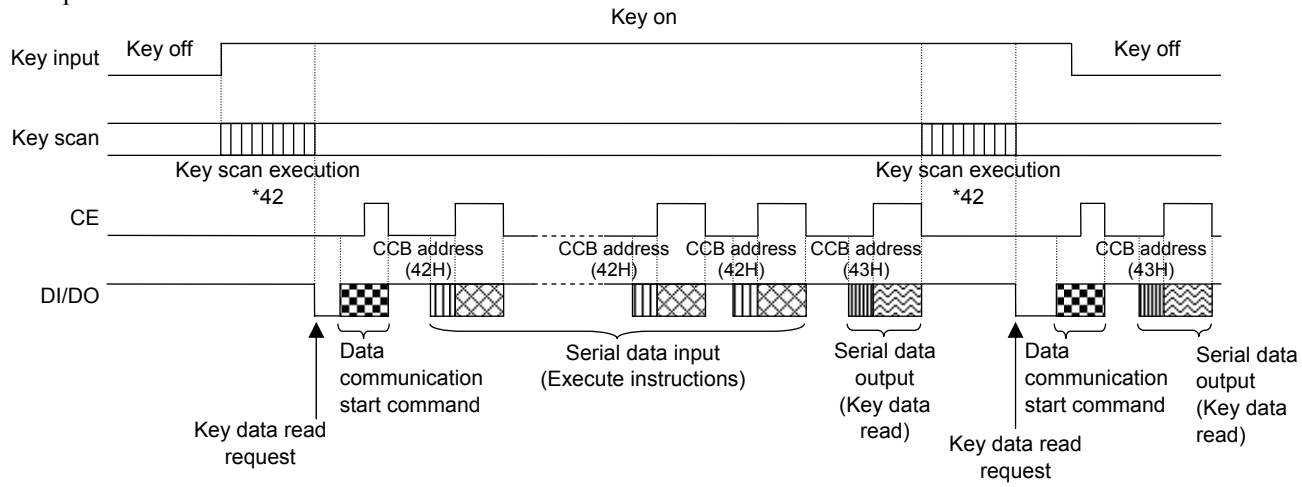
<Example 1>



<Example 2>



<Example 3>



Note: *42. When the key data agrees for two key scans, the key scan execution time is 4800T[s].
And, when the key data does not agree for two key scans and the key scan is executed again, the key scan execution time is 9600T[s].

$T = \frac{1}{fosc}$ $T = \frac{1}{f_{CK}}$

LC75812PT-8565 Character Font (Standard)

Lower 4BIT \ Upper 4BIT	MSB 0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000 LSB	CG RAM(1)	α		0	@	P	＼	p	á	â	＼	｡	タ	ミ	Á	Â
0001	(2)	β	!	1	A	Q	a	q	à	ä	。	ア	チ	ム	À	Ä
0010	(3)	±	”	2	B	R	b	r	é	ê	「	イ	ツ	メ	É	Ê
0011	(4)	÷	#	3	C	S	c	s	è	ë	」	ウ	テ	モ	È	Ë
0100	(5)	π	$	4	D	T	d	t	í	î	、	エ	ト	ヤ	Í	Î
0101	(6)	¿	%	5	E	U	e	u	ì	ï	・	オ	ナ	ユ	Ì	Ï
0110	(7)	Φ	&	6	F	V	f	v	ó	ô	ヲ	カ	ニ	ヨ	Ó	Ô
0111	(8)	ϕ	’	7	G	W	g	w	ò	ö	ァ	キ	ヌ	ラ	Ò	Ö
1000	(9)	Æ	(	8	H	X	h	x	ú	û	ィ	ク	ネ	リ	Ú	Û
1001	(10)	æ	)	9	I	Y	i	y	ù	ü	ゥ	ケ	ノ	ル	Ù	Ü
1010	(11)	Œ	*	:	J	Z	j	z	Ñ	ñ	ェ	コ	ハ	レ	Ã	ã
1011	(12)	œ	+	;	K	[	k	{	Ç	ç	ォ	サ	ヒ	ロ	Õ	õ
1100	(13)	→	,	<	L	¥	l	|	Ş	ş	ャ	シ	フ	ワ	Å	å
1101	(14)	←	−	=	M	]	m	}	Ğ	ğ	ュ	ス	ヘ	ン	a	o
1110	(15)	↑	.	>	N	^	n	—	İ	i	ョ	セ	ホ	゛	ń	ň
1111	(16)	↓	/	?	O	_	o	■	IJ	ij	ッ	ソ	マ	゜	ě	£

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC75812PT-8565-H	TQFP100 14x14 / TQFP100 (Pb-Free / Halogen Free)	90 / Tray JEDEC
LC75812PTH-8565-H	TQFP100 14x14 / TQFP100 (Pb-Free / Halogen Free)	450 / Tray JEDEC
LC75812PTS-8565-H	TQFP100 14x14 / TQFP100 (Pb-Free / Halogen Free)	450 / Tray JEDEC

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