LC75847T

1/3, 1/4-Duty General-Purpose LCD Driver

ON Semiconductor®

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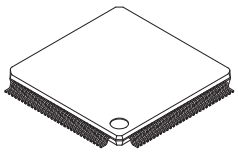


TQFP120 14x14 / TQFP120

Overview

The LC75847T is 1/3 duty and 1/4 duty general-purpose LCD driver that can be used for frequency display in electronic tuners under the control of a microcontroller. The LC75847T can drive an LCD with up to 420 segments directly. The LC75847T can also control up to 8 general-purpose output ports.

Features

- Switching between 1/3 duty and 1/4 duty drive techniques under serial data control.
- Switching between 1/2 bias and 1/3 bias drive techniques under serial data control.
- Up to 318 segments for 1/3 duty drive and 420 segments for 1/4 duty drive can be displayed.
- Serial data input supports CCB* format communication with the system controller.
- Serial data control of the power-saving mode based backup function and all the segments forced off function.
- Serial data control of switching between the segment output port and the general-purpose output port functions.
- Serial data control of frame frequency for common and segment output waveforms.
- High generality, since display data is displayed directly without decoder intervention.
- Built-in display contrast adjustment circuit
- Independent V_{LCD} for the LCD driver block
- The $\overline{INH}$ pin can force the display to the off state.
- RC oscillator circuit

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
	V_{LCD} max	V_{LCD}	–0.3 to +7.0	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	–0.3 to +7.0	V
	$V_{IN}2$	OSC	–0.3 to V_{DD} +0.3	
	$V_{IN}3$	$V_{LCD}1$, $V_{LCD}2$	–0.3 to V_{LCD} +0.3	
Output voltage	$V_{OUT}1$	OSC	–0.3 to V_{DD} +0.3	V
	$V_{OUT}2$	$V_{LCD}0$, S1 to S106, COM1 to COM4, P1 to P8	–0.3 to V_{LCD} +0.3	
Output current	$I_{OUT}1$	S1 to S106	300	μA
	$I_{OUT}2$	COM1 to COM4	3	mA
	$I_{OUT}3$	P1 to P8	5	mA
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 28 of this data sheet.

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		6.0	V
	V_{LCD}	V_{LCD}, $V_{LCD}0$ = 0.70 V_{LCD} to 0.95 V_{LCD}	4.0		6.0	
		V_{LCD}, $V_{LCD}0$ = V_{LCD}	2.7		6.0	
Output voltage	$V_{LCD}0$	$V_{LCD}0$	2.7		V_{LCD}	V
Input voltage	$V_{LCD}1$	$V_{LCD}1$		2/3 $V_{LCD}0$	$V_{LCD}0$	V
	$V_{LCD}2$	$V_{LCD}2$		1/3 $V_{LCD}0$	$V_{LCD}0$	
Input high level voltage	V_{IH}	CE, CL, DI, $\overline{INH}$	0.8 V_{DD}		6.0	V
Input low level voltage	V_{IL}	CE, CL, DI, $\overline{INH}$	0		0.2 V_{DD}	V
Recommended external resistance	R_{OSC}	OSC		39		kΩ
Recommended external capacitance	C_{OSC}	OSC		1000		pF
Guaranteed oscillation range	f_{OSC}	OSC	19	38	76	kHz
Data setup time	t_{ds}	CL, DI: Figure 2	160			ns
Data hold time	t_{dh}	CL, DI: Figure 2	160			ns
CE wait time	t_{cp}	CE, CL: Figure 2	160			ns
CE setup time	t_{cs}	CE, CL: Figure 2	160			ns
CE hold time	t_{ch}	CE, CL: Figure 2	160			ns
High level clock pulse width	$t_{øH}$	CL: Figure 2	160			ns
Low level clock pulse width	$t_{øL}$	CL: Figure 2	160			ns
Rise time	t_r	CE, CL, DI: Figure 2		160		ns
Fall time	t_f	CE, CL, DI: Figure 2		160		ns
$\overline{INH}$ switching time	t_c	$\overline{INH}$, CE: Figure 3, Figure 4	10			µs

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics for the allowable operating ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$		0.1 V_{DD}		V
Input high level current	I_{IH}	CE, CL, DI, $\overline{INH}$: V_I = 6.0 V			5.0	μA
Input low level current	I_{IL}	CE, CL, DI, $\overline{INH}$: V_I = 0 V	–5.0			μA
Output high level voltage	$V_{OH}1$	S1 to S106: I_O = –20 μA	$V_{LCD}0$ – 0.9			V
	$V_{OH}2$	COM1 to COM4: I_O = –100 μA	$V_{LCD}0$ – 0.9			
	$V_{OH}3$	P1 to P8: I_O = –1 mA	V_{LCD} – 0.9			
Output low level voltage	$V_{OL}1$	S1 to S106: I_O = 20 μA			0.9	V
	$V_{OL}2$	COM1 to COM4: I_O = 100 μA			0.9	
	$V_{OL}3$	P1 to P8: I_O = 1 mA			0.9	
Output middle level voltage*1	$V_{MID}1$	COM1 to COM4: 1/2 bias, I_O = ±100 μA	1/2 $V_{LCD}0$ – 0.9		1/2 $V_{LCD}0$ + 0.9	V
	$V_{MID}2$	S1 to S106: 1/3 bias, I_O = ±20 μA	2/3 $V_{LCD}0$ – 0.9		2/3 $V_{LCD}0$ + 0.9	
	$V_{MID}3$	S1 to S106: 1/3 bias, I_O = ±20 μA	1/3 $V_{LCD}0$ – 0.9		1/3 $V_{LCD}0$ + 0.9	
	$V_{MID}4$	COM1 to COM4: 1/3 bias, I_O = ±100 μA	2/3 $V_{LCD}0$ – 0.9		2/3 $V_{LCD}0$ + 0.9	
	$V_{MID}5$	COM1 to COM4: 1/3 bias, I_O = ±100 μA	1/3 $V_{LCD}0$ – 0.9		1/3 $V_{LCD}0$ + 0.9	
Oscillator frequency	f_{OSC}	OSC: R_{OSC} = 39 kΩ, C_{OSC} = 1000 pF	30.4	38	45.6	kHz
Current drain	$I_{DD}1$	V_{DD}: Power-saving mode			5	μA
	$I_{DD}2$	V_{DD}: V_{DD} = 6.0 V, output open, f_{OSC} = 38 kHz		250	500	
	$I_{LCD}1$	V_{LCD}: Power-saving mode			5	
	$I_{LCD}2$	V_{LCD}: V_{LCD} = 6.0 V, output open, 1/2 bias, f_{OSC} = 38 kHz, $V_{LCD}0$ = 0.70 V_{LCD} to 0.95 V_{LCD}		400	800	
	$I_{LCD}3$	V_{LCD}: V_{LCD} = 6.0 V, output open, 1/2 bias, f_{OSC} = 38 kHz, $V_{LCD}0$ = V_{LCD}		350	700	
	$I_{LCD}4$	V_{LCD}: V_{LCD} = 6.0 V, output open, 1/3 bias, f_{OSC} = 38 kHz, $V_{LCD}0$ = 0.70 V_{LCD} to 0.95 V_{LCD}		300	600	
	$I_{LCD}5$	V_{LCD}: V_{LCD} = 6.0 V, output open, 1/3 bias, f_{OSC} = 38 kHz, $V_{LCD}0$ = V_{LCD}		250	500	

Note: *1 Excluding the bias voltage generation divider resistors built in the $V_{LCD}0$, $V_{LCD}1$, $V_{LCD}2$, and V_{SS}. (See Figure 1.)

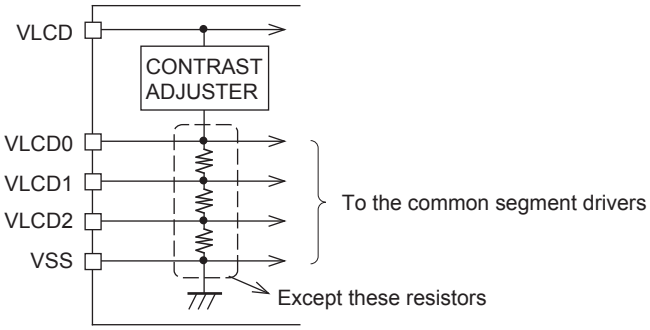
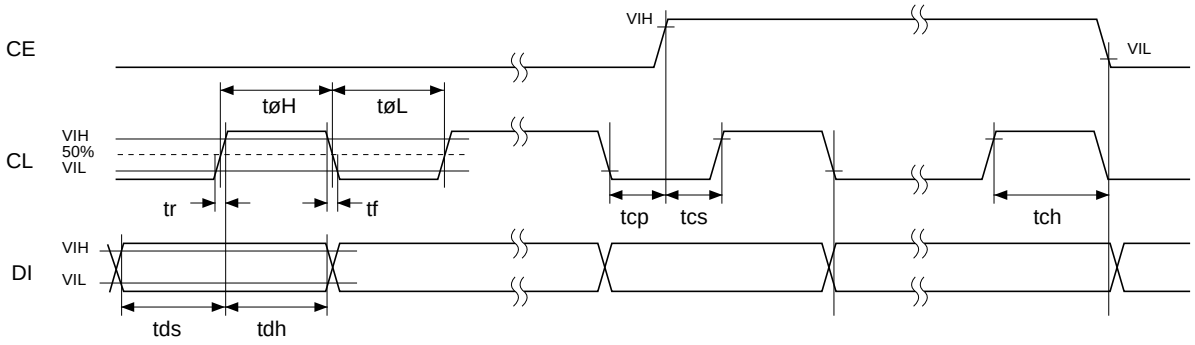


Figure 1

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. When CL is stopped at the low level



2. When CL is stopped at the high level

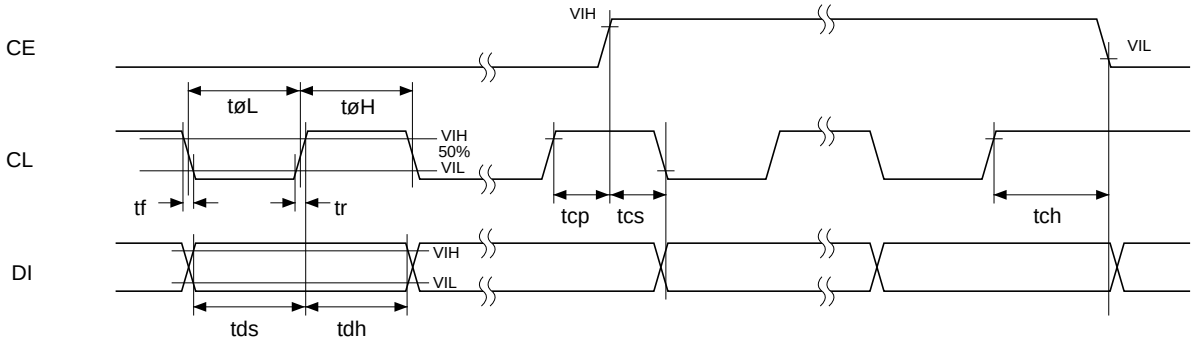
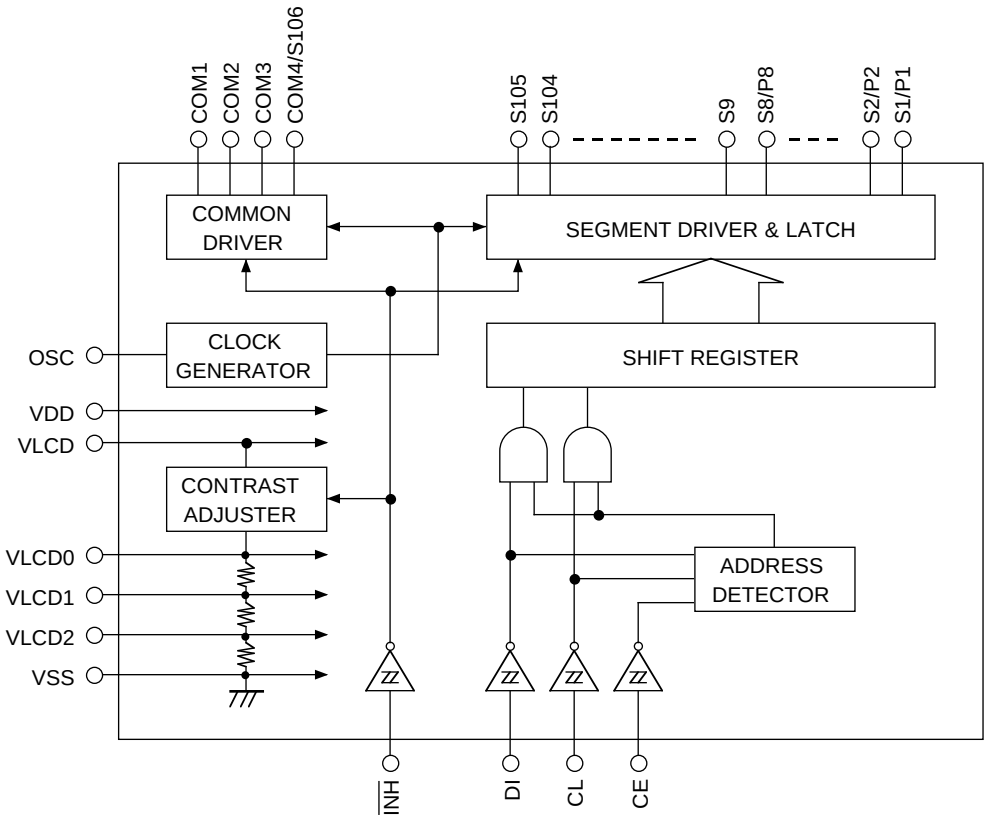


Figure 2

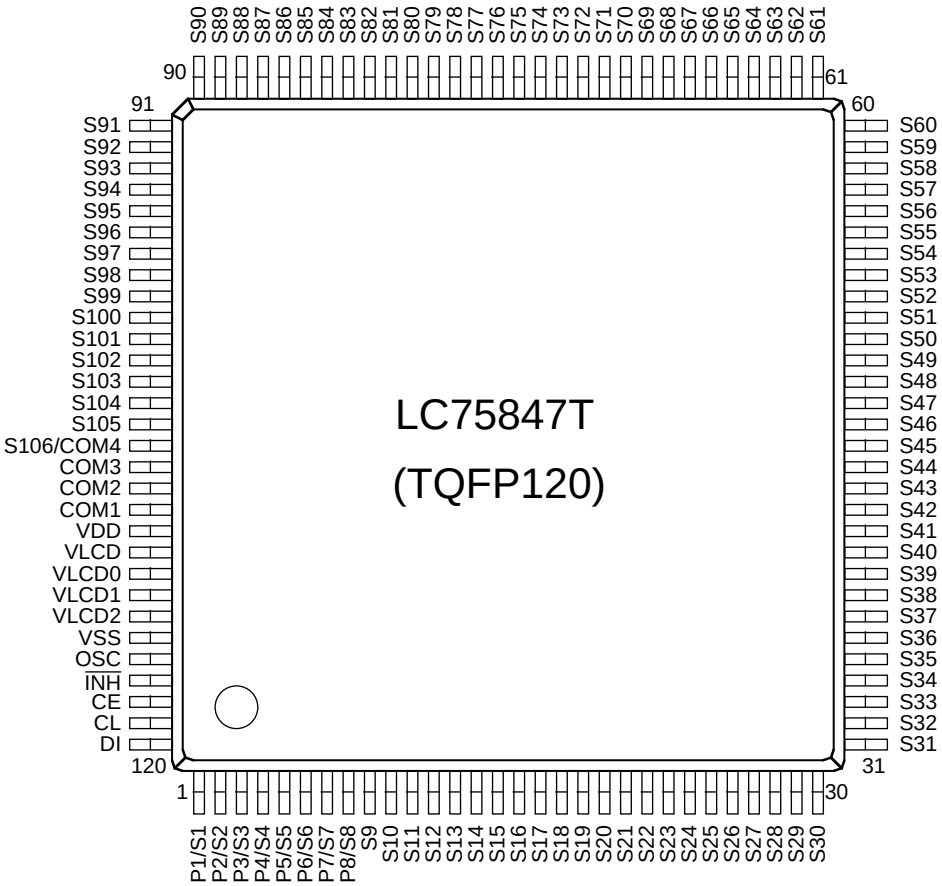
Block Diagram



Pin Functions

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1 to S8/P8 S9 to S105	1 to 8 9 to 105	Segment outputs for displaying the display data transferred by serial data input. The pins S1/P1 to S8/P8 can be used as general-purpose output ports when so set up by the control data.	—	O	Open
COM1 to COM3 COM4/S106	109 to 107 106	Common driver outputs. The frame frequency is f_O Hz. The COM4/S106 pin can be used as a segment output in 1/3 duty.	—	O	Open
OSC	116	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor to this pin.	—	I/O	V_{DD}
CE CL DI	118 119 120	Serial data transfer inputs. These pins are connected to the control microprocessor. CE: Chip enable CL: Synchronization clock DI: Transfer data	H ↑ —	I I I	GND
$\overline{INH}$	117	Display off control input • $\overline{INH}$ = low (V_{SS}) ....Off S1/P1 to S8/P8 = low (V_{SS}) (These pins are forcibly set to the segment output port function and fixed at the V_{SS} level.) S9 to S105 = low (V_{SS}) COM1 to COM3 = low (V_{SS}) COM4/S106 = low (V_{SS}) • $\overline{INH}$ = high (V_{DD}) ..On Note that serial data transfers can be performed when the display is forced off by this pin.	L	I	GND
$V_{LCD}0$	112	LCD drive 3/3 bias voltage (high level) supply. This level can be modified using the display contrast adjustment circuit. However, note that $V_{LCD}0$ must be greater than or equal to 2.7 V. Also, since this IC provides the built-in display contrast adjustment circuit, applications must not attempt to provide this level from external circuits.	—	O	Open
$V_{LCD}1$	113	LCD drive 2/3 bias voltage (middle level) supply. It is possible to supply the 2/3 $V_{LCD}0$ voltage to this pin externally. This pin must be shorted to $V_{LCD}2$ if 1/2 bias is used.	—	I	Open
$V_{LCD}2$	114	LCD drive 1/3 bias voltage (middle level) supply. It is possible to supply the 1/3 $V_{LCD}0$ voltage to this pin externally. This pin must be shorted to $V_{LCD}1$ if 1/2 bias is used.	—	I	Open
V_{DD}	110	Logic block power supply. Provide a voltage in the range 2.7 to 6.0 V.	—	—	—
V_{LCD}	111	LCD driver block power supply. When $V_{LCD}0$ is between 0.70 V_{LCD} and 0.95 V_{LCD}, supply a voltage in the range 4.0 to 6.0 V. When $V_{LCD}0$ and V_{LCD} will be equal, supply a voltage in the range 2.7 to 6.0 V.	—	—	—
V_{SS}	115	Ground pin. Connect to ground.	—	—	—

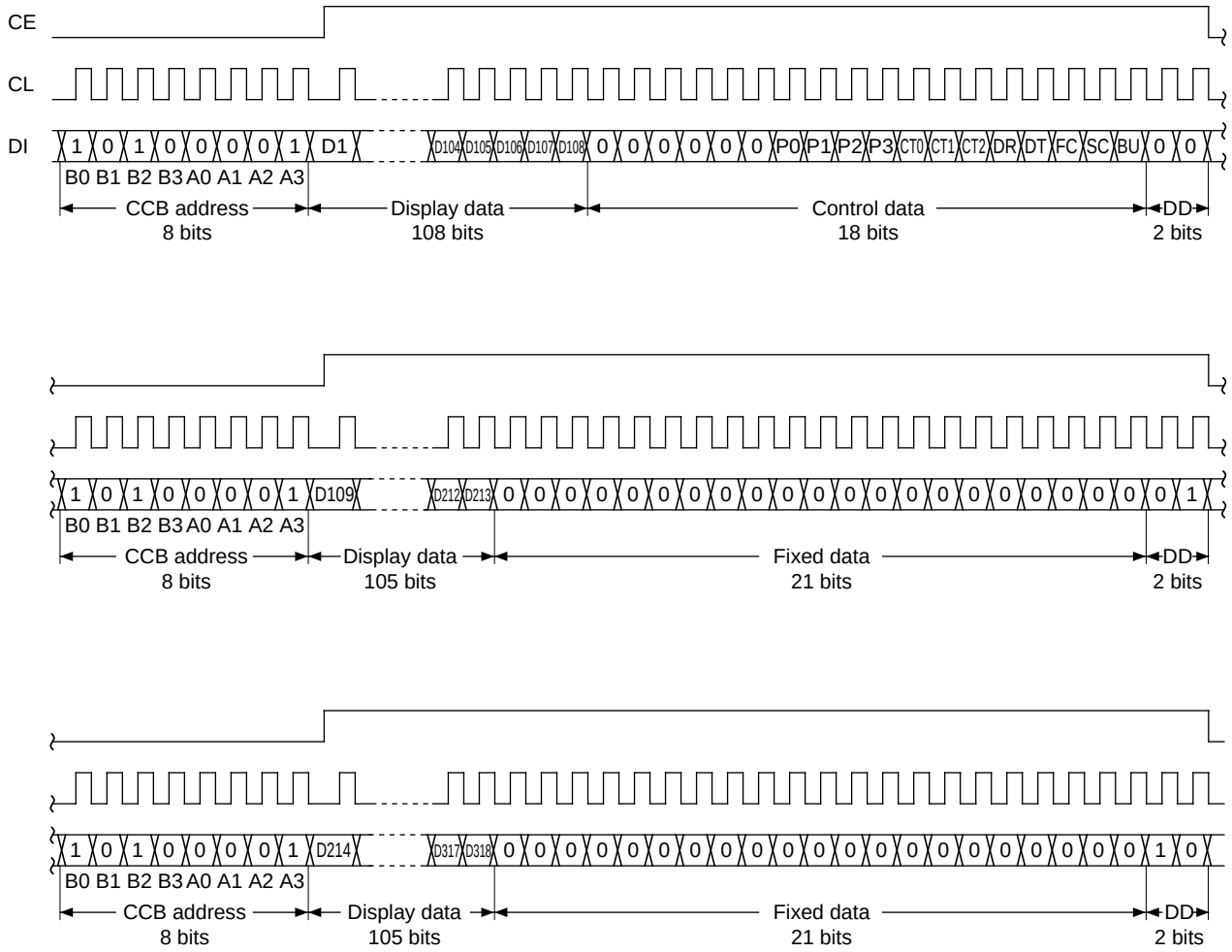
Pin Assignment



Serial Data Transfer Format

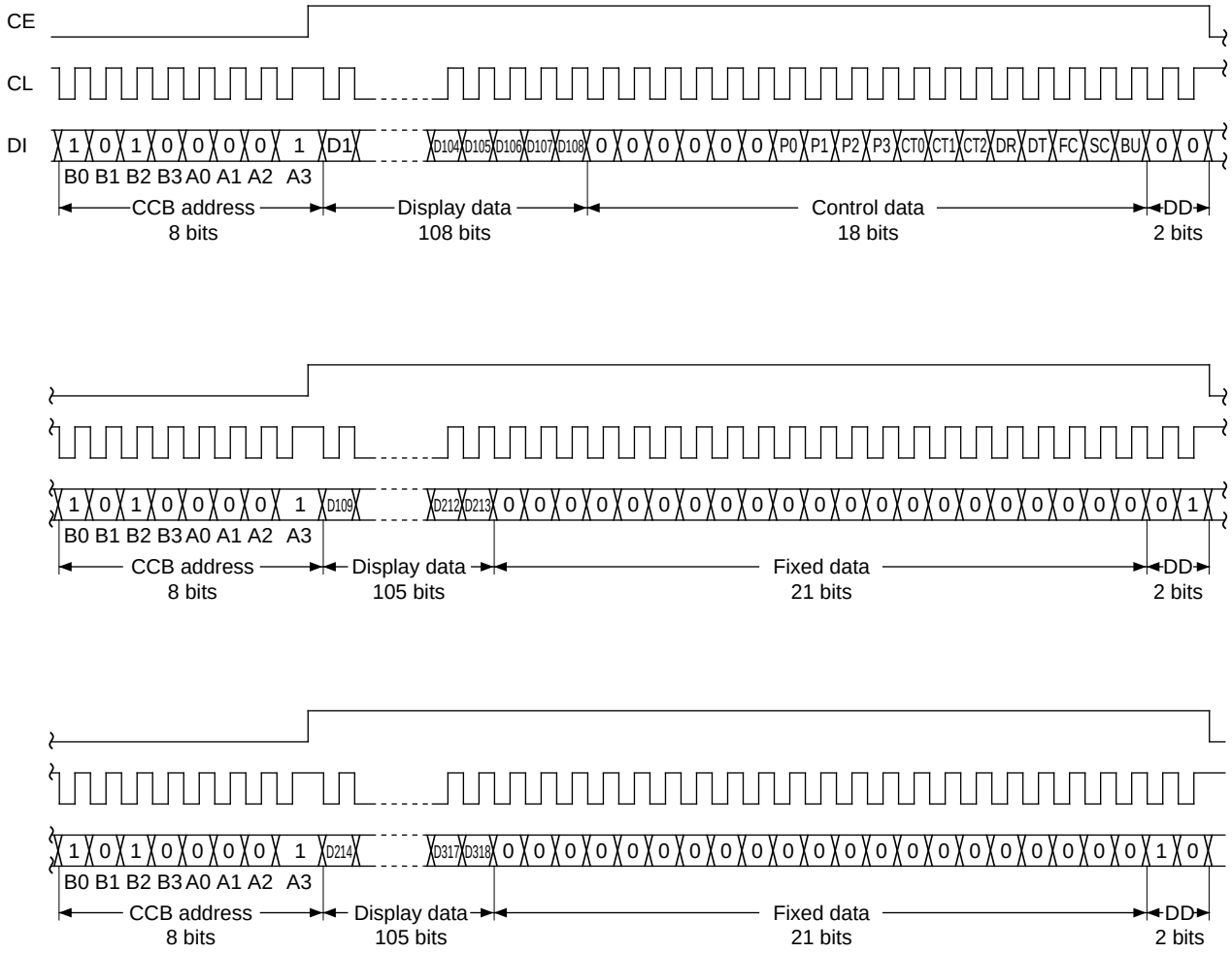
1. 1/3 duty

① When CL is stopped at the low level



Note: DD···Direction data.

② When CL is stopped at the high level

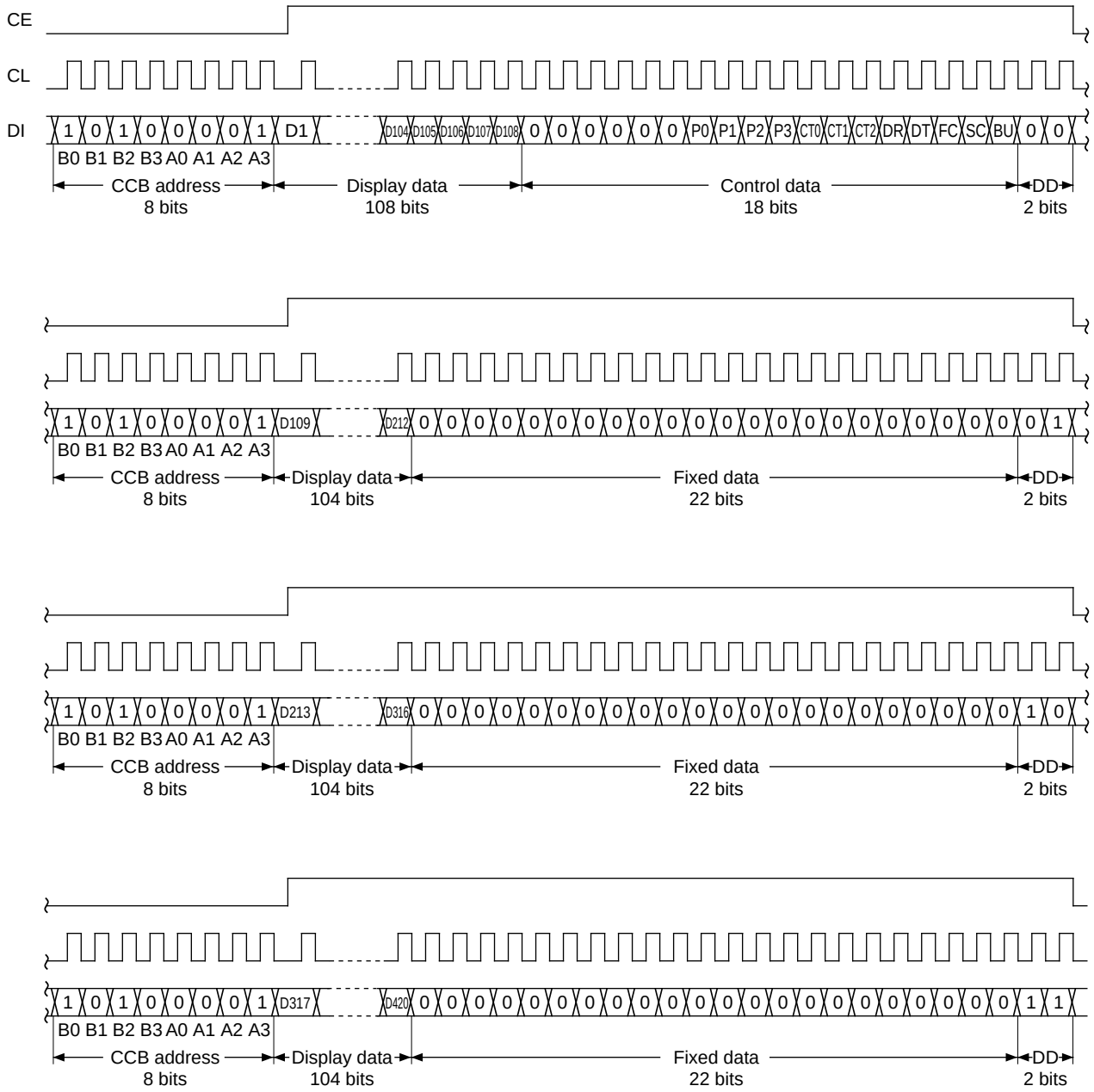


Note: DD···Direction data.

- CCB address.....85H
- D1 to D318.....Display data
- P0 to P3 .....Segment output port/general-purpose output port switching control data
- CT0 to CT2 .....Control data that sets the display contrast
- DR .....1/2 bias drive or 1/3 bias drive switching control data
- DT .....1/3 duty drive or 1/4 duty drive switching control data
- FC.....Common and segment output waveforms frame frequency setting control data
- SC.....Segments on/off control data
- BU .....Normal mode/power-saving mode control data

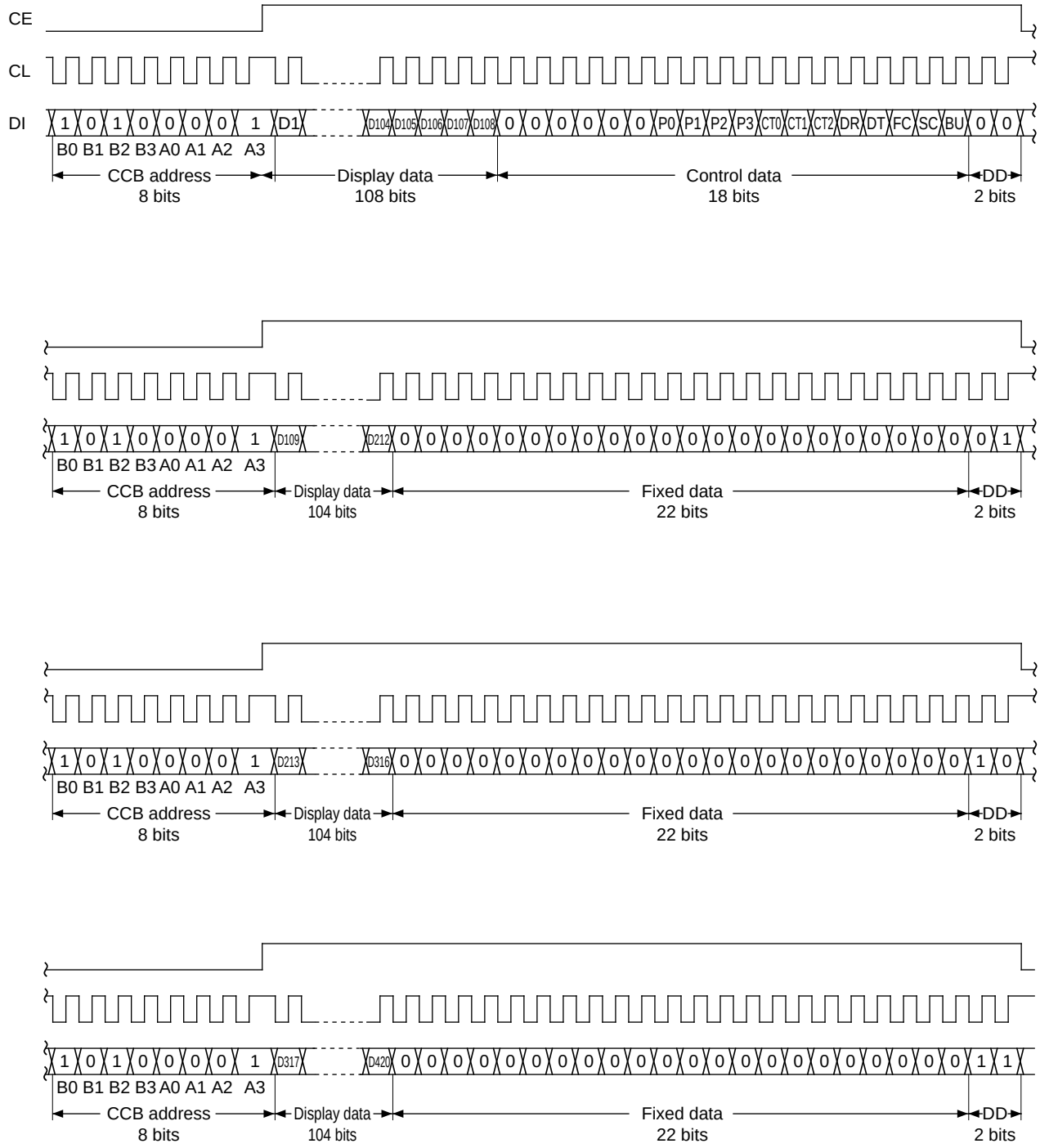
2. 1/4 duty

① When CL is stopped at the low level



Note: DD···Direction data.

② When CL is stopped at the high level



Note: DD···Direction data.

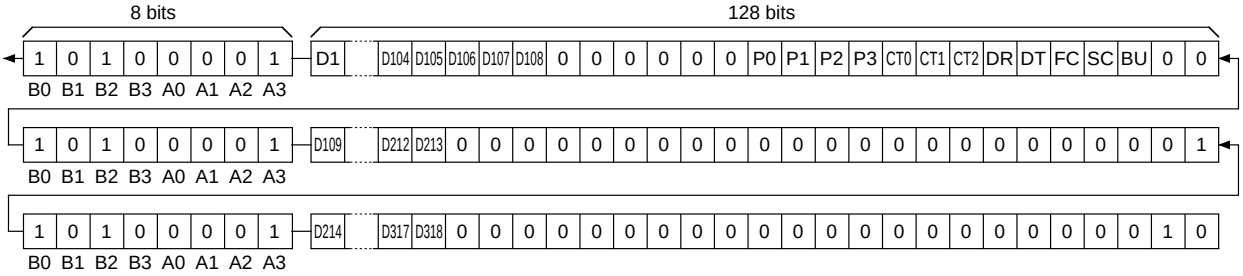
- CCB address.....85H
- D1 to D420.....Display data
- P0 to P3.....Segment output port/general-purpose output port switching control data
- CT0 to CT2 .....Control data that sets the display contrast
- DR.....1/2 bias drive or 1/3 bias drive switching control data
- DT .....1/3 duty drive or 1/4 duty drive switching control data
- FC.....Common and segment output waveforms frame frequency setting control data
- SC.....Segments on/off control data
- BU .....Normal mode/power-saving mode control data

Serial Data Transfer Example

1. 1/3 duty

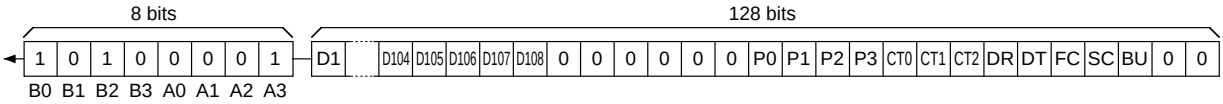
① When 214 or more segments are used

All 384 bits of serial data must be sent.



② When fewer than 214 segments are used

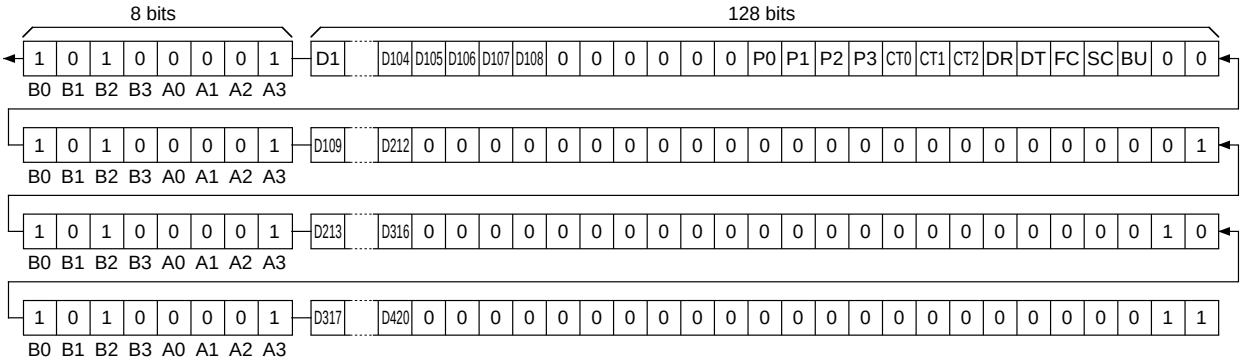
Either 128 or 256 bits of serial data may be sent, depending on the number of segments used. However, the serial data shown below (the D1 to D108 display data and the control data) must be sent.



2. 1/4 duty

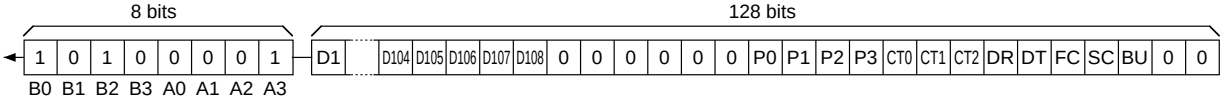
① When 317 or more segments are used

All 512 bits of serial data must be sent.



② When fewer than 317 segments are used

Either 128, 256 or 384 bits of serial data may be sent, depending on the number of segments used. However, the serial data shown below (the D1 to D108 display data and the control data) must be sent.



Control Data Functions

1. P0 to P3: Segment output port/general-purpose output port switching control data.
   These control data bits switch the S1/P1 to S8/P8 output pins between their segment output port and general-purpose output port functions.

Control data				Output pin state							
P0	P1	P2	P3	S1/P1	S2/P2	S3/P3	S4/P4	S5/P5	S6/P6	S7/P7	S8/P8
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0	1	P1	S2	S3	S4	S5	S6	S7	S8
0	0	1	0	P1	P2	S3	S4	S5	S6	S7	S8
0	0	1	1	P1	P2	P3	S4	S5	S6	S7	S8
0	1	0	0	P1	P2	P3	P4	S5	S6	S7	S8
0	1	0	1	P1	P2	P3	P4	P5	S6	S7	S8
0	1	1	0	P1	P2	P3	P4	P5	P6	S7	S8
0	1	1	1	P1	P2	P3	P4	P5	P6	P7	S8
1	0	0	0	P1	P2	P3	P4	P5	P6	P7	P8

Note: Sn (n = 1 to 8): Segment output ports
Pn (n = 1 to 8): General-purpose output ports

Also note that when the general-purpose output port function is selected, the output pins and the display data will have the correspondences listed in the tables below.

Output pin	Corresponding display data	
	1/3 duty	1/4 duty
S1/P1	D1	D1
S2/P2	D4	D5
S3/P3	D7	D9
S4/P4	D10	D13
S5/P5	D13	D17
S6/P6	D16	D21
S7/P7	D19	D25
S8/P8	D22	D29

For example, when 1/4 duty drive scheme is used, if the general-purpose output port function is selected for the S4/P4 output pin, that output pin will output a high level (V_{LCD}) when the display data D13 is 1, and a low level (V_{SS}) when the D13 is 0.

2. CT0 to CT2: Control data that sets the display contrast
   This control data is used to set the display contrast.
   CT0 to CT2: Display contrast setting (7 steps)

CT0	CT1	CT2	LCD drive 3/3 bias voltage power supply ($V_{LCD}0$) level
0	0	0	1.00 V_{LCD} = V_{LCD} – (0.05 V_{LCD} × 0)
1	0	0	0.95 V_{LCD} = V_{LCD} – (0.05 V_{LCD} × 1)
0	1	0	0.90 V_{LCD} = V_{LCD} – (0.05 V_{LCD} × 2)
1	1	0	0.85 V_{LCD} = V_{LCD} – (0.05 V_{LCD} × 3)
0	0	1	0.80 V_{LCD} = V_{LCD} – (0.05 V_{LCD} × 4)
1	0	1	0.75 V_{LCD} = V_{LCD} – (0.05 V_{LCD} × 5)
0	1	1	0.70 V_{LCD} = V_{LCD} – (0.05 V_{LCD} × 6)

Note that although the display contrast can be adjusted by operating the built-in display contrast adjustment circuit, it is also possible to adjust the contrast by varying the voltage level on the LCD drive block power supply V_{LCD} pin. However, $V_{LCD}0$ must always be greater than or equal to 2.7 V.

3. DR: 1/2 bias drive or 1/3 bias drive switching control data
   This control data bit selects either 1/2 bias drive or 1/3 bias drive.

DR	Bias drive scheme
0	1/3 bias drive
1	1/2 bias drive

4. DT: 1/3 duty drive or 1/4 duty drive switching control data
   This control data bit selects either 1/3 duty drive or 1/4 duty drive.

DT	Duty drive scheme	Output pin state (COM4/S106)
0	1/4 duty drive	COM4
1	1/3 duty drive	S106

Note: COM4: Common output
S106: Segment output

5. FC: Common and segment output waveforms frame frequency setting control data
   This control data bit sets the frame frequency for common and segment output waveforms.

FC	Frame frequency f_0 [Hz]
0	$\frac{fosc}{384}$
1	$\frac{fosc}{192}$

6. SC: Segments on/off control data
   This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

7. BU: Normal mode/power-saving mode control data
   This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power saving mode (The OSC pin oscillator is stopped, and the common and segment output pins go to the V_{SS} level. However, the S1/P1 to S8/P8 output pins that are set to be general-purpose output ports by the control data P0 to P3 can be used as general-purpose output ports.)

Display Data to Segment Output Pin Correspondence

1. 1/3 duty

Segment Output pin	COM1	COM2	COM3
S1/P1	D1	D2	D3
S2/P2	D4	D5	D6
S3/P3	D7	D8	D9
S4/P4	D10	D11	D12
S5/P5	D13	D14	D15
S6/P6	D16	D17	D18
S7/P7	D19	D20	D21
S8/P8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D86	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105
S36	D106	D107	D108

Segment Output pin	COM1	COM2	COM3
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
S51	D151	D152	D153
S52	D154	D155	D156
S53	D157	D158	D159
S54	D160	D161	D162
S55	D163	D164	D165
S56	D166	D167	D168
S57	D169	D170	D171
S58	D172	D173	D174
S59	D175	D176	D177
S60	D178	D179	D180
S61	D181	D182	D183
S62	D184	D185	D186
S63	D187	D188	D189
S64	D190	D191	D192
S65	D193	D194	D195
S66	D196	D197	D198
S67	D199	D200	D201
S68	D202	D203	D204
S69	D205	D206	D207
S70	D208	D209	D210
S71	D211	D212	D213
S72	D214	D215	D216

Segment Output pin	COM1	COM2	COM3
S73	D217	D218	D219
S74	D220	D221	D222
S75	D223	D224	D225
S76	D226	D227	D228
S77	D229	D230	D231
S78	D232	D233	D234
S79	D235	D236	D237
S80	D238	D239	D240
S81	D241	D242	D243
S82	D244	D245	D246
S83	D247	D248	D249
S84	D250	D251	D252
S85	D253	D254	D255
S86	D256	D257	D258
S87	D259	D260	D261
S88	D262	D263	D264
S89	D265	D266	D267
S90	D268	D269	D270
S91	D271	D272	D273
S92	D274	D275	D276
S93	D277	D278	D279
S94	D280	D281	D282
S95	D283	D284	D285
S96	D286	D287	D288
S97	D289	D290	D291
S98	D292	D293	D294
S99	D295	D296	D297
S100	D298	D299	D300
S101	D301	D302	D303
S102	D304	D305	D306
S103	D307	D308	D309
S104	D310	D311	D312
S105	D313	D314	D315
COM4/S106	D316	D317	D318

Note: This applies to the case where the S1/P1 to S8/P8, and COM4/S106 output pins are set to be segment output ports.

For example, the table below lists the segment output states for the S11 output pin.

Display data			Segment output pin (S11) state
D31	D32	D33	
0	0	0	The LCD segments corresponding to COM1, COM2, and COM3 are off.
0	0	1	The LCD segment corresponding to COM3 is on.
0	1	0	The LCD segment corresponding to COM2 is on.
0	1	1	The LCD segments corresponding to COM2 and COM3 are on.
1	0	0	The LCD segment corresponding to COM1 is on.
1	0	1	The LCD segments corresponding to COM1 and COM3 are on.
1	1	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	1	The LCD segments corresponding to COM1, COM2, and COM3 are on.

2. 1/4 duty

Segment Output pin	COM1	COM2	COM3	COM4
S1/P1	D1	D2	D3	D4
S2/P2	D5	D6	D7	D8
S3/P3	D9	D10	D11	D12
S4/P4	D13	D14	D15	D16
S5/P5	D17	D18	D19	D20
S6/P6	D21	D22	D23	D24
S7/P7	D25	D26	D27	D28
S8/P8	D29	D30	D31	D32
S9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200
S51	D201	D202	D203	D204
S52	D205	D206	D207	D208
S53	D209	D210	D211	D212

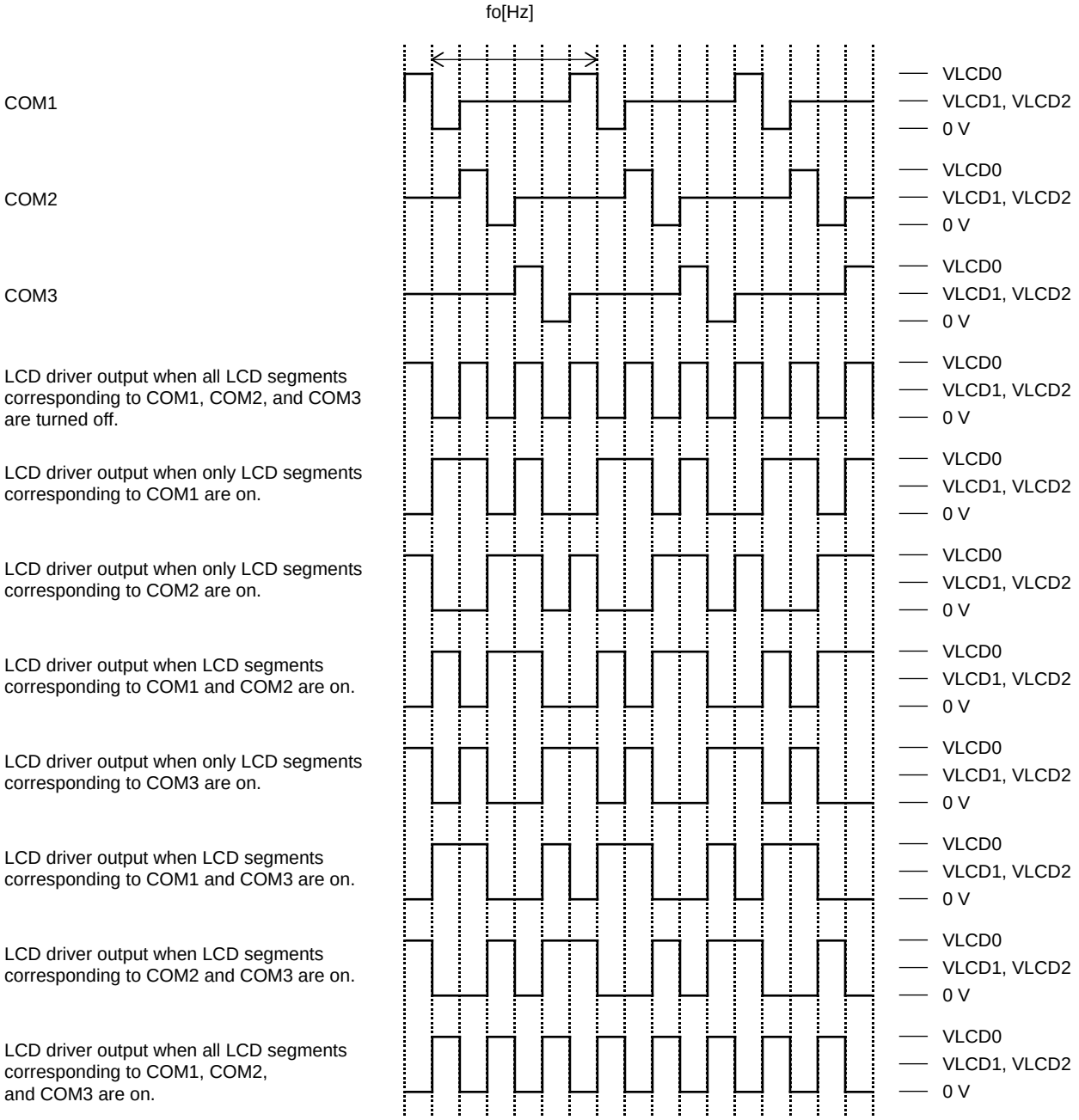
Segment Output pin	COM1	COM2	COM3	COM4
S54	D213	D214	D215	D216
S55	D217	D218	D219	D220
S56	D221	D222	D223	D224
S57	D225	D226	D227	D228
S58	D229	D230	D231	D232
S59	D233	D234	D235	D236
S60	D237	D238	D239	D240
S61	D241	D242	D243	D244
S62	D245	D246	D247	D248
S63	D249	D250	D251	D252
S64	D253	D254	D255	D256
S65	D257	D258	D259	D260
S66	D261	D262	D263	D264
S67	D265	D266	S267	D268
S68	D269	D270	D271	D272
S69	D273	D274	D275	D276
S70	D277	D278	D279	D280
S71	D281	D282	D283	D284
S72	D285	D286	D287	D288
S73	D289	D290	D291	D292
S74	D293	D294	D295	D296
S75	D297	D298	D299	D300
S76	D301	D302	D303	D304
S77	D305	D306	D307	D308
S78	D309	D310	D311	D312
S79	D313	D314	D315	D316
S80	D317	D318	D319	D320
S81	D321	D322	D323	D324
S82	D325	D326	D327	D328
S83	D329	D330	D331	D332
S84	D333	D334	D335	D336
S85	D337	D338	D339	D340
S86	D341	D342	D343	D344
S87	D345	D346	D347	D348
S88	D349	D350	D351	D352
S89	D353	D354	D355	D356
S90	D357	D358	D359	D360
S91	D361	D362	D363	D364
S92	D365	D366	D367	D368
S93	D369	D370	D371	D372
S94	D373	D374	D375	D376
S95	D377	D378	D379	D380
S96	D381	D382	D383	D384
S97	D385	D386	D387	D388
S98	D389	D390	D391	D392
S99	D393	D394	D395	D396
S100	D397	D398	D399	D400
S101	D401	D402	D403	D404
S102	D405	D406	D407	D408
S103	D409	D410	D411	D412
S104	D413	D414	D415	D416
S105	D417	D418	D419	D420

Note: This applies to the case where the S1/P1 to S8/P8 output pins are set to be segment output ports.

For example, the table below lists the segment output states for the S11 output pin.

Display data				Segment output pin (S11) state
D41	D42	D43	D44	
0	0	0	0	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off.
0	0	0	1	The LCD segment corresponding to COM4 is on.
0	0	1	0	The LCD segment corresponding to COM3 is on.
0	0	1	1	The LCD segments corresponding to COM3 and COM4 are on.
0	1	0	0	The LCD segment corresponding to COM2 is on.
0	1	0	1	The LCD segments corresponding to COM2 and COM4 are on.
0	1	1	0	The LCD segments corresponding to COM2 and COM3 are on.
0	1	1	1	The LCD segments corresponding to COM2, COM3, and COM4 are on.
1	0	0	0	The LCD segment corresponding to COM1 is on.
1	0	0	1	The LCD segments corresponding to COM1 and COM4 are on.
1	0	1	0	The LCD segments corresponding to COM1 and COM3 are on.
1	0	1	1	The LCD segments corresponding to COM1, COM3, and COM4 are on.
1	1	0	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	0	1	The LCD segments corresponding to COM1, COM2, and COM4 are on.
1	1	1	0	The LCD segments corresponding to COM1, COM2, and COM3 are on.
1	1	1	1	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.

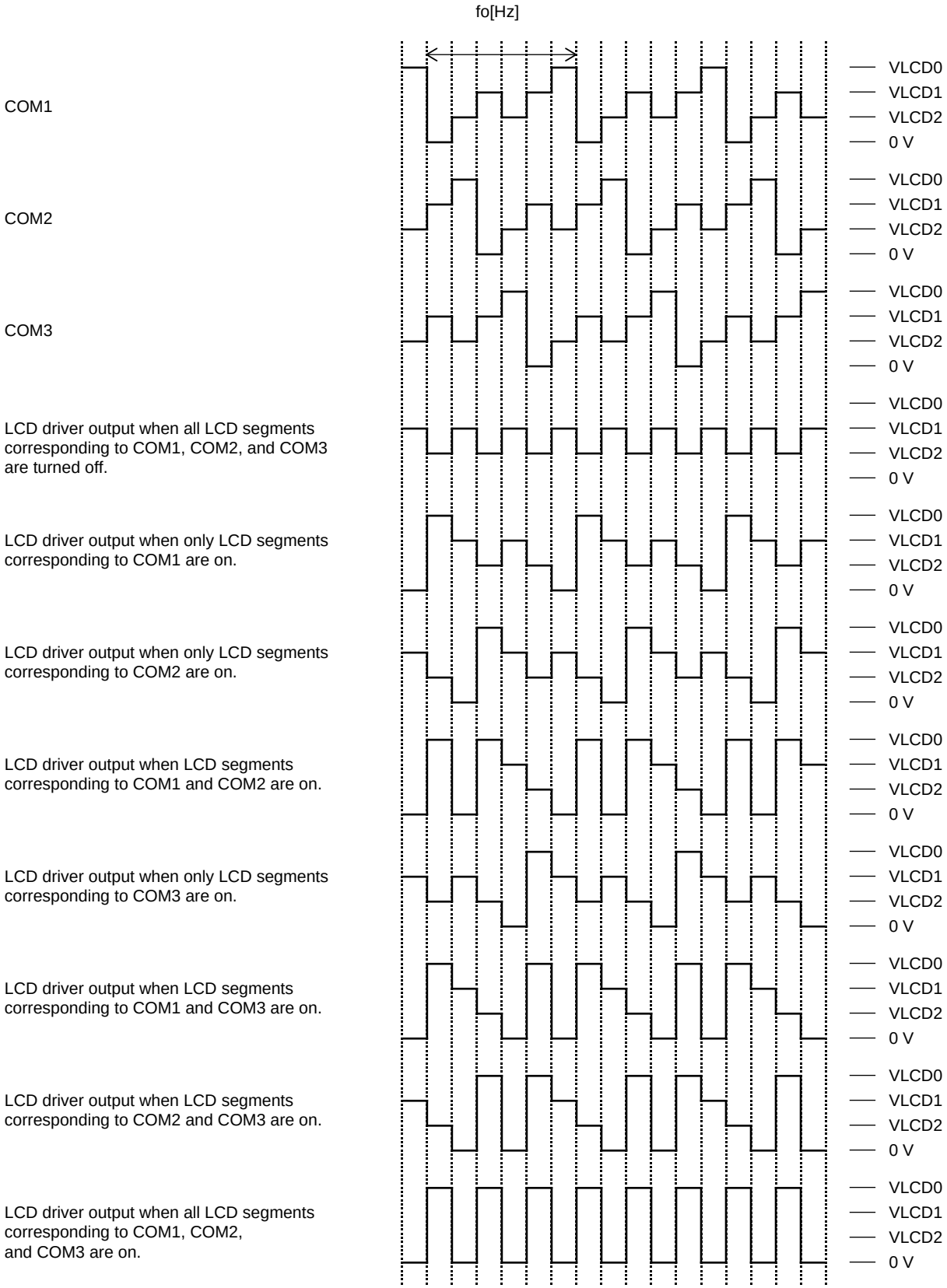
1/3 Duty, 1/2 Bias Drive Technique



When the control data FC = 0 : $f_0 = \frac{fosc}{384}$

When the control data FC = 1 : $f_0 = \frac{fosc}{192}$

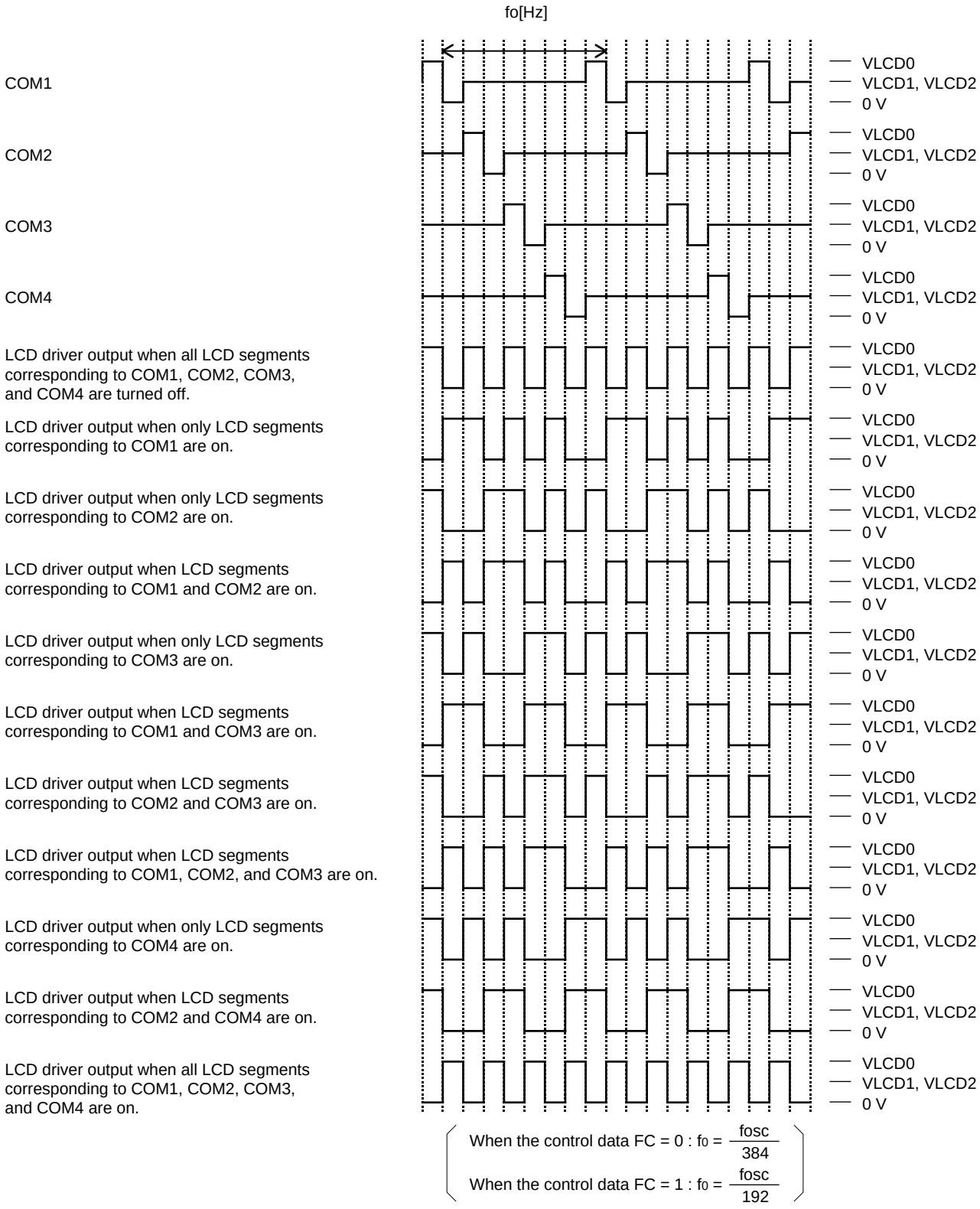
1/3 Duty, 1/3 Bias Drive Technique



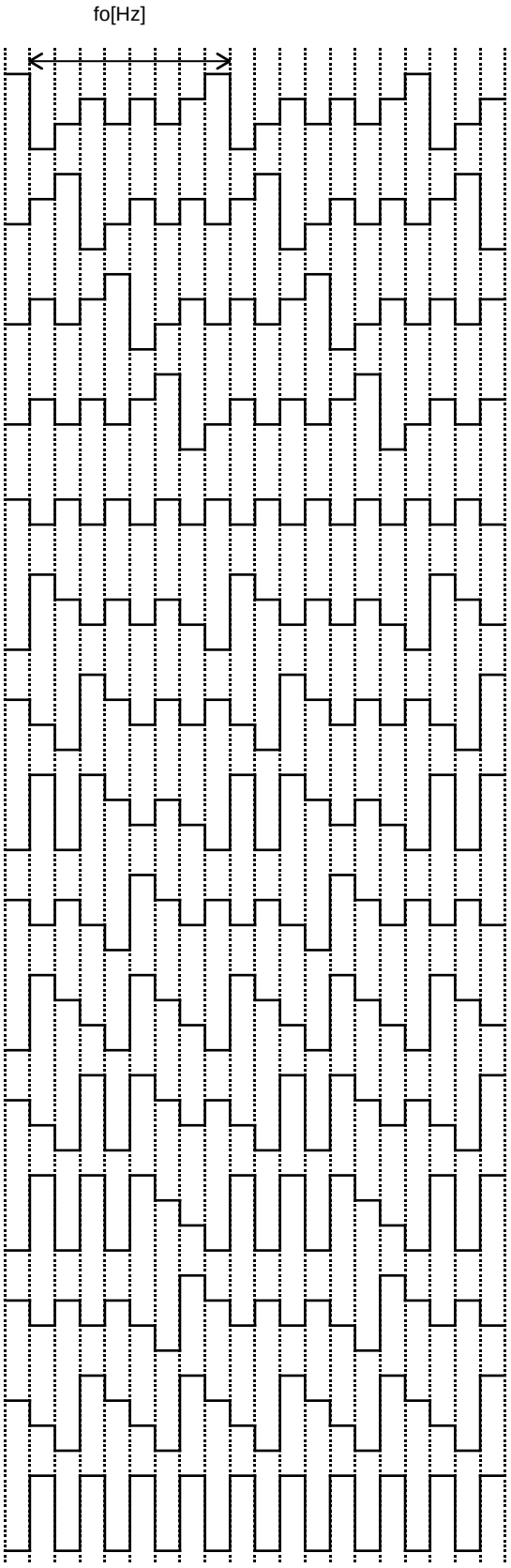
When the control data FC = 0 : $f_0 = \frac{fosc}{384}$

When the control data FC = 1 : $f_0 = \frac{fosc}{192}$

1/4 Duty, 1/2 Bias Drive Technique



1/4 Duty, 1/3 Bias Drive Technique



COM1

COM2

COM3

COM4

LCD driver output when all LCD segments corresponding to COM1, COM2, COM3, and COM4 are turned off.

LCD driver output when only LCD segments corresponding to COM1 are on.

LCD driver output when only LCD segments corresponding to COM2 are on.

LCD driver output when LCD segments corresponding to COM1 and COM2 are on.

LCD driver output when only LCD segments corresponding to COM3 are on.

LCD driver output when LCD segments corresponding to COM1 and COM3 are on.

LCD driver output when LCD segments corresponding to COM2 and COM3 are on.

LCD driver output when LCD segments corresponding to COM1, COM2, and COM3 are on.

LCD driver output when only LCD segments corresponding to COM4 are on.

LCD driver output when LCD segments corresponding to COM2 and COM4 are on.

LCD driver output when all LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.

When the control data FC = 0 : $f_0 = \frac{fosc}{384}$

When the control data FC = 1 : $f_0 = \frac{fosc}{192}$

The $\overline{INH}$ pin and Display Control

Since the IC internal data (1/3 duty: the display data D1 to D318 and the control data, 1/4 duty: the display data D1 to D420 and the control data) is undefined when power is first applied, applications should set the $\overline{INH}$ pin low at the same time as power is applied to turn off the display (This sets the S1/P1 to S8/P8, S9 to S105, COM1 to COM3, and COM4/S106 to the V_{SS} level.) and during this period send serial data from the controller. The controller should then set the $\overline{INH}$ pin high after the data transfer has completed. This procedure prevents meaningless displays at power on. (See Figures 3 and 4.)

Notes on the Power On/Off Sequences

Applications should observe the following sequences when turning the LC75847T power on and off.

- At power on: Logic block power supply (V_{DD}) on → LCD driver block power supply (V_{LCD}) on
- At power off: LCD driver block power supply (V_{LCD}) off → Logic block power supply (V_{DD}) off

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.

- 1/3 duty

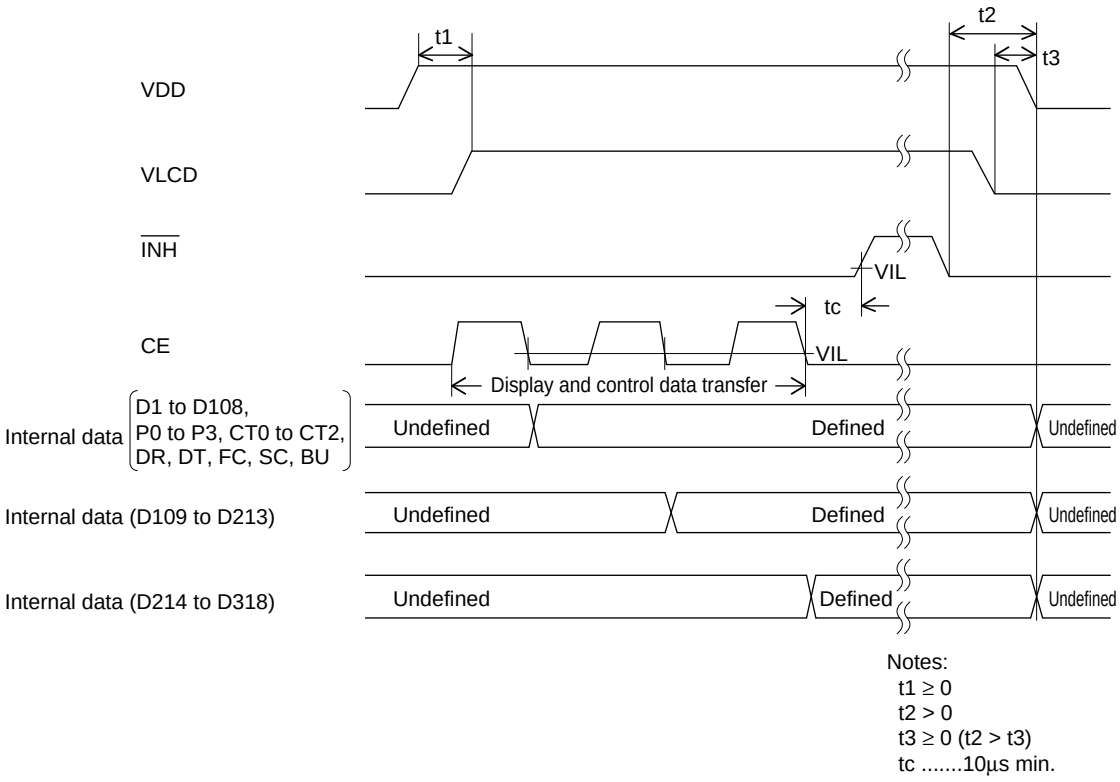


Figure 3

• 1/4 duty

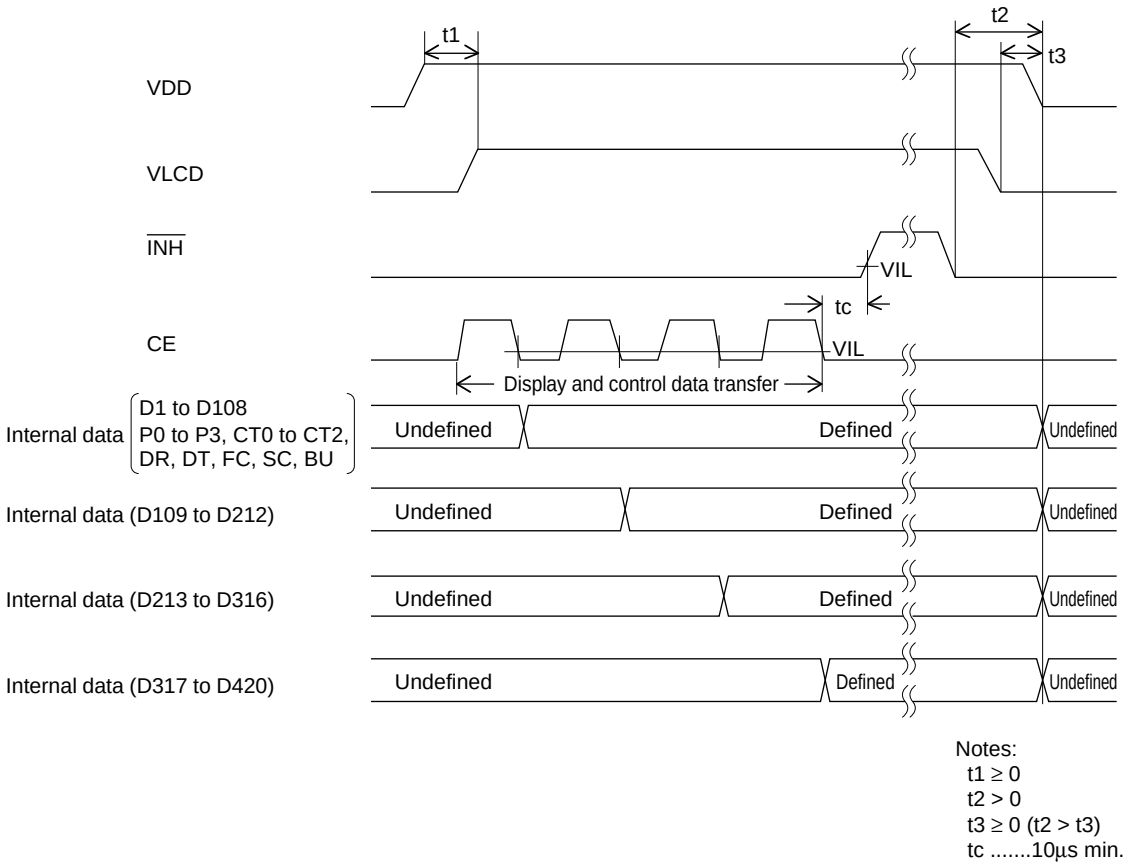


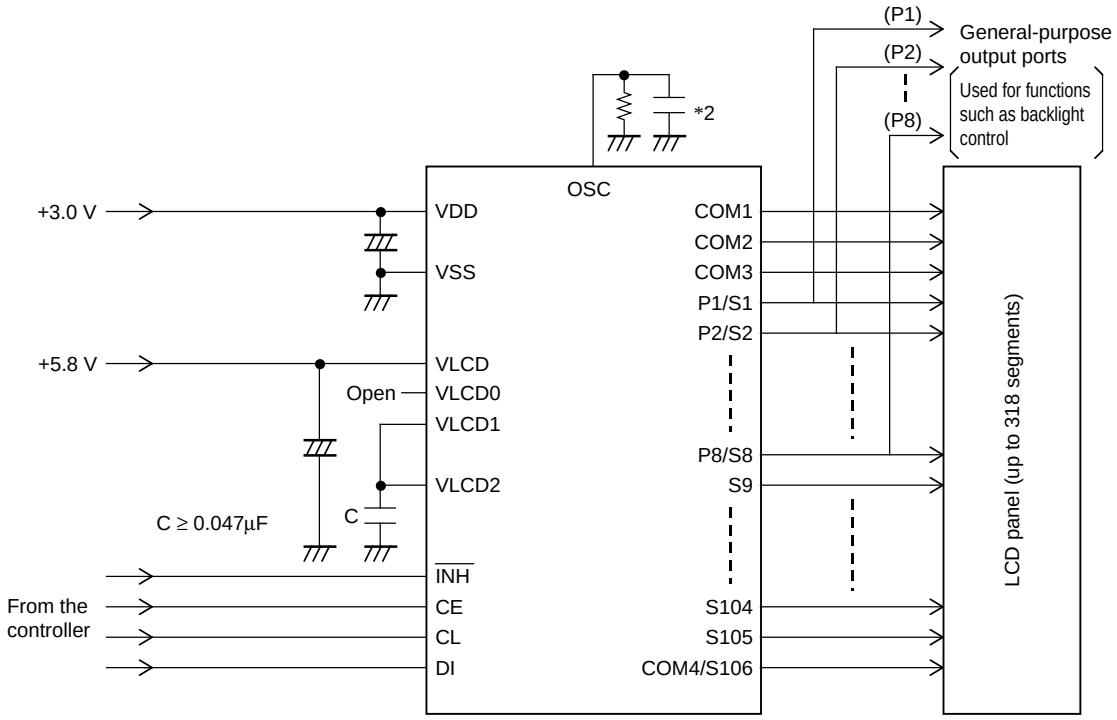
Figure 4

Notes on Controller Transfer of Display Data

Since the LC75847T accepts the display data (D1 to D318) divided into three separate transfer operations when using 1/3 duty drive scheme and the data (D1 to D420) divided into four separate transfer operations when 1/4 duty drive, we recommend that applications transfer all of the display data within a period of less than 30 ms to prevent observable degradation of display quality.

Sample Application Circuit 1

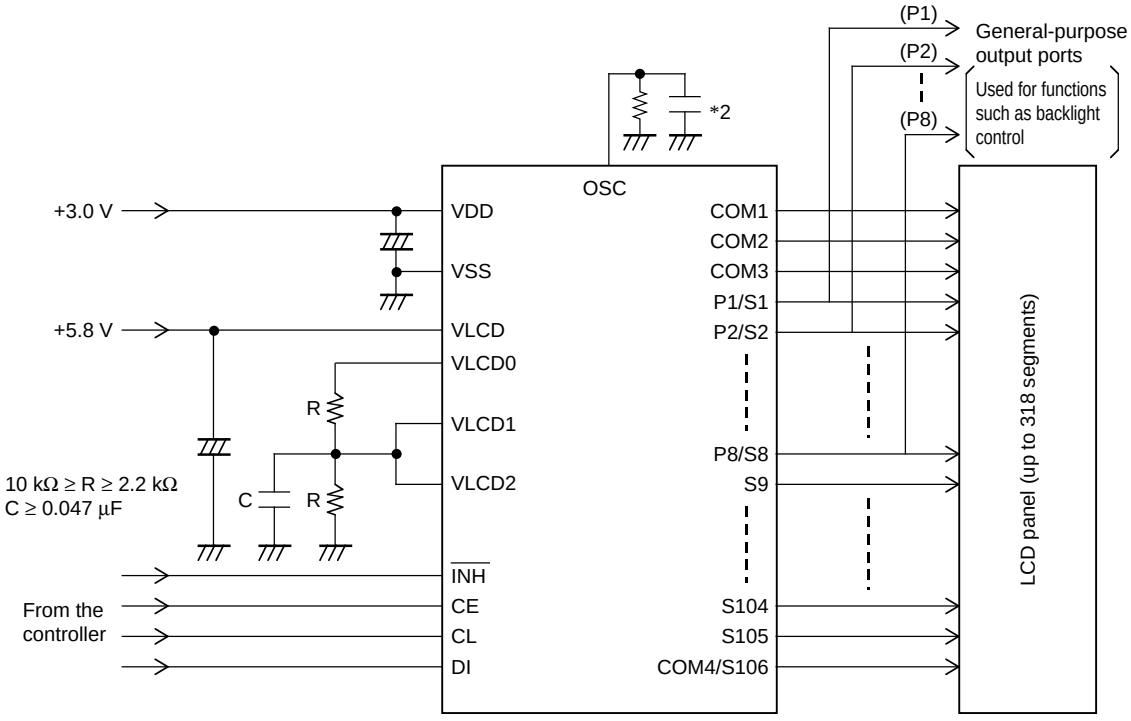
1/3 Duty, 1/2 Bias (for use with normal panels)



Note: *2 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 2

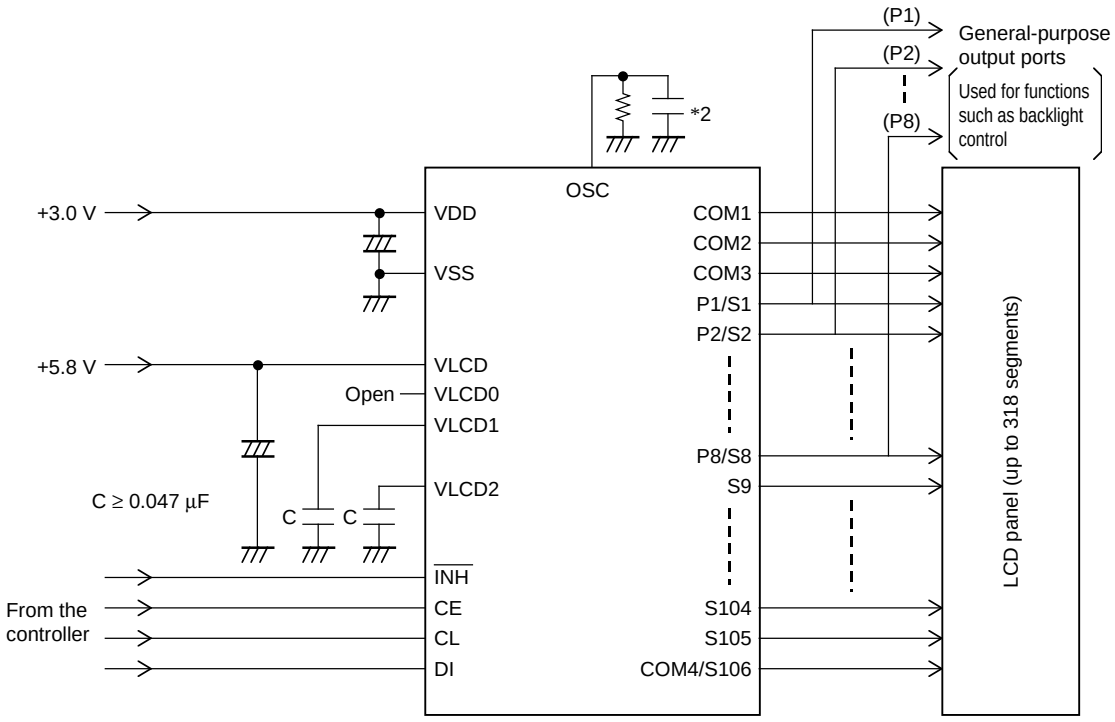
1/3 Duty, 1/2 Bias (for use with large panels)



Note: *2 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 3

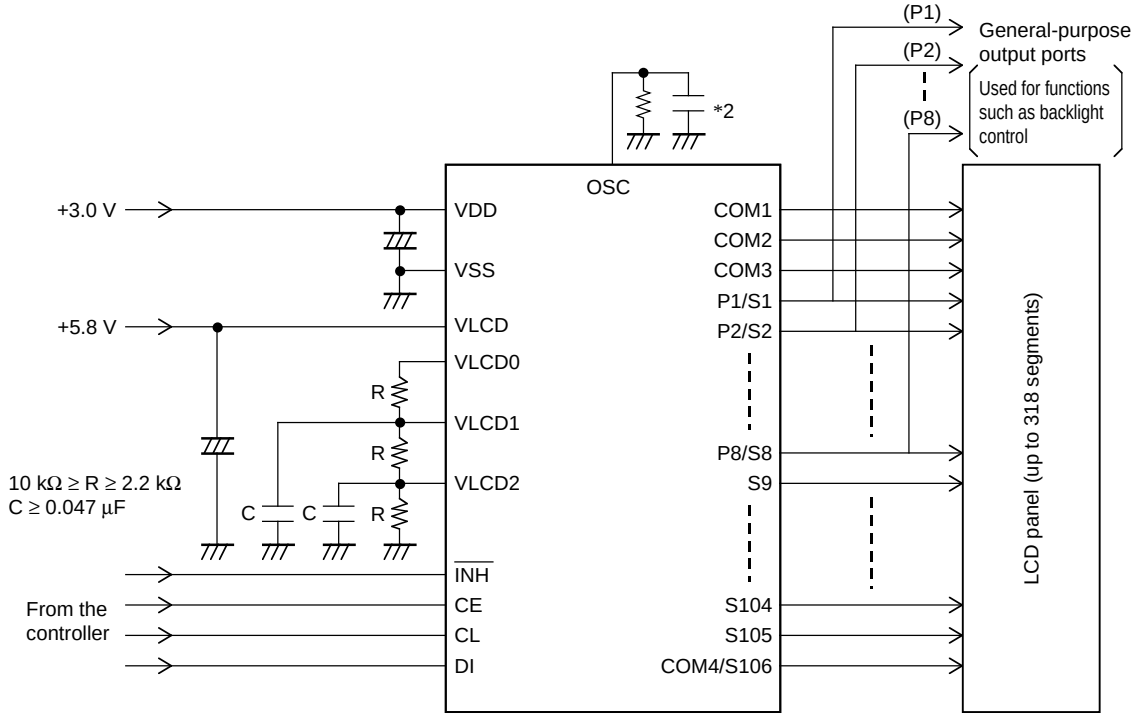
1/3 Duty, 1/3 Bias (for use with nornal panels)



Note: *2 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 4

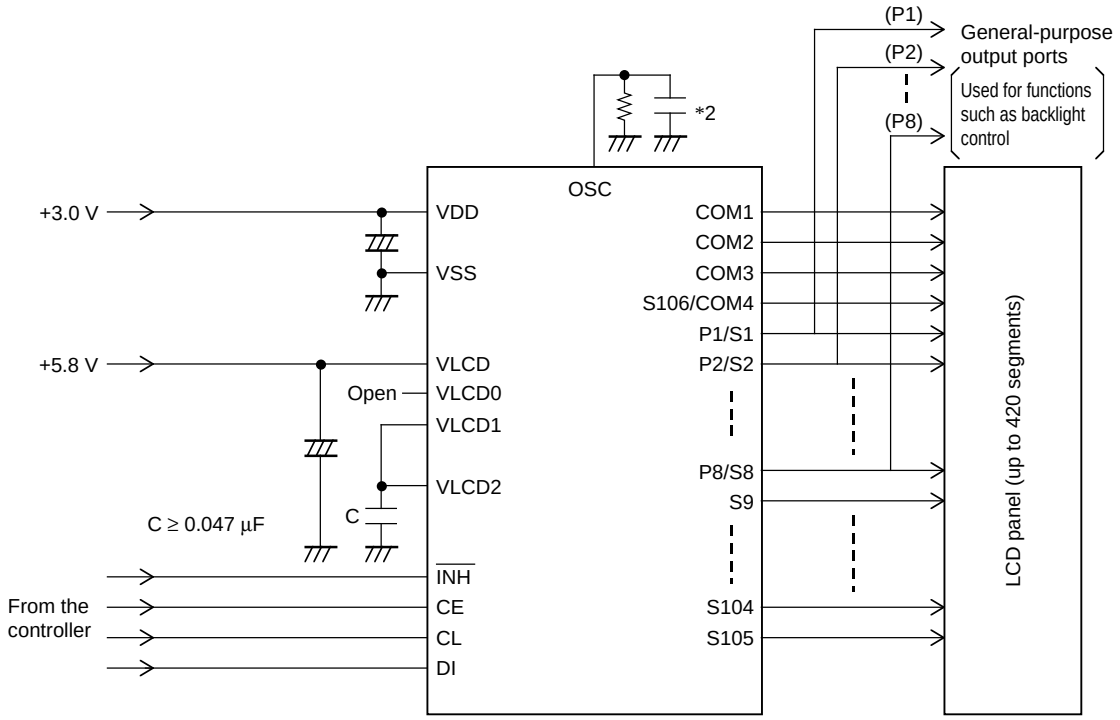
1/3 Duty, 1/3 Bias (for use with large panels)



Note: *2 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 5

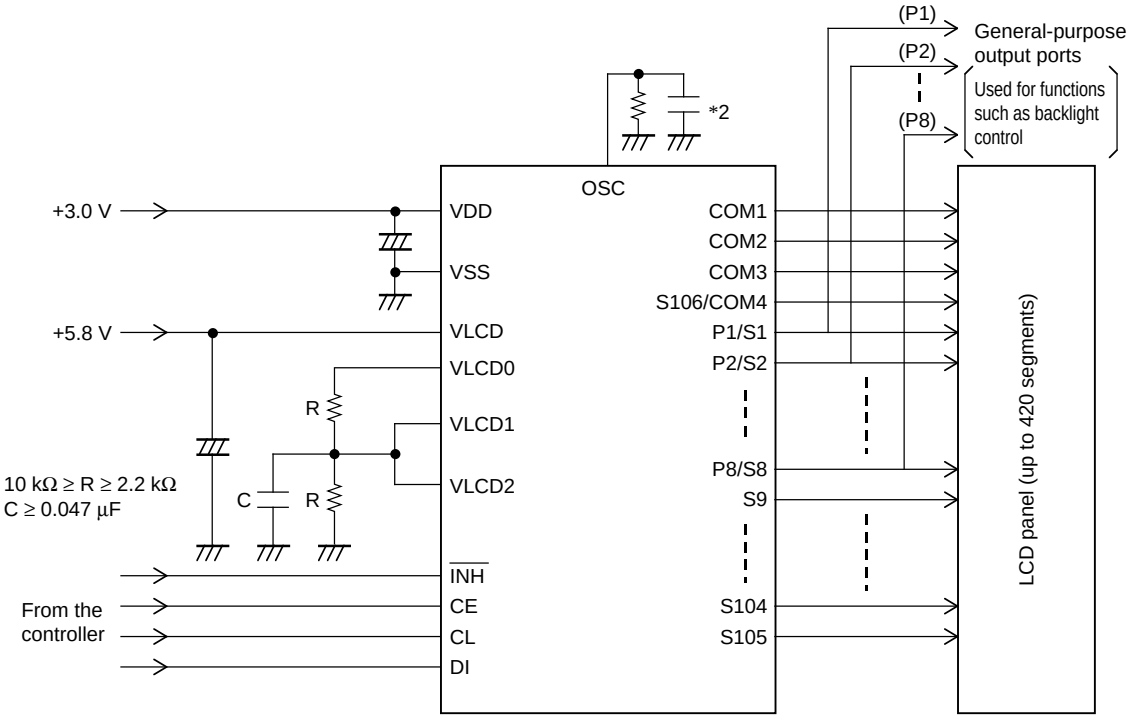
1/4 Duty, 1/2 Bias (for use with normal panels)



Note: *2 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 6

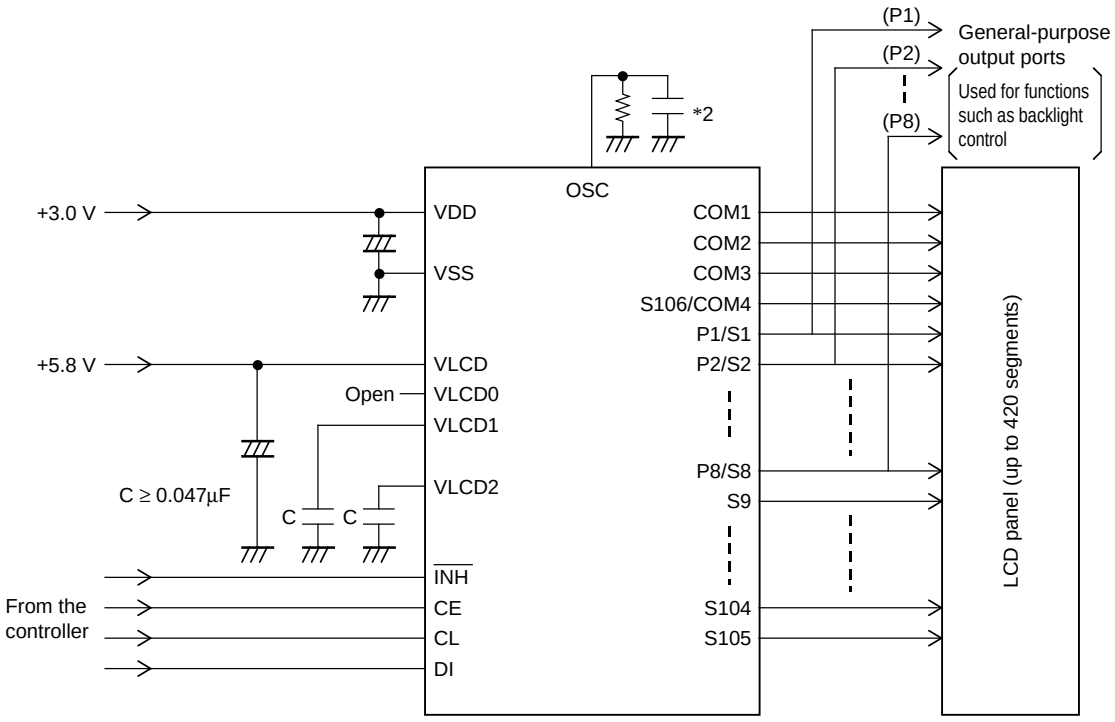
1/4 Duty, 1/2 Bias (for use with large panels)



Note: *2 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 7

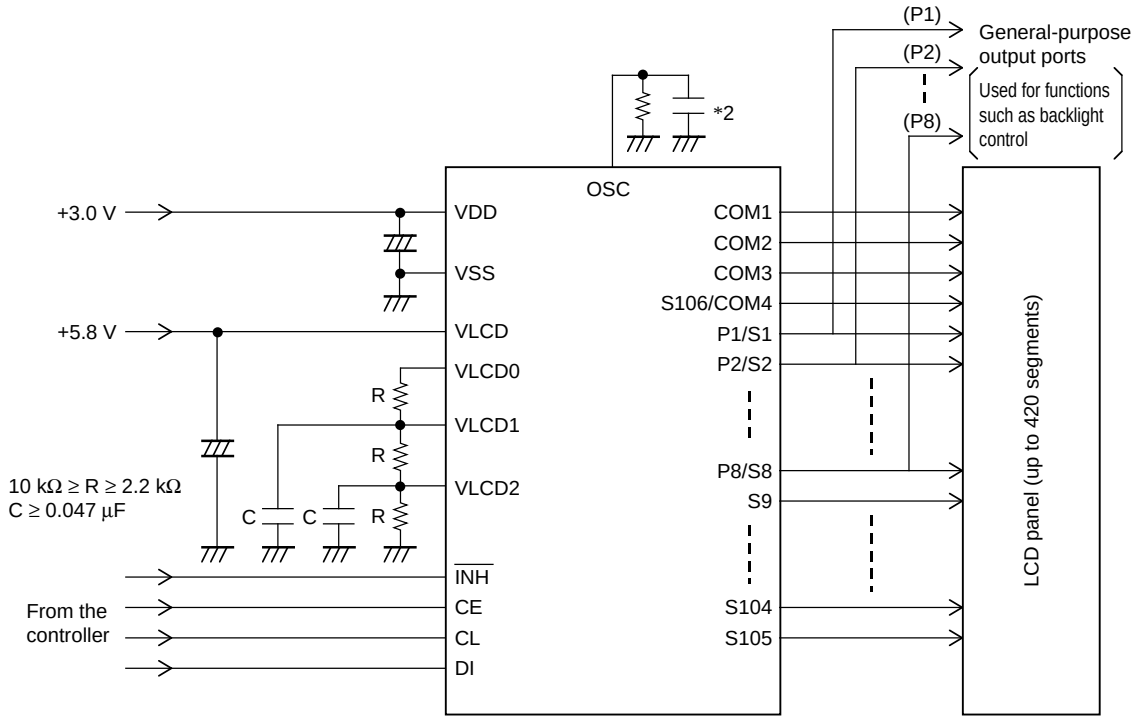
1/4 Duty, 1/3 Bias (for use with nornal panels)



Note: *2 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 8

1/4 Duty, 1/3 Bias (for use with large panels)

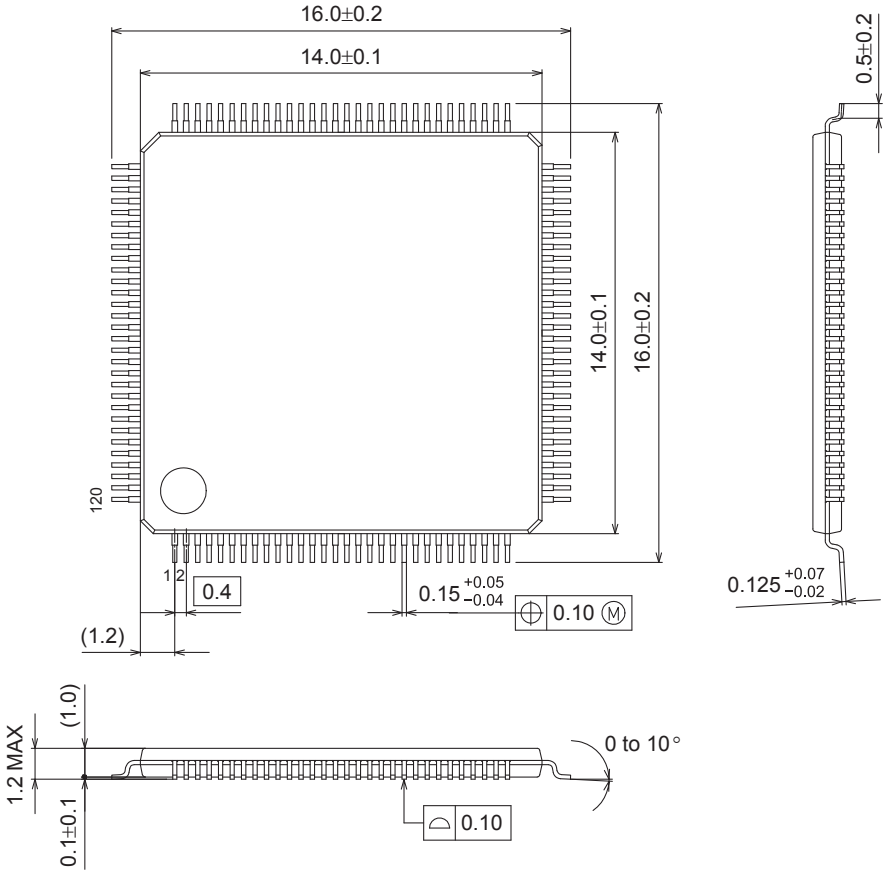


Note: *2 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

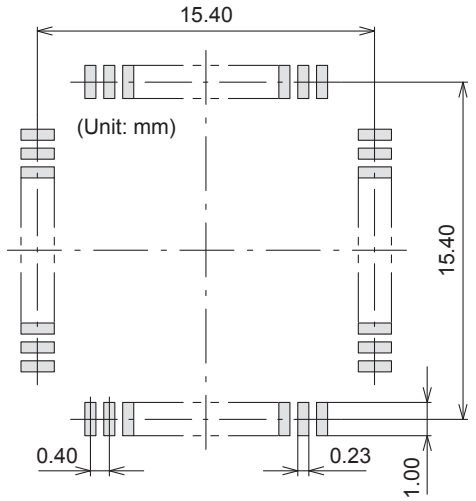
Package Dimensions

unit : mm

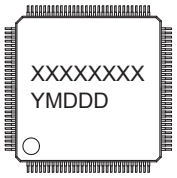
TQFP120 14x14 / TQFP120
CASE 932AZ
ISSUE A



SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “ ▪ ”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC75847T-E	TQFP120 14x14 / TQFP120 (Pb-Free)	450 / Tray JEDEC
LC75847TS-E	TQFP120 14x14 / TQFP120 (Pb-Free)	450 / Tray JEDEC

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