High Resolution Audio Signal Processing SoC with USB and Bluetooth® Controller

LC786830

Overview

The LC786830 integrates Arm® Cortex®−M0+, an Arm Cortex−M3 processor, audio DSP, USB controllers, SD card support, compressed audio decoder, Bluetooth audio, and car audio signals.

Multiple interfaces enable connection to external Flash memories to store program code for the Arm Cortex−M0+ and Arm Cortex−M3 processors and the audio DSP, making the device suitable for developing high−performance and multifunctional audio player systems.

Main Features

- Dual CPU System with Arm Cortex−M0+ and Cortex−M3 Processors
- Arm Cortex−M0+ Provides Overall System Control, Including Power Supply
- Arm Cortex−M3 Provides USB and Audio Playing Control
- USB2.0 OTG (High Speed and Full Speed) Controller, PHY (1 Port)
- USB2.0 Host (Full Speed) Controller, PHY (1 Port)
- Bluetooth Audio Playback
- Hands−free Audio Playback
- SD Memory Card Host Function
- Audio DSP Stored, Processing Decodes such as MP3*, WMA*, AAC*, FLAC*, SBC* (Capable for 24−bit and 192 kHz High−Resolution Audio Processing)
- Digital Audio Signal Processing Functions such as High−Frequency Range Extendable Filter, 22−Band Equalizer, Audio Mixing, Volume Control, etc.
- Analog Selector Input for Audio Input Function, Capable for Absorbing Clock Jitter by a Sampling Rate Converter in Asynchronous Conditions for Digital Input
- DA Converter Output for Audio Output (Fs: 96 kHz) or Digital 3−Wire Output (Fs: 192 kHz)

Power Supply / Temperature / External Form

- Operating Power Supply Voltage: 3.3 V (for I/O and Analog)
  1.2 V (for Internal Logic)
- Operation Ambient Temperature Range: −40°C to +85°C
- Package: LQFP208 (28 x 28) Lead and Halogen Free

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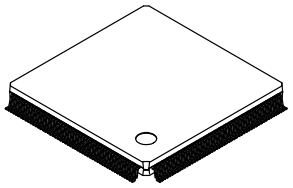

LQFP208
CASE 561AP

MARKING DIAGRAM

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 54 of this data sheet.

*MP3	MPEG Layer−3 Audio Coding
*AAC	Advanced Audio Coding
*SBC	Sub Band Codec
*Bluetooth profile	Copyright 1999−2014 OpenSynergy GmbH. All rights reserved. All unpublished rights reserved.
*WMA	Windows Media Audio
*FLAC	Free Lossless Audio Codec

ACRONYMS

The acronyms listed below are used thorughout this document to refer to internal blocks and functions of LC786830.

ACRONYMS

Acronyms	Description
ADC	Audio AD Converter
ALC	Automated Level Control
ASS	Audio Source Selector (Analog)
AudPLL1	Audio Clock PLL1 (for Fs = 32 or 48 kHz)
AudPLL2	Audio Clock PLL2 (for Fs = 44.1 kHz)
BCK	Bit Clock
BR	Bit Rate
ch	Channel
DAC	Audio DA Converter
DF	Audio Digital Filter
DMAC	DMA Controller
DPC	Digital Pitch Controller
Fs	Sampling Frequency
FS−USB	USB2.0 Full Speed
Gen−ADC	General AD Converter
GPIO	General Input−Output Port
HF	Handsfree
HS−USB	USB2.0 High/Full Speed
I/F	Interface
LPDSP	Audio DSP
LRCK	LR Clock
Mono	Monaural
NC/EC	Noise Canceller/Echo Canceller
Pdn	Pull−down
PEQ	Parametric Equalizer
PSRAM	Pseudo−SRAM
Pup	Pull−up
RTC	Real Time Clock
SDC	SD Card
SFlash	Serial Flash Memory
SIO	Serial Communication
SPI	Serial Peripheral Interface
SRC	Sampling Rate Converter
ST	Stereo
SysPLL	System Clock PLL
T.A	Time Alignment
WDT	Watchdog Timer

DETAILED BLOCK DIAGRAM

Functional blocks that are not shaded are powered off during shutdown.
And all analog IPs are set to standby in shutdown.

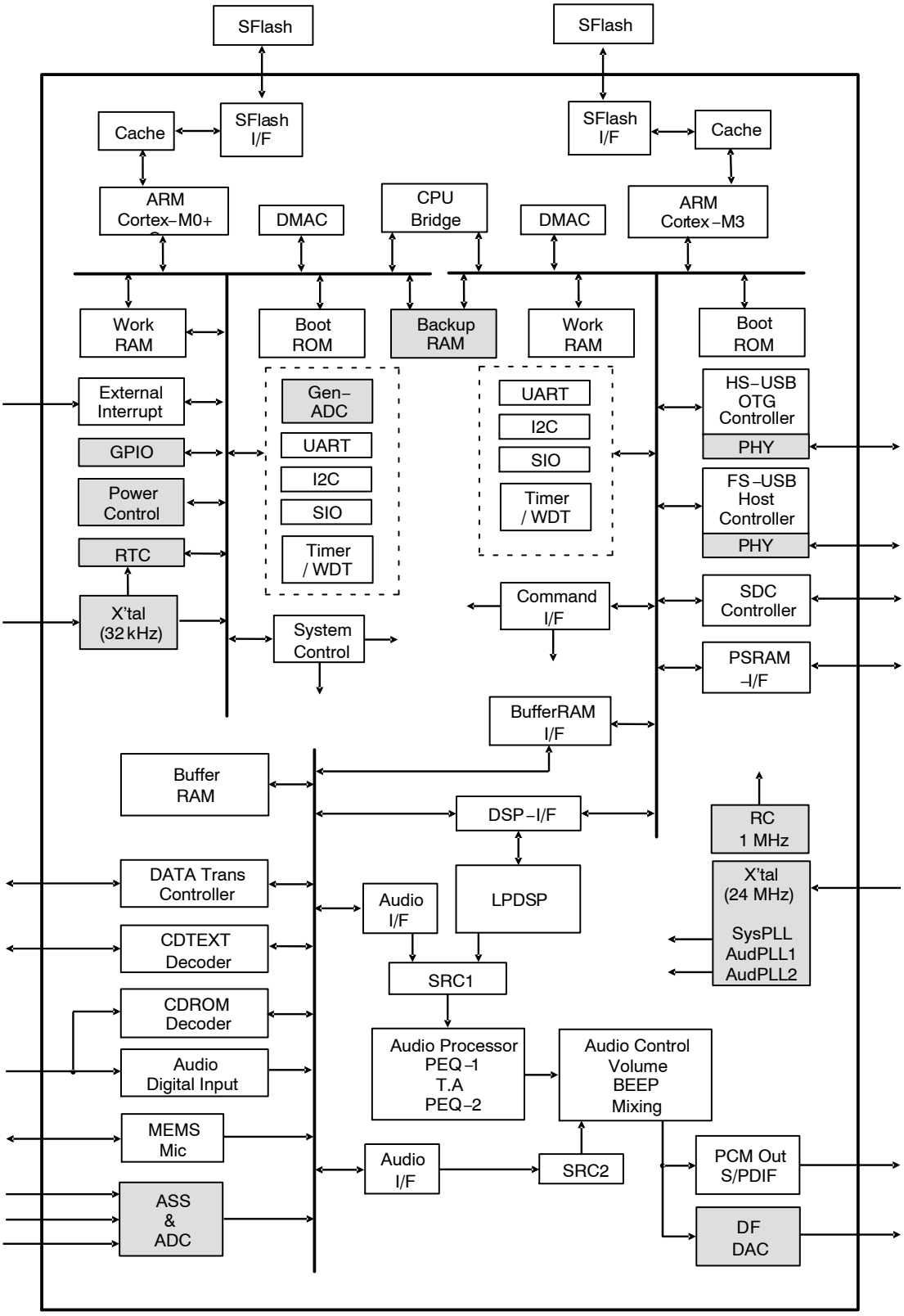

Figure 1. Detailed Block Diagram

DETAIL FUNCTIONS

Arm Cortex−M0+ Processor

Control

- Provides overall system control for the various components in the system (Power Supply Control, Key or Remote Controller Input, Display Control, Tuner Control, etc.)
- Cortex−M3 Control

Program Memory

- Integrated BootROM to start up
- Program stored in external Sflash
  Communication Sflash setup:
  Communication interface: Standard−SPI or Quad−I/O
  Memory size: Max 128 MB
  Operating clock: Dependent on Cortex−M0+ operating clock, Max: 30 MHz
- Integrated Cache Memory

Internal RAM

- Twotypes of integrated RAM
  1. Main RAM: For when the Cortex−M power supply is off shutdown.
  2. Backup RAM: For data backup during shutdown mode. Can be shared with Cortex−M3

Peripheral I/F

- GPIO: 47 ports (Shared with other functions)
- External Interrupt Pins: 8 pins (Shared with other functions)
- Serial I/F
  SIO Clock synchronized full duplex (3 lines): 4 ch (Shared with other functions)
  UART Full duplex: 3 ch (Shared with other functions)
  I^2C Master function: 3 ch (Shared with other functions)
  PWM: 4 ch (Shared with other functions)
- 12−bit Gen−ADC input: 8 inputs (Shared with other functions)

Others

- DMAC: 3 ch
- RTC: Supports operation at shutdown
- Timer: 7 ch (4 ch for capture input or Capable of PWM output)
- WDT: 1 ch

Arm Cortex−M3 Processor

Control

- Provides sequence control during audio playback
  USB and SDC file analysis and audio playing controls
  Bluetooth Audio playback and HF playback controls
  LPDSP decode control for various audio compression data
  Audio PEQ, Acoustic signal processing control

Program Memory

- BootROM to start
- Program stored in external SFlash (for Cortex−M3 / LPDSP)
  Corresponding SFlash setup:
  Communication interface: Standard−SPI or Quad−I/O
  Memory size: Max. 128 MB
  Operating clock: Depend on Cortex−M3 operating clock, Max: 60 MHz
- Integrated Cache Memory

Internal RAM

- Build−in dedicated Work RAM
- Can be used as shared RAM, providing access as:
  1. Back−up for Cortex−M0+
  2. LPDSP memory
  3. Audio data buffer memory

Peripheral I/F

- GPIO: 58 ports (Shared with other functions)
- External Interrupt Pins: 3 pins (Shared with other functions)
- Serial I/F
  SIO Clock synchronized full duplex (3 lines): 4 ch (Shared with other functions)
  UART Full duplex: 3 ch (Shared with other functions)
  Full duplex (Supports CTS / RST): 1 ch (Shared with other functions)
  I^2C Master function: 3−ch (Shared with other functions)
- PSRAM−I/F
  Corresponding PSRAM setup:
  Communication Format: SPI Mode, Parallel Mode or QPI Mode
  Memory Size: Max. 8 MB
  Operating Clock: Depend Cortex−M3 operating clock, Max 30 MHz
- USB−I/F: For HS−USB (OTG) and FS−USB (Host) Controller
- SDC−I/F

Others

- DMAC: 6 ch
- Timer: 4 ch
- WDT: 1 ch

External Interface

USB−I/F

- Embedded 2 Port USB−Function, HS−USB and FS−USB
  1. HS−USB I/F
     Embedded USB2.0 High/Full Speed Controller and PHY

Universal Serial Bus Specification 2.0 High/Full Speed compliant
On−The−Go and Embedded Host Supplement to the USB Revision 2.0 Specification compliant (ADC is not supported)

2. FS−USB I/F
   Embedded USB2.0 Full Speed Controller and PHY
   Open HCI (Open Host Controller Interface) 1.0a compliant
   Universal Serial Bus Specification 2.0 Full Speed compliant

SDC−I/F

- Multimedia Card Specification v2.11 compliant
- Secure Digital Memory Card Physical Layer Specification v0.96 compliant

LPDSP Function

System Configuration

- Integrated SRAM for program and data memory
- Programs are stored in SFlash. Cortex−M3 downloads necessary programs.
- Input−output buffer
  Input Buffer Memory: Embedded SRAM for Channel 1 and Channel 2
  Output Buffer Memory: Embended SRAM

Audio Decode Processing

- The following audio decode programs are available

1. MP3: ISO/IEC 11172−3, ISO/IEC 13818−3 compliant
   Supported Fs MPEG1−Layer1/2/3 (32 kHz, 44.1 kHz, 48 kHz)
   MPEG2−Layer1/2/3 (16 kHz, 22.05 kHz, 24 kHz)
   MPEG2.5−Layer3 (8 kHz, 11.025 kHz, 12 kHz)
   Supported BR All the bit rate including VBR
2. WMA: WMA Ver.9.2 Standard compliant
   Supported Fs 8 kHz to 48 kHz
   Supported BR 5 kbps to 384 kbps (Supports VBR)
3. AAC: ISO/IEC 14496−3, 13818−7 compliant
   Supported Profile MPEG2−AAC, MPEG4−AAC−LC (Low Complexity)
   Supported Fs 8 kHz to 96 kHz
   Supported BR 8 kbps to 1152 kbps (Supports VBR)
   (*)LATM (Low Overhead Audio Transport Multiplex) for Bluetooth
4. FLAC: FLAC 1.3.0 compliant
   Supported Format Block size: up to 4608
   Quantization Bit Number 8, 16 or 24 bit per sample
   Supported Fs 8 kHz to 192 kHz
   Supported channels 1 ch or 2 ch
5. PCM (WAVE)
   Supported Fs 8 kHz to 192 kHz
   Supported channels 1 ch or 2 ch
6. SBC: Bluetooth A2DP Ver1.2 compliant
   Supported Format Block Length: 4, 8, 12 or 16, Subband: 4 or 8, SNR, Loudness
   Supported Fs 16 kHz, 32 kHz, 44.1 kHz, 48 kHz
   Supported BR to 512 kbps
7. NC/EC
   Supported Fs 8 kHz or 16 kHz
8. DPC: Support for audio data playback pitch control
   Control speed range PCM 0.5 to 2.0 speed, MP3: 0.5 to 1.5 speed
   (*) Capable of preventing sound drop out for Bluetooth (0.9 to 1.1 speed)
9. HF−Filter: High frequency compensation for compressed audio playback
   Supported Fs 32 kHz, 44.1 kHz or 48 kHz
10. De−emphasis Filter
    Supported Format 50 / 15 μs, CCITTj, 17
    De−emphasis for MP3 playing and audio CD playing
11. Voice Cancellation
    Ability to delete the singing voice during audio playback, suitable for Karaoke use

Audio Processing Function

Audio Input Function

- Analog Audio Data Input
  Microphone (Monaural) Input: 1 ch (for differential input)
  Input Gain: 0, +18, +24, or +30 dB
  Stereo (Single Ended) Input: 4 ch (2 ch for differential input)
  Input Gain: −12 dB to +19 dB (1 dB step)
  ADC: 24−bit accuracy, convert Fs up to max. 48 kHz
- Digital Audio Input
  Numbers of ch: max. ST 5 ch (Max)
  Format: Digital 3 wires (LRCK, BCK and Data)
  I2S, MSB First Right−justified, Left−justified, Long or Short Frame Synchronization
  LRCK and BCK for Master or Slave mode (Supports BCK of 32 fs or 64 fs in master mode)
  Fs / Data: Data 16− or 24−bit
  Fs = 8 kHz to 192 kHz (With SRC, capable for absorbing clock jitter among devices)

- MEMS Microphone Input

Digital Data Input (PDM format)	Clock Output and Data Input
Input Fs	8 kHz to 48 kHz
IIR Filter	Built−in IIR filters, one is 1−pole and the other is 2−pole and arbitrary coefficient setting is possible.
Automatic Level Control	−33 dB to +48 dB (0.25 dB Step)
Silence Detection	Ability to set desired level
Output Data	Mute (−∞), attenuator support

Audio Signal Processing

- SRC: 2 ch (Asynchronous input and output, 24−bit accuracy)
  Frequency conversion range 8 kHz to 192 kHz
  1. SRC for Main Data
     Convert Fs for audio main data into desired Fs
  2. SRC for Sub Data
     Convert speech/voice input during HF playback into FS for EC/NC processing
     Convert mixing data to match main data Fs
- PEQ−1: 24bit data, two−pole IIR filter
  Various equalizer characteristics can be achieved by changing the filter coefficients
  The following are supported, based on the number of audio data channels
  1. ST 1 ch Data: Max. 22 Band PEQ
  2. ST 2 ch Data: Max. 11 Band PEQ
- T.A Function
  Convert 2 channels (ST 1channel) input to 6 channels (ST 3channels: Front, Rear and Subwoofer) output
  The desired delay for output data can be set for each channel
  (max. 21 ms delay at Fs = 192 kHz)
- PEQ−2: 24−bit data, two−poles IIR filter
  Various equalizer characteristics can be achieved by changing the filter coefficients
  Capable of processing EQ 2 Band and Fade−In or Out for each of ST 3channels
  ST 1 ch (for sub−wafer) Input Data
  Available for direct or Left channel and Right channel addition ((L ch + R ch) / 2)
  Capable of reading data for level meter
- Mixing Function
  Mixing monaural data (1channel) into main data
  (Capable for mixing data to process 2Band−PEQ)
  Capable of mixing two modes
  1. Mixing with main data (ST 1 ch: Front) before main volume
  2. Mixing with main data (ST 2 ch: Front and Rear) before main volume

Audio Output Function

- Volume
  Output Range: −∞ to +42 dB
  Change Rate: support dB setting or Linear setting
  (dB setting: supports down to 1/32 dB as the minimum)
  Built−in 9 ch for volume function, capable of independent control for each ch
  1. Main Volume: 6 ch (ST 3 ch: Front, Rear and Subwoofer)
  2. Mixing level for adjustment−1: 2 ch (ST 1 ch: Front)
  3. Mixing level for adjustment−2: 1 ch (Monaural: For mixing)
- Beep Sound Output Function: 4 ch (ST 2 ch)
  Capable of outputting a desired frequency for main data (ST 2 ch: Front and Rear) output
- DAC Output: 5 ch (Front L ch and R ch, Rear L ch and R ch, Subwoofer)
  24−bit accuracy, x8 Oversampling Digital Filter
  Max. 96 kHz for output Fs
  Built−in two−pole LPF for audio output
- Audio PCM Output
  Format: Digital Output (LRCK, BC and Data)
  Support format: I2S, MSB First Right−justified and Left−justified (Long or short frame can be supported during Bluetooth HF Playback)
  LRCK and BCK for Master or Slave mode (Supports BCK of 32 fs or 64 fs in master mode
  Support for I2S and BCK of 64 fs in slave mode)
  Fs / Data: 24−bit data output
  Support Fs output from 8 kHz to 192 kHz
  Capable for data to output max. St 3 channels at the same time (Digital 5 wires output: LRCK, BCK, Front−L/R, Rear−L/R and Subwoofer−L/R)
  Capable of 128 or 256 Fs Clock Output (Fs = 8 kHz to 192 kHz)
- S/PDIF Output (Fs = 8 kHz to 192 kHz)
- Mute (−∞ / −12 dB) (Capable of muting after main volume control)

CD−DSP IC Connection Usage

CD−TEXT Function

- Support for CD−TEXT data buffering
- Ability tot start buffering from desired ID3 and ID4 of CD−TEXT data
  CD−DSP must be connected to the following 4 wires: Sub code synchronization signals (SBSY and SFSY), serial clock (SBCK), and data (PW).

CDROM Function

- Supports max. 4x speed decode operation
- Supports CDROM Mode1, Mode2−Form1 and Mode2−Form2
  CD−DSP must be connected to the following 3 wires: LRCK, BCK, and DATA

Clock Function

Oscillator

- System Clock: 24.000 MHz
- RTC: 32.768 kHz

Clock for System

- SysPLL: built−in PLL, clock generation for CPU and peripheral
- RC Oscillation: CPU start−up clock
- PLL for USB: built−in PLL, 48 MHz and 480 MHz clock generation for USB

Clock for Audio

- AudPLL stored: 2 ch PLL
  AudPLL1: Fs = 32 or 48 kHz series clock generation
  (*) includes 96 kHz or 192 kHz
  AudPLL2: Fs = 44.1 kHz series clock generation

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Pin Name	Condition	Rating	Unit
$V_{DD\ max}$	Supply Voltage	AVDD1, AVDD2, AVDD3, AVDD4, AVDD5, DVDD, UVDD1, UVDD2, XVDD		−0.3 to +3.95	V
VDD12 max		DVDD12, UVDD12, XVDD12		−0.3 to +1.4	
VSS		AVSS1, AVSS2, AVSS3, AVSS4, AVSS5, DVSS, UVSS1, UVSS2, XVSS, XVSS12		−0.3 to +0.3	
VIN	Input Voltage	Digital input pin		−0.3 to DVDD+0.3	
VOUT	Output Voltage	Digital input or output pin		−0.3 to DVDD+0.3	
AVIN	Analog Input Voltage	Analog input pin		−0.3 to DVDD+0.3	
Pdmax	Allowable Power Dissipation		Ta ≤ 85°C Mounted reference on PCB (Note 1)	1.23	W
Topr	Operating Temperature			−40 to +85	°C
Tstg	Storage Temperature			−40 to +125	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Reference PCB: 114.3 mm x 101.6 mm x 1.6 mm, 4−layer, glass epoxy resin. Uses a substrate conforming to JEDEC standard JESD 51−7.

ALLOWABLE OPERATING RANGES

Symbol	Item	Pin Name	Condition	Min	Typ	Max	Unit
IN RUN MODE (Ta = −40 to 85°C, DVSS = AVSS1 = AVSS2 = AVSS3 = AVSS4 = AVSS5 = UVSS1 = UVSS2 = XVSS = XVSS12 = 0 V)							
V_{DD}	Supply Voltage	AVDD1, AVDD2, AVDD3, AVDD4, AVDD5, DVDD, UVDD1, UVDD2, XVDD		3.00	3.30	3.60	V
$V_{DD}12$		DVDD12, UVDD12, XVDD12		1.14	1.20	1.26	
$I_{DD}1$	Current Consumption (Note 2)	AVDD1, AVDD2, AVDD3, AVDD4, AVDD5, DVDD, UVDD1, UVDD2, XVDD		−	−	175	mA
I_{DD2}		DVDD12, UVDD12, XVDD12		−	−	150	mA
FX_{24M}	Oscillator Frequency	X24MIN	Oscillator circuit	−	24.000	−	MHz
		X24MOUT					
FX_{32K}		X32KIN		−	32.768	−	kHz
		X32KOUT					
IN SHUTDOWN MODE (Ta = 25°C, VDD = 3.3 V / VDD12 = 1.2 V, DVSS = AVSS1 = AVSS2 = AVSS3 = AVSS4 = AVSS5 = UVSS1 = UVSS2 = XVSS = XVSS12 = 0 V							
I_{DD1S}	Current Consumption (Note 3)	AVDD1, AVDD2, AVDD3, AVDD4, AVDD5, DVDD, UVDD1, UVDD2, XVDD		−	35	55	μA
I_{DD2S}		DVDD12, UVDD12, XVDD12		−	100	280	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. The current consumption measurement conditions are as follows.
   - Cortex−M0+ Operating Frequency: 60 MHz and SFlash Cache ON (SFlash: 30 MHz Access)
     Peripherals: Gen−ADC, SIO (3 ch), UART (3 ch), PWM (1 ch) are running.
   - Cortex−M3 Operating Frequency: 120 MHz and SFlash Cache ON (SFlash: 60 MHz Access)
     Peripherals: High Speed USB and Fast UART, I^2C (1 ch) are running.
   - LPDSP Operating Frequency: 150 MHz and flac decode (Fs: 192 kHz) program execute.
   - Other hardware 24 MHz xtal, 32 kHz crystal are oscillating, SysPLL, AudPLL1, AudPLL2 are executing,
     Audio analog input: ADC is running / Fs: 48 kHz
     Audio analog output: DAC (5 ch) are running / Fs: 96 kHz
     Audio digital output: IIS 3 ch output / Fs: 192 kHz, 256 fs clock output.
3. Current value in shutdown mode with all functions stopped except for the following: 32 kHz crystal is oscillating, RTC function is running and Backup RAM data storage function is running.

DC CHARACTERISTICS (Ta = −40 to 85°C, DVSS = AVSS1 = AVSS2 = AVSS3 = AVSS4 = AVSS5 = UVSS1 = UVSS2 = XVSS = XVSS12 = 0 V)

Symbol	Item	Pin Name	Condition	Min	Typ	Max	Unit
VIH(1)	High−level Input Voltage	(1), (2), (3), (4), (5), (6)	Schmitt	2.10	−	V_{DD} +0.3	V
VIH(2)		(7), (9)	CMOS	0.7x VDD	−	V_{DD} +0.3	V
VIL(1)	Low−level Input Voltage	(1), (2), (3), (4), (5), (6)	Schmitt	VSS −0.3	−	0.80	V
VIL(2)		(7), (8)	CMOS	VSS −0.3	−	0.3x VDD	V
I_{IN}	Off−leakage Input Current	(1), (2), (3), (4), (5), (6), (7), (8), (9)	V_{IN} = V_{DD}1 or V_{IN} = 0 V Integrated Pup / Pdn OFF	−10.0	−	10.0	μA
V_{OH}(1)	High−level Output Voltage	(1), (2), (4), (6)	CMOS I_{OH} = −2 mA	V_{DD} −0.6	−	−	V
V_{OH}(2)		(1), (2), (4), (5)	CMOS I_{OH} = −4 mA				
V_{OH}(3)		(4), (5)	CMOS I_{OH} = −8 mA				
V_{OL}(1)	Low−level Output Voltage	(1), (2), (4), (6)	CMOS I_{OL} = 2 mA	−	−	0.4	V
V_{OL}(2)		(1), (2), (4), (5)	CMOS I_{OL} = 4 mA				
V_{OL}(3)		(4), (5)	CMOS I_{OL} = 8 mA				
RPD	Built−in Pdn Resistor	(1), (2), (4), (5)		30	60	120	kΩ
RPU	Built−in Pup Resistor	(4), (6)		25	50	100	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Analog pin, USB pin, and oscillator connection pin are excluded.
5. In case of using any pins shown as (2) as GPIO
6. The drive strength of any pin shown as (1) or (2) can be changed to 2 mA or 4 mA
7. The drive strength of any pin shown as (4) can be changed to 2 mA, 4 mA or 8 mA
8. The drive strength of any pin shown as (5) can be changed to 4 mA or 8 mA
9. Any pins shown as (1), (2) can be set as N−channel open drain.
   However, input “H” level depends on VIH.

NOTES:

(1) GP00_0, GP00_1, GP00_2, GP00_3, GP00_4, GP00_5, GP00_6, GP00_7,
GP01_0, GP01_1, GP01_2, GP01_3, GP01_4, GP01_5, GP01_6, GP01_7,
GP02_0, GP02_1, GP02_2, GP02_3, GP02_4, GP02_5, GP02_6, GP02_7,
GP03_0, GP03_1, GP03_2, GP03_3, GP03_4, GP03_5, GP03_6,
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GP13_0, GP13_1, GP13_2, GP13_3, GP13_4, GP13_5, GP13_6, GP13_7,
GP14_0, GP14_3

(2) GP05_0, GP05_1, GP05_2, GP05_3, GP05_4, GP05_5, GP05_6, GP05_7

(3) RESB, M0_SWCK, M3_SWCK

(4) SFLCS1, SFLWP1, SFLHOLD1, SFLCS2, SFLWP2, SFLHOLD2

(5) SFLCL1, SFLDI1, SFLDO1, SFLCL2, SFLDI2, SFLDO2

(6) GP04_0, M0_SWDT, M3_SWDT

(7) GP04_1, GP07_7, GP14_1, GP14_2

(8) TEST0, TEST1, TEST2, TEST3

(9) MODE

PIN ASSIGNMENT

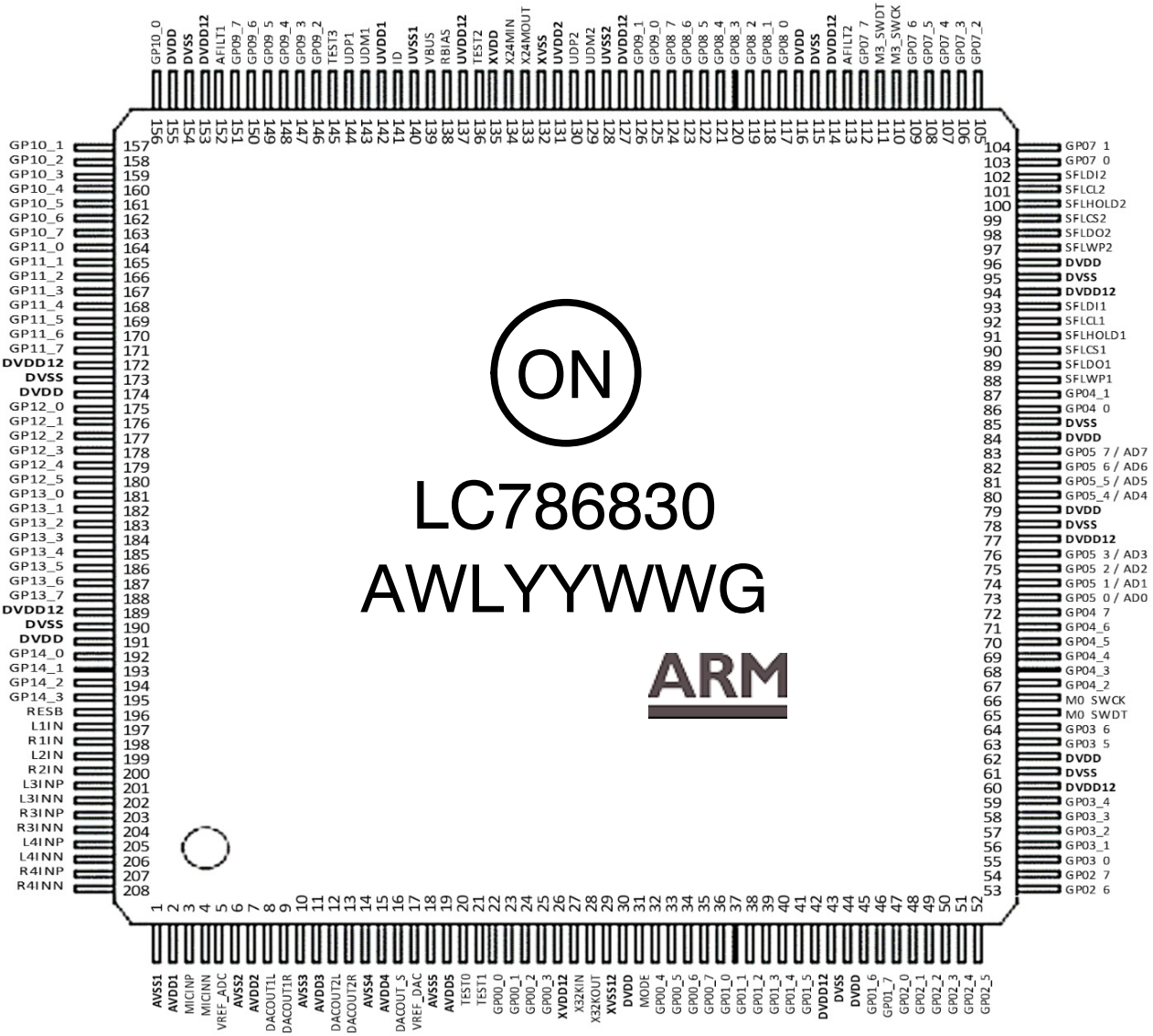


Figure 2. Pin Assignment

PIN DESCRIPTION

Pin No.	Pin Name	I/O	State when "Reset"	Description
1	AVSS1	–	–	Analog system (ASS) ground. This pin must be connected to 0 V.
2	AVDD1	–	–	Analog system (ASS) power supply
3	MICINP	AI	Input	Differential input for microphone (Positive)
4	MICINN	AI	Input	Differential input for microphone (Negative) (Connected to GND for microphone)
5	VREF_ADC	AO	AVDD2 / 2	Capacitor connection pin for ADC reference voltage
6	AVSS2	–	–	Analog system (ADC) ground. This pin must be connected to 0 V.
7	AVDD2	–	–	Analog system (ADC) power supply
8	DACOUT1L	AO	Undefined	DAC Left channel Output−1 (for Front)
9	DACOUT1R	AO	Undefined	DAC Right channel Output−1 (for Front)
10	AVSS3	–	–	Analog system (DAC) ground. This pin must be connected to 0 V.
11	AVDD3	–	–	Analog system (DAC) power supply
12	DACOUT2L	AO	Undefined	DAC Left channel Output−2 (for Rear)
13	DACOUT2R	AO	Undefined	DAC Right channel Output−2 (for Rear)
14	AVSS4	–	–	Analog system (DAC) ground. This pin must be connected to 0 V.
15	AVDD4	–	–	Analog system (DAC) power supply
16	DACOUT_S	AO	Undefined	DAC Output (for Subwoofer)
17	VREF_DAC	AO	AVDD5 / 2	Capacitor connection pin for ADC reference voltage
18	AVSS5	–	–	Analog system (DAC) ground. This pin must be connected to 0 Vl.
19	AVDD5	–	–	Analog system (DAC) power supply
20	TEST0	I	Input	Test input. This pin must be connected to 0 V.
21	TEST1	I	Input	Test input. This pin must be connected to 0 V.
22	GP00_0	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ External Interrupt _0 input Shutdown mode release control_0 input
23	GP00_1	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ External Interrupt _1 input Shutdown mode release control_1 input
24	GP00_2	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ External Interrupt _2 input Shutdown mode release control_2 input
25	GP00_3	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0 External Interrupt _3 input Shutdown mode release control_3 input
26	XVDD12	–	–	Oscillator (1.2 V) power supply
27	X32KIN	I	Oscillation	X'tal oscillator connection (32.768 kHz)
28	X32KOUT	O	Oscillation	X'tal oscillator connection (32.768 kHz)
29	XVSS12	–	–	Oscillator ground. This pin must be connected to the 0 V.
30	DVDD	–	–	Digital system (3.3 V) power supply
31	MODE	I	Input	Mode input ("H"−active) This pin must be connected to "VDD".

PIN DESCRIPTION (continued)

Pin No.	Pin Name	I/O	State when "Reset"	Description
32	GP00_4	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ External Interrupt _4 input Capture input for timer4 (exclusive with GP00_5, 6, 7) Shutdown mode release control_4 input
33	GP00_5	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ External Interrupt _5 input Capture input for timer4 (exclusive with GP00_4, 6, 7) Shutdown mode release control_5 input
34	GP00_6	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ External Interrupt _6 input Capture input for timer4 (exclusive with GP00_4, 5, 7) Shutdown mode release control_6 input
35	GP00_7	I/O	Input (L)	General purpose I/O port with Pdn resistor Cortex−M0+ External Interrupt _7 input PWM output for timer4 / Capture input (exclusive with GP00_4, 5, 6) Shutdown mode release control_7 input
36	GP01_0	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Clock output for I^2C channel−1 (Note 10) Clock output for serial data communication channel−1
37	GP01_1	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Data input −output for I^2C channel 1 (Note 10) Receive data input for serial data communication channel−1
38	GP01_2	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Transmit data output for serial data communication channel−1
39	GP01_3	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ PWM output for timer5 or Capture input
40	GP01_4	I/O	Input (L)	General purpose I/O port with Pdn resistor
41	GP01_5	I/O	Input (L)	General purpose I/O port with Pdn resistor
42	DVDD12	−	−	Digital system (1.2 V) power supply
43	DVSS	−	−	Digital system ground. This pin must be connected to 0 V.
44	DVDD	−	−	Digital system (3.3 V) power supply
45	GP01_6	I/O	Input (L)	General purpose I/O port with Pdn resistor
46	GP01_7	I/O	Input (L)	General purpose I/O port with Pdn resistor Cortex−M0+ PWM output for timer6 or Capture input
47	GP02_0	I/O	Input (L)	General purpose I/O port with Pdn resistor
48	GP02_1	I/O	Input (L)	General purpose I/O port with Pdn resistor
49	GP02_2	I/O	Input (L)	General purpose I/O port with Pdn resistor
50	GP02_3	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Transmit data output for serial communication channel−2
51	GP02_4	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Clock input/output for I^2C data channel−2 (Note 10) Clock output for serial communication channel−2

PIN DESCRIPTION (continued)

Pin No.	Pin Name	I/O	State when "Reset"	Description
52	GP02_5	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Data input/output for I^{2}C data channel−2 (Note 10) Receive data input for serial communication channel−2
53	GP02_6	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Data output for UART channel−1
54	GP02_7	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Data input for UART channel−1
55	GP03_0	I/O	Input (L)	General purpose I/O port with Pdn resistor
56	GP03_1	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Clock output for serial communication channel−4 (exclusive with GP05_5) Data output for UART channel−2 (exclusive with GP05_4)
57	GP03_2	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Receive data input for serial communication channel−4 (exclusive with GP05_6) Data input for UART channel−2 (exclusive with GP05_5)
58	GP03_3	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Transmit data output for serial communication channel−4 (exclusive with GP05_7)
59	GP03_4	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Clock output for I^{2}C data channel−3 (Note 10) Clock output for serial communication channel3 Data output for UART channel−3 (exclusive with GP05_6)
60	DVDD12	−	−	Digital system (1.2 V) power supply
61	DVSS	−	−	Digital system ground. This pin must be connected to 0 V.
62	DVDD	−	−	Digital system (3.3 V) power supply
63	GP03_5	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Data input/output for I^{2}C communication data channel−3 (Note 10) Receive data input for serial communication channel−3 Data input for UART communication channel−3 (exclusive with GP05_7)
64	GP03_6	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Transmit data output for serial communication channel−3
65	M0_SWDT	I/O	Input (H)	Debugger port (for Cortex−M0+) with Pdn resistor SWD (Serial Wire Debug) data input or output
66	M0_SWCK	I/O	Input	Debugger port (for Cortex−M0+) with Pdn resistor SWD (Serial Wire Debug) clock input
67	GP04_2	I/O	Input (L)	General purpose I/O port with Pdn resistor
68	GP04_3	I/O	Input (L)	General purpose I/O port with Pdn resistor
69	GP04_4	I/O	Input (L)	General purpose I/O port with Pdn resistor
70	GP04_5	I/O	Input (L)	General purpose I/O port with Pdn resistor
71	GP04_6	I/O	Input (L)	General purpose I/O port with Pdn resistor
72	GP04_7	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ PWM output for timer7 or Capture input
73	GP05_0 / AD0	I/O /AI	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Input0 for Gen−ADC

PIN DESCRIPTION (continued)

Pin No.	Pin Name	I/O	State when "Reset"	Description
74	GP05_1 / AD1	I/O /AI	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Input1 for Gen−ADC
75	GP05_2 / AD2	I/O /AI	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Input2 for Gen−ADC
76	GP05_3 / AD3	I/O /AI	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Input3 for Gen−ADC
77	DVDD12	−	−	Digital system (1.2 V) power supply
78	DVSS	−	−	Digital system / Analog system (Gen−ADC) ground This pin must be connected to 0 V.
79	DVDD	−	−	Digital system (3.3 V) / Analog system (Gen−ADC) power supply
80	GP05_4 / AD4	I/O /AI	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Input4 for Gen−ADC Data output for UART channel−2 (exclusive with GP03_1)
81	GP05_5 / AD5	I/O /AI	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Input5 for Gen−ADC Clock output for serial communication channel−4 (exclusive with GP03_1) Data input for UART channel−2 (exclusive with GP03_2)
82	GP05_6 / AD6	I/O /AI	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Input6 for Gen−ADC Receive data input for serial communication channel−4 (exclusive with GP03_2) Data output for UART channel−3 (exclusive with GP03_4)
83	GP05_7 / AD7	I/O /AI	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M0+ Input7 for Gen−ADC Transmit data output for serial communication channel−4 (exclusive with GP03_3) Data input for UART channel−3 (exclusive with GP03_5)
84	DVDD	−	−	Digital system (3.3 V) and System−PLL power supply
85	DVSS	−	−	Digital system and System−PLL ground. This pin must be connected to 0 V.
86	GP04_0	I/O	Output (L)	General purpose I/O port with Pdn resistor
87	GP04_1	I/O	Input	General purpose Input port *Must be need to connect VDD (3.3 V) through external Pup register.
88	SFLWP1	I/O	Input (H)	Port for Sflash−1 connection (for Cortex−M0+, with Pup or Pdn resistor) Write protect (WP) output (Note 11) or Data input−2 or output−2 (Note 12)
89	SFLDO1	I/O	Input	Port for Sflash−1 connection (for Cortex−M0+, with Pup or Pdn resistor) Data input (Note 11, 13) or Data input−1 or output−1 (Note 12)
90	SFLCS1	I/O	Input	Port for Sflash−1 connection (for Cortex−M0+, with Pup or Pdn resistor) Chip select (CS) output
91	SFLHOLD1	I/O	Input (H)	Port for SFlash−1 connection (for Cortex−M0+, with Pup or Pdn resistor) Hold (HOLD) output (Note 11) or Data input−3 or output−3 (Note 12)
92	SFLCL1	I/O	Input	Port for SFlash−1 connection (for Cortex−M0+, with Pup or Pdn resistor) Clock output
93	SFLDI1	I/O	Input	Port for SFlash−1 connection (for Cortex−M0+, with Pdn resistor) Data output (Note 11, 13) or Data input−0 or output−0 (Note 12)
94	DVDD12	−	−	Digital system (1.2 V) power supply
95	DVSS	−	−	Digital system ground. This pin must be connected to 0 V.
96	DVDD	−	−	Digital system (3.3 V) power supply

PIN DESCRIPTION (continued)

Pin No.	Pin Name	I/O	State when "Reset"	Description
97	SFLWP2	I/O	Input (H)	Port for Sflash−2 connection (for Cortex−M3, with Pup or, Pdn resistor) Write protect (WP) output (Note 11) or Data input−2 or output−2 (Note 12)
98	SFLDO2	I/O	Input	Port for SFlash−2 connection (for Cortex−M3, with Pup or Pdn resistor) Data input (Note 11, 13) or Data input−1 or output−1 (Note 12)
99	SFLCS2	I/O	Input	Port for SFlash−2 connection (for Cortex−M3, with Pup or Pdn resistor) Chip select (CS) output
100	SFLHOLD2	I/O	Input (H)	Port for SFlash−2 connection (for Cortex−M3, with Pup or Pdn resistor) Hold (HOLD) output (Note11) or Data input−3 or output−3 (Note 12)
101	SFLCL2	I/O	Input	Port for SFlash−2 connection (for Cortex−M3, with Pup or Pdn resistor) Clock output
102	SFLDI2	I/O	Input	Port for SFlash−2 connection (for Cortex−M3, with Pup or Pdn resistor) Data output (Note 11, 13) or Data input−0 or output−0 (Note 12)
103	GP07_0	I/O	Output (L)	General purpose I/O port with Pdn resistor clock input or output for audio interface
104	GP07_1	I/O	Output (L)	General purpose I/O port with Pdn resistor Bit clock input or output for audio interface
105	GP07_2	I/O	Output (L)	General purpose I/O port with Pdn resistor Data output−1 (for Front) for audio interface
106	GP07_3	I/O	Output (L)	General purpose I/O port with Pdn resistor Data output−2 (for Rear) for audio interface
107	GP07_4	I/O	Output (L)	General purpose I/O port with Pdn resistor Data output−3 (for Subwoofer) for audio interface
108	GP07_5	I/O	Output (L)	General purpose I/O port with Pdn resistor LR clock input−1 or output−1 for audio interface For Cortex−M3 Transmit data output for serial communication channel−4
109	GP07_6	I/O	Output (L)	General purpose I/O port with Pdn resistor Bit clock input−1 or output−1 for audio interface For Cortex−M3 Transmit data input for serial communication channel−4
110	M3_SWCK	I	Input	Debugger port (for Cortex−M3) with Pdn register SWD (Serial Wire Debug) clock input
111	M3_SWDT	I/O	Output (H)	Debugger port (for Cortex−M3) with Pup register SWD (Serial Wire Debug) data input or output
112	GP07_7	I/O	Output (L)	General purpose I/O port with Pdn resistor Data input1 for audio interface For Cortex−M3 Clock output for serial communication channel−4
113	AFILT2	AO	Unknown	Audio−PLL2 Charge pump output (for filter connection) pin
114	DVDD12	−	−	Digital system (1.2 V) power supply
115	DVSS	−	−	Digital system and Audio−PLL2 ground This pin must be connected to the 0 V.
116	DVDD	−	−	Digital system (3.3 V) and Audio−PLL2 power supply
117	GP08_0	I/O	Input (L)	General purpose I/O port with Pdn resistor Clock output for MEMS microphone connection (exclusive with GP10_0, GP13_4) Reference clock (fs256) input or output for audio Clock input or output for stream data transfer
118	GP08_1	I/O	Input (L)	General purpose I/O port with Pdn resistor Data input for MEMS microphone connection (exclusive with GP10_1, GP13_5) Data input or output for stream data transfer
119	GP08_2	I/O	Input (L)	General purpose I/O port with Pdn resistor

PIN DESCRIPTION (continued)

Pin No.	Pin Name	I/O	State when "Reset"	Description
120	GP08_3	I/O	Input (L)	General purpose I/O port with Pdn resistor Request input or output for stream data transfer
121	GP08_4	I/O	Input (L)	General purpose I/O port with Pdn resistor
122	GP08_5	I/O	Input (L)	General purpose I/O port with Pdn resistor
123	GP08_6	I/O	Input (L)	General purpose I/O port with Pdn resistor
124	GP08_7	I/O	Input (L)	General purpose I/O port with Pdn resistor
125	GP09_0	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M3 Data output for UART channel−1
126	GP09_1	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M3 Data input for UART channel−1
127	DVDD12	−	−	Digital system (1.2 V) power supply
128	UVSS2	−	−	FS−USB ground. This pin must be connected to 0 V.
129	UDM2	I/O	Input	FS−USB D− signal connection
130	UDP2	I/O	Input	FS−USB D+ signal connection
131	UVDD2	I/O	Input (L)	FS−USB power supply
132	XVSS	I/O	Input (L)	Oscillator ground. This pin must be connected to 0 V.
133	X24MOUT	O	Oscillation	X'tal oscillator connection (24.000 MHz)
134	X24MIN	I	Oscillation	X'tal oscillator connection (24.000 MHz)
135	XVDD	−	−	Oscillator (3.3 V) power suplly
136	TEST2	I	Input	Test mode setting pin. This pin must be connected to 0 V.
137	UVDD12	−	−	USB digital system (1.2 V) power supply
138	RBIAS	AI	Input	Resistance connection for internal bias for HS−USB
139	VBUS	AI	Input	VBUS input for HS−USB
140	UVSS1	−	−	HS−USB ground. This pin must be connected to 0 V.
141	ID	AI	Input	D input for HS−USB. This pin must be connected to 0 VI. (Note 14)
142	UVDD1	−	−	HS−USB power supply
143	UDM1	I/O	Input	HS−USB D− signal connection
144	UDP1	I/O	Input	HS−USB D+ signal connection
145	TEST3	I	Input	Test mode setting pin. This pin must be connected to 0 V.
146	GP09_2	I/O	Input (L)	General purpose I/O port with Pdn resistor LR clock input/output for Bluetooth module communication
147	GP09_3	I/O	Input (L)	General purpose I/O port with Pdn resistor Bit clock input/output for Bluetooth module communication
148	GP09_4	I/O	Input (L)	General purpose I/O port with Pdn resistor Data input for Bluetooth module communication
149	GP09_5	I/O	Input (L)	General purpose I/O port with Pdn resistor Data output for Bluetooth module communication
150	GP09_6	I/O	Input (L)	General purpose I/O port with Pdn resistor
151	GP09_7	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M3 External interruption _0 input

PIN DESCRIPTION (continued)

Pin No.	Pin Name	I/O	State when "Reset"	Description
152	AFILT1	AO	Unknown	Audio−PLL1 Charge pump output pin (for filter connection)
153	DVDD12	−	−	Digital system (1.2 V) power supply
154	DVSS	−	−	Digital system ground and Audio−PLL1 ground. This pin must be connected to 0 V.
155	DVDD	−	−	Digital system (3.3 V) and Audio−PLL1 power supply
156	GP10_0	I/O	Input (L)	General purpose I/O port with Pdn resistor Clock output for MEMS microphone connection (exclusive with GP08_0, GP13_4) For Cortex−M3 Data output for UART channel−2
157	GP10_1	I/O	Input (L)	General purpose I/O port with Pdn resistor Data input for MEMS microphone connection (exclusive with GP08_1,GP13_5) For Cortex−M3 Data input for UART channel−2
158	GP10_2	I/O	Input (L)	General purpose I/O port with Pdn resistor LR clock input−4 or output−4 for audio interface Data1 input or output for SDC Data2 input or output for PSRAM (Note 15, 16) For Cortex−M3 Data output for UART channel−3
159	GP10_3	I/O	Input (L)	General purpose I/O port with Pdn resistor Bit clock input or output4 for audio interface Data0 input or output for SDC Data output for PSRAM (Note 15) or Data1 input or output (Note 16) For Cortex−M3 Data input for UART channel−3
160	GP10_4	I/O	Input (L)	General purpose I/O port with Pdn resistor Data input4 for audio interface Clock output for SDC Chip enable (CE) output for PSRAM JTAG clock input for LPDSP debugger (exclusive with GP12_2)
161	GP10_5	I/O	Input (L)	General purpose I/O port with Pdn resistor LR clock input or output−5 for for audio interface Command output for SDC Data3 input or output for PSRAM (Note 15, 16) For Cortex−M3 Clock output for I^2C channel−2 (exclusive with GP13_4) Clock output for serial communication channel−2 (exclusive with GP13_4) JTAG mode input for LPDSP debugger (exclusive with GP12_3)
162	GP10_6	I/O	Input (L)	General purpose I/O port with Pdn resistor Bit clock input or output−5 for audio interface Data3 input or output for SDC Clock output for PSRAM For Cortex−M3 Data input or output for I^2C channel−2 (exclusive with GP13_5) Receive data input for serial communication channel−2 (exclusive with GP13_5) JTAG data input for LPDSP debugger (exclusive with GP12_4)
163	GP10_7	I/O	Input (L)	General purpose I/O port with Pdn resistor Data input5 for for audio interface Data2 input/output for SDC Data input for PSRAM (Note 15) or Data0 input or output (Note 16) for Cortex−M3 Transmit data output for serial communication channel−2 (exclusive with GP13_6) JTAG data output for LPDSP debugger (exclusive with GP12_5)
164	GP11_0	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M3 Transmit data output for serial communication channel−5
165	GP11_1	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M3 Receive data input for serial communication channel−5

PIN DESCRIPTION (continued)

Pin No.	Pin Name	I/O	State when "Reset"	Description
166	GP11_2	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M3 Transmit data output for serial communication channel−5
167	GP11_3	I/O	Input (L)	General purpose I/O port with Pdn resistor
168	GP11_4	I/O	Input (L)	General purpose I/O port with Pdn resistor Clock input for CD sub code data (SBCK)
169	GP11_5	I/O	Input (L)	General purpose I/O port with Pdn resistor Input for CD sub code data (PW)
170	GP11_6	I/O	Input (L)	General purpose I/O port with Pdn resistor Flame synchronization signal (SFSY) input for CD sub code
171	GP11_7	I/O	Input (L)	General purpose I/O port with Pdn resistor Block synchronization signal (SBSY) input for CD sub code
172	DVDD12	−	−	Digital system (1.2 V) power supply
173	DVSS	−	−	Digital system ground. This pin must be connected to 0 V.
174	DVDD	−	−	Digital system (3.3 V) power supply
175	GP12_0	I/O	Input (L)	General purpose I/O port with Pdn resistor Data1 input or output for SDC (exclusive with GP10_2) Data2 input or output for PSRAM (Note 15, 16) (exclusive with GP10_2) For Cortex−M3 External interruption _1 input
176	GP12_1	I/O	Input (L)	General purpose I/O port with Pdn resistor LR clock input−2 or output−2 for audio interface Data0 input or output for SDC (exclusive with GP10_3) Data output for PSRAM (Note 15) or Data1 input or output (Note 16) (exclusive with GP10_3)
177	GP12_2	I/O	Input (L)	General purpose I/O port with Pdn resistor Bit clock input or output−2 for audio interface Clock output for SDC (exclusive with GP10_4) Chip enable (CE) output for PSRAM (exclusive with GP10_4) JTAG clock input for LPDSP debugger (exclusive with GP10_4)
178	GP12_3	I/O	Input (L)	General purpose I/O port with Pdn resistor Data input−2 for audio interface Command output for SDC (exclusive with GP10_5) Data3 output for PSRAM (Note 15, 16) (exclusive with GP10_5) JTAG mode input for LPDSP debugger (exclusive with GP10_5)
179	GP12_4	I/O	Input (L)	General purpose I/O port with Pdn resistor Data input−3 or output−3 for SDC (exclusive with GP10_6) Clock output for PSRAM (exclusive with GP10_6) For Cortex−M3 External interruption _2 input JTAG data input for LPDSP debugger (exclusive with GP10_6)
180	GP12_5	I/O	Input (L)	General purpose I/O port with Pdn resistor Data input−2 or output−2 for SDC (exclusive with GP10_7) Data input for PSRAM (Note 15) or Data0 input or output (Note 16) (exclusive with GP10_7) JTAG data output for LPDSP debugger (exclusive with GP10_7)
181	GP13_0	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M3 Transmit data output for serial communication channel−1
182	GP13_1	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M3 Clock output for I^2C channel−1 Clock output for serial communication channel−1
183	GP13_2	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M3 Data input or output for I^2C channel−1 Data input for serial communication channel−1

PIN DESCRIPTION (continued)

Pin No.	Pin Name	I/O	State when "Reset"	Description
184	GP13_3	I/O	Input (L)	General purpose I/O port with Pdn resistor LR clock input−3 or output−3 for audio interface For Cortex−M3 Transmit data output for serial communication channel−2 (exclusive with GP10_7)
185	GP13_4	I/O	Input (L)	General purpose I/O port with Pdn resistor Bit clock input−3 or output−3 for audio interface Clock output for MEMS microphone connection (exclusive with GP08_0, GP10_0) For Cortex−M3 Clock output for I^2C channel−2 (exclusive with GP10_5) Clock output for serial communication channel−2 (exclusive with GP10_5)
186	GP13_5	I/O	Input (L)	General purpose I/O port with Pdn resistor Data input−3 for audio interface Data input for MEMS microphone connection (exclusive with GP08_1, GP10_1) For Cortex−M3 Data input/output for I^2C channel−2 (exclusive with GP10_6) Receive data input for serial communication channel−2 (exclusive with GP10_6)
187	GP13_6	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M3 Clock output for I^2C channel−3 Clock output for serial communication channel−3
188	GP13_7	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M3 Data input/output for I^2C channel−3 Data input for serial communication channel−3
189	DVDD12	−	−	Digital system (1.2 V) power supply
190	DVSS	−	−	Digital system ground. This pin must be connected to 0 V.
191	DVDD	−	−	Digital system (3.3 V) power supply
192	GP14_0	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M3 Data output for serial communication channel RTS output for UART (for channel−4), corresponding to CTS and RTS
193	GP14_1	I	Input	General input port For Cortex−M3 CTS input for UART (for channel−4), corresponding to CTS and RTS
194	GP14_2	I	Input	General input port For Cortex−M3 Data input for UART (for channel−4), corresponding to CTS and RTS
195	GP14_3	I/O	Input (L)	General purpose I/O port with Pdn resistor For Cortex−M3 Data output for UART (for channel−4), corresponding to CTS and RTS
196	RESB	I	Input	IC reset input ("L"−active) This pin must be set to low once after power is first applied.
197	L1IN	AI	Input	Analog stereo Left channel Single Ended input
198	R1IN	AI	Input	Analog stereo Right channel Single Ended input
199	L2IN	AI	Input	Analog stereo Left channel Single Ended input
200	R2IN	AI	Input	Analog stereo Right channel Single Ended input
201	L3INP	AI	Input	Analog stereo Left channel Differential input (Positive) or Single ended input
202	L3INN	AI	Input	Analog stereo Left channel Differential input (Negative) (Note 17)
203	R3INP	AI	Input	Analog stereo Right channel Differential input (Positive) or Single ended input
204	R3INN	AI	Input	Analog stereo Right channel Differential input (Negative) (Note 17)
205	L4INP	AI	Input	Analog stereo Left channel Differential input (Positive) or Single ended input
206	L4INN	AI	Input	Analog stereo Left channel Differential input (Negative) (Note 17)

PIN DESCRIPTION (continued)

Pin No.	Pin Name	I/O	State when "Reset"	Description
207	R4INP	AI	Input	Analog stereo Right channel Differential input (Positive) or Single ended input
208	R4INN	AI	Input	Analog stereo Right channel Differential input (Negative) (Note 17)

10. Pin is N channel open drain when I^2C function is selected.
11. SFlash operational mode: at Standard−SPI
12. SFlash operational mode: at Quad−I/O
13. Regarding the notation of SFlash data connection pin, SFlash side is the reference.
14. Necessary of host setting as a default for this product HS−USB
    At system startup, 5 V must be supplied to the VBUS pin, and 0 V supplied to the ID pin.
15. PSRAM operational mode : SPI Mode and Parallel Mode
    Pull−down processing is recommended, since data−2 and data−3 are unused.
16. PSRAM operational mode : QPI Mode
17. Must be connected to ground (GND) via the coupling capacitor when used as a single−ended input.

NOTES:

(10) For unused pins:
- The unused input pins must be connected to the GND (0 V) level if there is no individual note in the above table.
- The unused output pins must be left open (No connection) if there is no individual note in the above table.
- The unused input/output pins must follow the below conditions if there is no individual note in the above table:

  Input pins
  Must be left open with internal Pup/Pdn register ON.
  When running with internal Pup/Pdn resistor OFF, connect to GND (0 V) or connect to power pins for I/O.
  However, use of individual Pup/Pdn resistor is recommended as a fail−safe measure.

  Output pins
  Must be left open.

(11) For power supply pins:
Same voltage level must be supplied to DVDD, AVDD1, AVDD2, AVDD3, AVDD4, AVDD5, UVDD1, UVDD2, and XVDD power supply pins.
And same voltage level must be supplied to DVDD12, UVDD12, and XVDD12.
(Refer to "Allowable operating ranges")

(12) For unused "Analog Source" pins:
The unused "Analog Source" pins (No.3, 4, and 197 to 208) must be connected to GND (0 V) through the coupling capacitor

(13) For Sflash CS pins
The CS pins (No.90 and 99) for Sflash are at Hi impedance (Hi−z) when the RESB pin is set to "Low". Therefore, comply with the specifications of the Sflash being used, such as inserting a pull−up resistor on the substrate if necessary.

SYSTEM−MCU (CORTEX−M0+) MEMORY MAP AND BUS CONFIGURATION

Figure 3 shows the memory map for the System−MCU (Cortex−M0+).

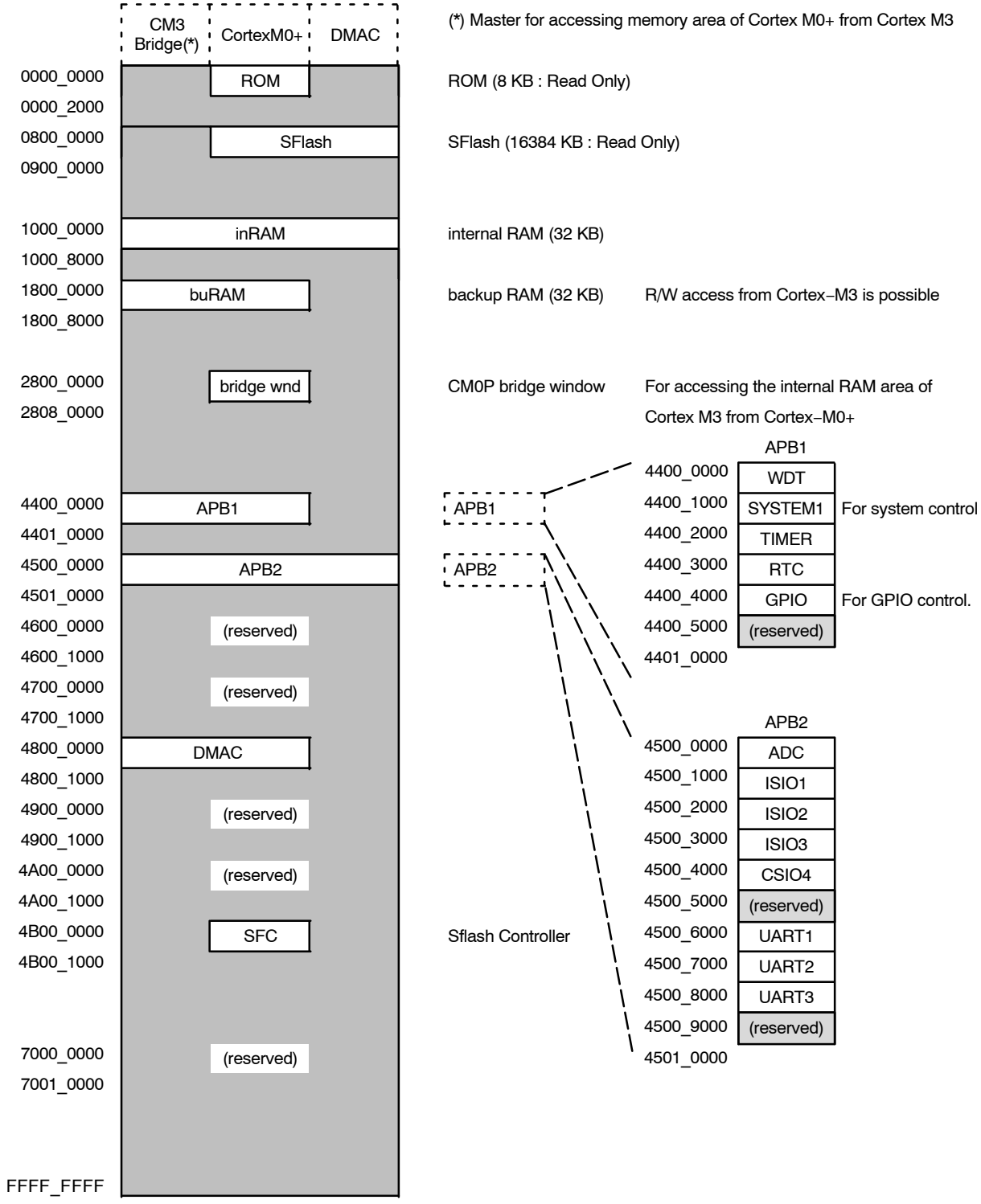


Figure 3. System−MCU Memory Map

AUDIO−MCU (CORTEX−3) MEMORY MAP AND BUS CONFIGURATION

Figure 4 shows the memory map for the Audio−MCU (Cortex−M3).

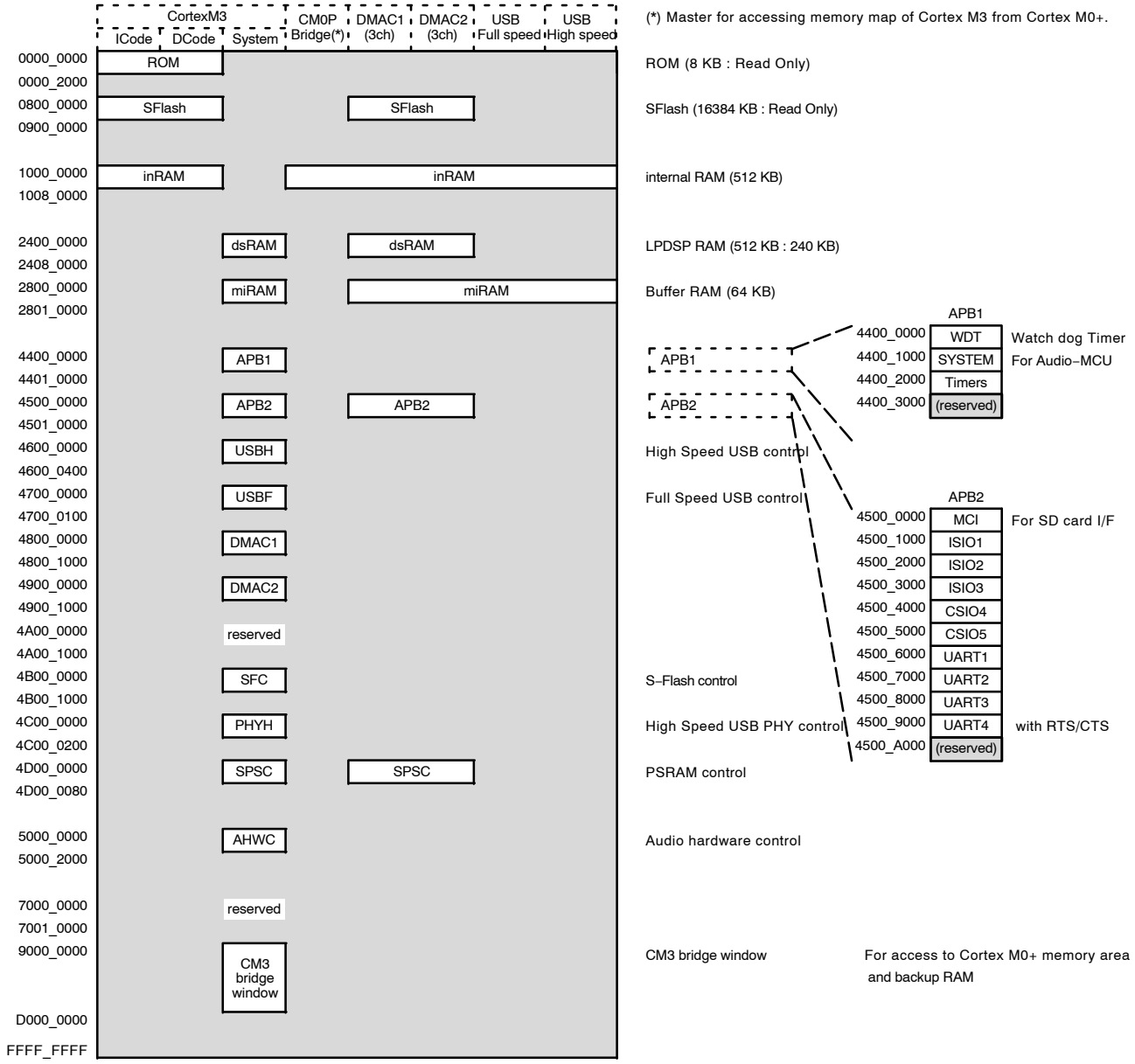


Figure 4. Audio−MCU Memory Map

CLOCK SYSTEM DIAGRAM

Figure 5 shows the clock system diagram of the LC786830.

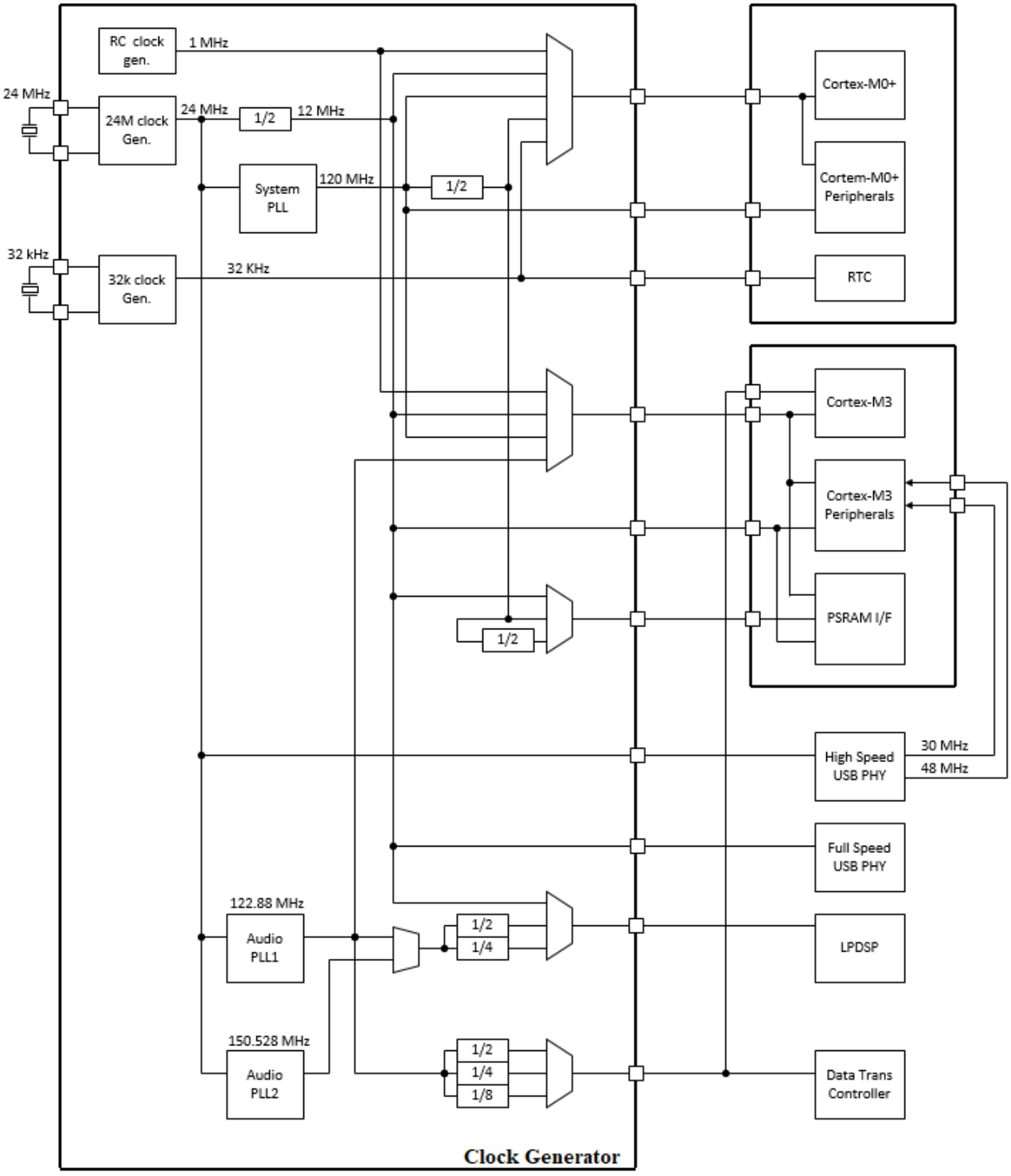


Figure 5. Clock System Diagram

POWER−ON AND RESET CONTROL

This SoC must always be reset when the power is turned on (Input “L” to RESB pin).

The power supply pin has a Power−On Control Function, so no issues will occur even when either VDD or VDD12 starts first.

The release of the power−on reset signal to the RESB pin must be performed after a predetermined time has elapsed following both VDD and VDD12 coming within their allowable operating range.

Follow the sequence below.

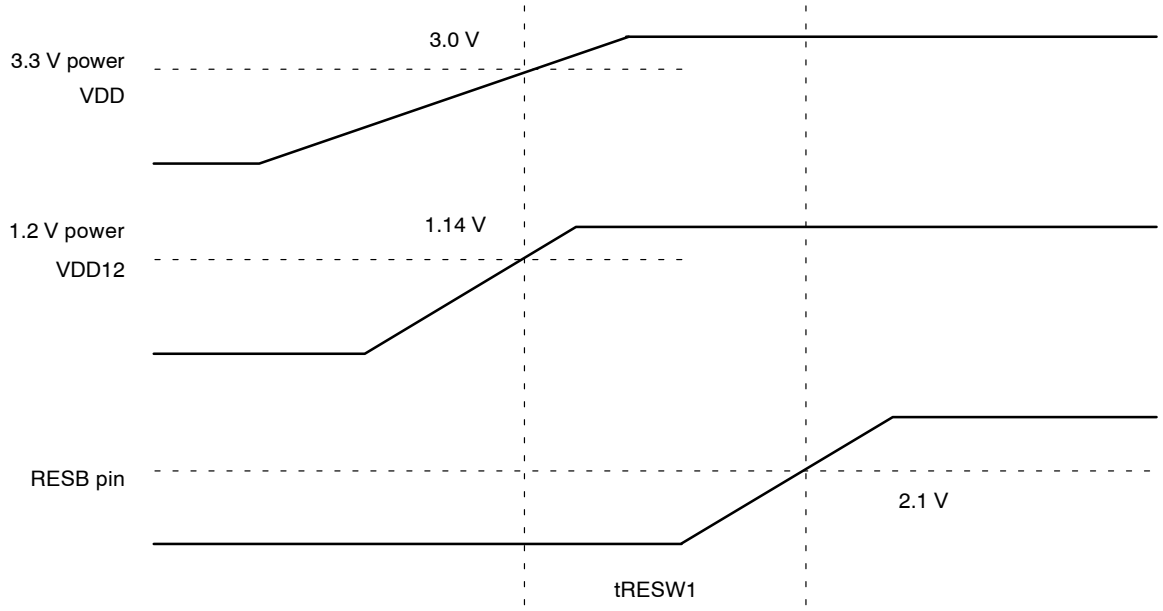


Figure 6. Power−ON and Reset Control Timing Diagram

Table 1.

Symbol	Parameter	Min	Typ	Max	Unit
tRESW1	Reset Period (RESB Pin = “L”)	200	−	−	μs

18. Even when resetting this SoC during operation, the reset period is as “tRESW1” above.

This SoC removes chattering for reset signals inputted into the RESB pins by the RC oscillator clock inside the SoC.

Since the RC oscillator circuit starts with 1.2 V (VDD12), the above tRESW1 period is required for initializing the SoC with consideration of the stabilizing time of RC oscillator circuit after VDD12 enters into an allowable operational range.

This SoC does not have power on reset (POR) and low voltage detection reset (LVD) functions.

Therefore, when the voltage value is out of the allowable operating range at power on or during operation, the SoC must be reset by setting the RESB pin to “L”.

In this case, be sure to input a reset signal to satisfy the above reset period.

SERIAL INTERFACE

This SoC has SIO interface and IIC interface as serial communication interfaces with external devices.

In both cases, this SoC functions as a master.

The SIO interface has 4 systems for Cortex−M0+ and 5 systems for Cortex−M3.

IIC interface has three systems for Cortex−M0+ and three systems for Cortex−M3.

And some SIO or IIC terminals are assigned to the same terminal and are used exclusively.

- Serial interface (SIO) master mode port

Table 2.

	SIO Number	SIO Clock (Output)	SIO Data (Input)	SIO Data (Output)
For Cortex−M0+	SIO1	GP01_0	GP01_1	GP01_2
	SIO2	GP02_4	GP02_5	GP02_3
	SIO3	GP03_4	GP03_5	GP03_6
	SIO4	GP03_1 or GP05_5	GP03_2 or GP05_6	GP03_3 or GP05_7
For Cortex−M3	SIO1	GP13_1	GP13_2	GP13_0
	SIO2	GP10_5 or GP13_4	GP10_6 or GP13_5	GP10_7 or GP13_3
	SIO3	GP13_6	GP13_7	GP14_0
	SIO4	M3_SWCK (Note 19)	GP07_6	GP07_5
	SIO5	GP11_2	GP11_1	GP11_0

19. Only when the Cortex−M3 debugger is not used

- Serial interface (SIO) master mode timing − AC characteristics

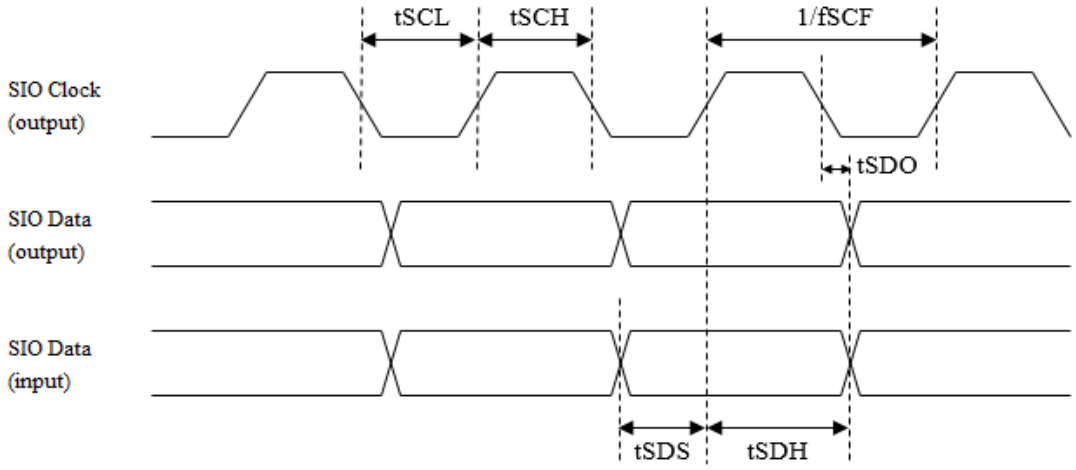


Figure 7. Serial Interface (SIO) Master Mode Input or Output Timing Chart

Table 3. Ta = −40 to 85°C, V_{DD} = 3.0 to 3.6 V, V_{DD}12 = 1.14 to 1.26 V, V_{SS} = 0 V

Symbol	Parameter	Signal Name	Min	Typ	Max	Unit
fSCF	SIO Clock Frequency	SIO Clock	0.016	−	3.0	MHz
tSCH	SIO Clock “H” Period	SIO Clock	150	−	31250	ns
tSCL	SIO Clock “L” Period	SIO Clock	150	−	31250	ns
tSDO	Data output Settle Time	SIO DATA (output) / Clock	−	−	4T+20	ns
tSDS	Data Input Setup Time	SIO DATA (input) / Clock	100	−	−	ns
tSDH	Data Input Hold Time	SIO DATA (input) / Clock	4T	−	−	ns

20. T: System clock cycle for each SIO interface module.

- Serial interface (IIC) master mode port

Table 4.

	IIC Number	IIC Clock (Output)	IIC Data (In/Out)
For Cortex−M0+	IICM1	GP01_0	GP01_1
	IICM2	GP02_4	GP02_5
	IICM3	GP03_4	GP03_5
For Cortex−M3	IICM1	GP13_1	GP13_2
	IICM2	GP10_5 or GP13_4	GP10_6 or GP13_5
	IICM3	GP13_6	GP13_7

- Serial interface (IIC) master mode timing − AC characteristics

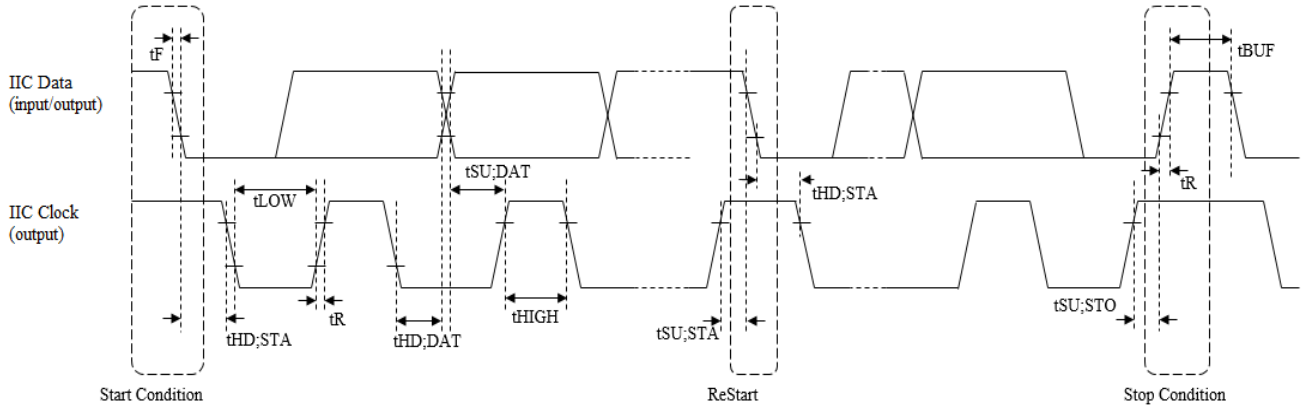


Figure 8. Serial Interface (IIC) Master Mode Input or Output Timing Chart

Table 5. Ta = −40 to 85°C, V_{DD} = 3.0 to 3.6 V, V_{DD}12 = 1.14 to 1.26 V, V_{SS} = 0 V

Symbol	Parameter	Normal (100 kbps)		High Speed (400 kbps)		Unit
		Min	Max	Min	Max	
fSCL	SCL Frequency	0	100	0	400	kHz
tBUF	Bus Open Time	4.7	−	1.3	−	μs
tLOW	SCL “L” Period	4.7	−	1.3	−	μs
tHIGH	SCL “H” Period	4.0	−	0.6	−	μs
tHD;STA	Start/Restart Condition Hold Time	4.0	−	0.6	−	μs
tSU;STA	Start/Restart Condition Setup Time	4.7	−	0.6	−	μs
tHD;DAT	SDA Hold Time	0	−	0	−	μs
tSU;DAT	SDA Setup Time	250	−	100	−	ns
tR	SDC and SCL Rise Time	−	1000	20+0.1Cb	300	ns
tF	SDA and SCL Fall Time	−	300	20+0.1Cb	300	ns
tSU;STO	Stop Condition Setup Time	4.0	−	0.6	−	μs

21. Cb is the total capacity added to each bus (Unit: pF)

UART INTERFACE

This SoC can perform data transfer functions with external devices via the UART interface.

There is a 3 ch UART interface for Cortex−M0+ and a 4 ch UART interface for Cortex−M3.

- UART interface port

Table 6.

Port Function	UART Interface for Cortex−M0+			UART Interface for Cortex−M3			
	UART1	UART2	UART3	UART1	UART2	UART3	HS−UART
TXD	GP02_6	GP03_1 or GP05_4	GP03_4 or GP05_6	GP09_0	GP10_0	GP10_2	GP14_3
RXD	GP02_7	GP03_2 or GP05_5	GP03_5 or GP05_7	GP09_1	GP10_1	GP10_3	GP14_2
RTS	−	−	−	−	−	−	GP14_0
CTS	−	−	−	−	−	−	GP14_1

22. UART−1, 2 and 3 for Cortex−M0+ and UART1, 2 and 3 for Cortex−M3 are separate.
For example, UART1 I/F for Cortex−M0+ and UART1 I/F for Cortex−M3 can be used at the same time.

Table 7. Ta = −40 to 85°C, V_{DD} = 3.0 to 3.6 V, V_{DD}12 = 1.14 to 1.26 V, V_{SS} = 0 V

Symbol	Parameter	Port	Min	Typ	Max	Unit
UBR	Transfer Rate	TXD and RXD port of UART1 or 2 or 3 for Cortex−M0+	12 / 65536	−	12 / 16	MHz
		TXD and RXD port of UART1 or 2 or 3 for Cortex−M3	12 / 65536	−	12 / 16	MHz
		TXD, RXD, RTS and CTS port of HS−UART for Cortex−M3	49.152 / 268435456	−	49.152 / 16	MHz

- Data length: 7 or 8 bits
- Stop bit length: 1 or 2 bits
- Parity bit: odd or even

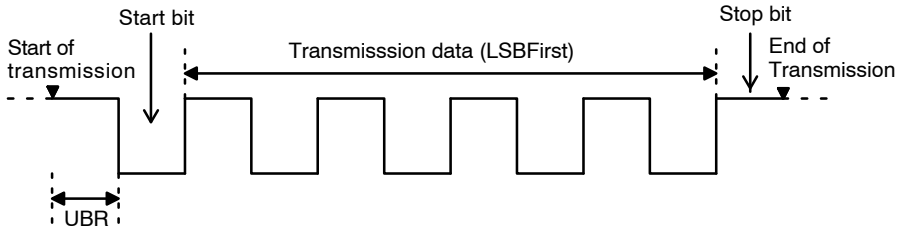


Figure 9. Continuous 8−bit Data Transmission Mode Example (Output Data: 0x55)

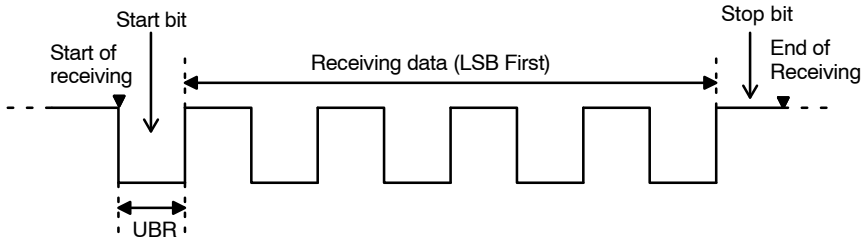


Figure 10. Continuous 8−bit Data Reception Mode Example (Output Data: 0x55)

- CTS and RTS signals of the HS−UART interface t – AC characteristics

The timing of the CTS and RTS signals of the HS−UART are explained here.

CTS Timing Chart

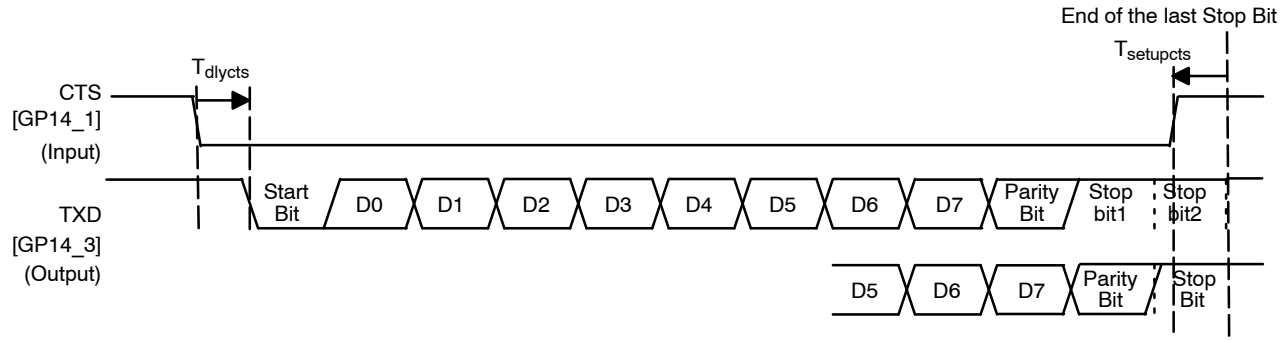


Figure 11. CTS Timing Chart

Table 8. Ta = −40 to 85°C, V_{DD} = 3.0 to 3.6 V, V_{DD}12 = 1.14 to 1.26 V, V_{SS} = 0 V, External Load: 50 pF

Symbol	Parameter	Condition	Signal Name	Min	Typ	Max	Unit
Tdlycts	Delay Time	– Completing preparation to transmit the current TXD data by setting registers at CTS1 = high. – From the negative edge	TXD	–	–	3T+30	ns
Tsetupcts	CTS Setup Time (Not to Transmit the Next TXD Data)	– From end of the last Stop Bit	CTS	3T+30	–	–	ns

23. T: UART functional clock rate.
24. In using hardware flow control by CTS and RTS, if the CTS setup time above is NOT met, the next TXD data will be transmitted at the time of having prepared it regardless of the CTS level.

RTS Timing Chart

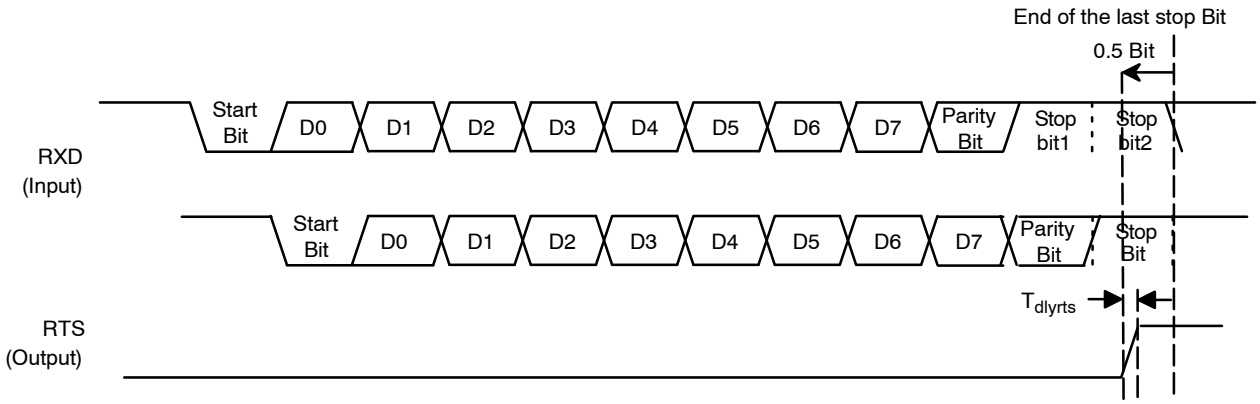


Figure 12. RTS Timing Chart

Table 9. Ta = −40 to 85°C, V_{DD} = 3.0 to 3.6 V, V_{DD}12 = 1.14 to 1.26 V, V_{SS} = 0 V, External Load: 50 pF

Symbol	Parameter	Condition	Signal Name	Min	Typ	Max	Unit
Tdlyrts	Delay Time	From 0.5 bit before of end of the last stop Bit	RTS	–	–	4T+30	ns

25. T: UART functional clock rate

SERIAL FLASH INTERFACE

This SoC has an external serial flash interface on both the Cortex−M0+ and Cortex−M3 processors.

Table 10.

Port Function						
DSP	**SFLCL (Output)**	**SFLCSB (Output)**	**SFLDI or SFLD [0]**	**SFLDO or SFLD [1]**	**SFLWPB or SFLD [2]**	**SFLHOLDB or SFLD [3]**
For Cortex−M0+	SFLCL1	SFLCS1	SFLDI1	SFLDO1	SFLWP1	SFLHOLD1
For Cortex−M3	SFLCL2	SFLCS2	SFLDI2	SFLDO2	SFLWP2	SFLHOLD2

26. Port function: Upper − Serial interface select, lower − Quad interface select.

- Serial flash input or output timing − AC characteristics

Serial Interface Selected:

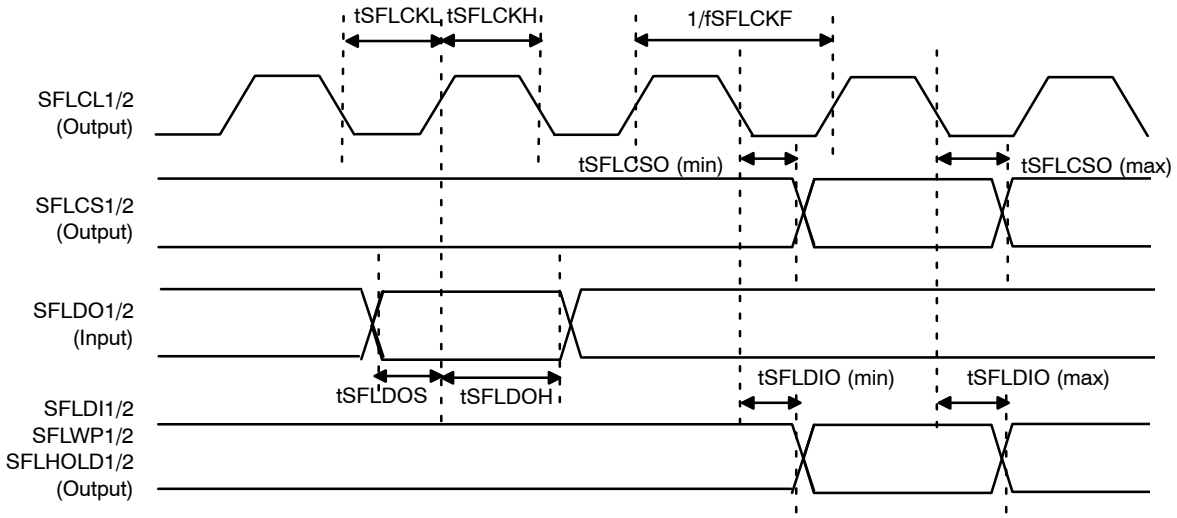
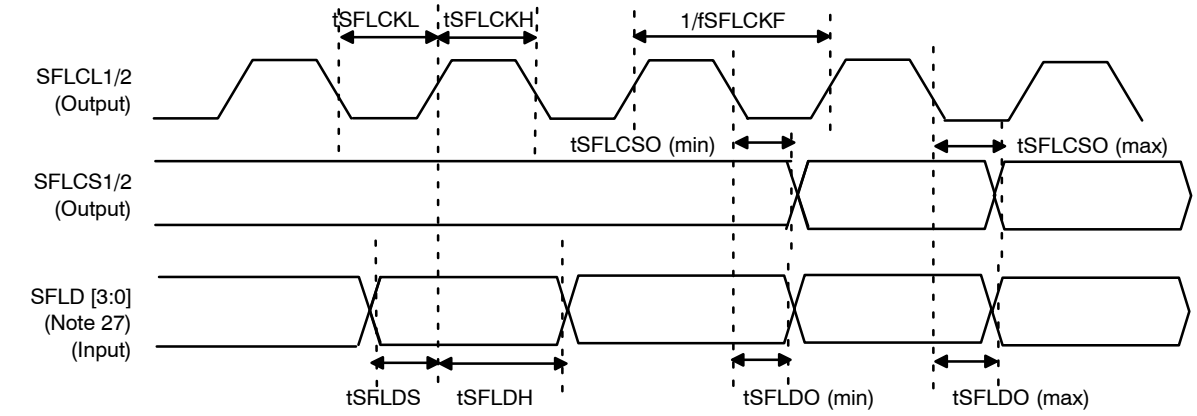


Figure 13. Serial Flash Timing Chart – Serial Interface Selected

Quad Interface Selected:



NOTE:
27. Fsys System clock frequency of Cortex−M0+ or Cortex−M3 (Cortex−M0+: 60 MHz, Cortex−M3: 120 MHz)

Figure 14. Serial Flash Timing Chart – Quad Interface Selected

Table 11. Ta = −40 to 85°C, V_{DD} = 3.0 to 3.6 V, V_{DD}12 = 1.14 to 1.26 V, V_{SS} = 0 V, External Load: 30 pF

Symbol	Parameter	Signal Name	Min	Typ	Max	Unit
fSFLCKF	SFLCL Clock Frequency	SFLCL1/2	–	–	Fsys/2 (Note 28)	MHz
tSFLCKL	SFLCL “L” Period	SFLCL1/2	Tsys−2 (Note 29)	–	Tsys/2+2 (Note 29)	ns
tSFLCKH	SFLCL “H” Period	SFLCL1/2	Tsys−2 (Note 29)	–	Tsys/2+2 (Note 29)	
tSFLCSO	Chip Select Output Delay Time	SELFCS1/2	0	–	2	
tSFLDOS	Data Input Setup Time (Serial Interface Selected)	SELFDO1/2	0	–	–	
tSFLDOH	Data Input Hold Time (Serial Interface Selected)	SELFDO1/2	tSFLCKH+1	–	–	
tSFLDIO	Data output Settle Time (Serial Interface Selected)	(Note 30)	0	–	2	
tSFLDS	Data Input Setup Time (Quad Interface Selected)	(Note 31)	0	–	–	
tSFLDH	Data Input Hold Time (Quad Interface Selected)		tSFLCKH+1	–	–	
tSFLDO	Data Output Settle Time (Quad Interface Selected)		0	–	2	

28. Fsys System clock frequency of Cortex−M0+ or Cortex−M3 (Cortex−M0+: 60 MHz, Cortex−M3: 120 MHz)
29. Tsys System clock rate of Cortex−M0+ or Cortex−M3 (Cortex−M0+: 16.7 ns, Cortex−M3: 8.33 ns)
30. SFLDI1/2, SFLWP1/2, SFLHOLD1/2
31. SFLDI1/2, SFLWP1/2, SFLHOLD1/2, SFLDO1/2

SD CARD INTERFACE

This SoC has one SD card interface.
The only supported mode is Default Speed Mode.

- SD card interface port

Table 12.

DSP	Port Function	Port Function Assignment No.1 (Note 33)	Port Function Assignment No.2 (Note 33)
For Cortex−M0+ (Note 32)	−	−	−
For Cortex−M3	SDC CLK	GP10_4	GP12_2
	SDC CMD	GP10_5	GP12_3
	SDC DT3	GP10_6	GP12_4
	SDC DT2	GP10_7	GP12_5
	SDC DT1	GP10_2	GP12_0
	SDC DT0	GP10_3	GP12_1

32. Cortex−M0+ is not able to control SD card interface.
33. Only one SD memory card interface is installed. You may only use one set of pin function assignments − select option No. 1 or option No. 2. Mixing of the two assignment options is prohibited.

- SD card interface timing − AC characteristics

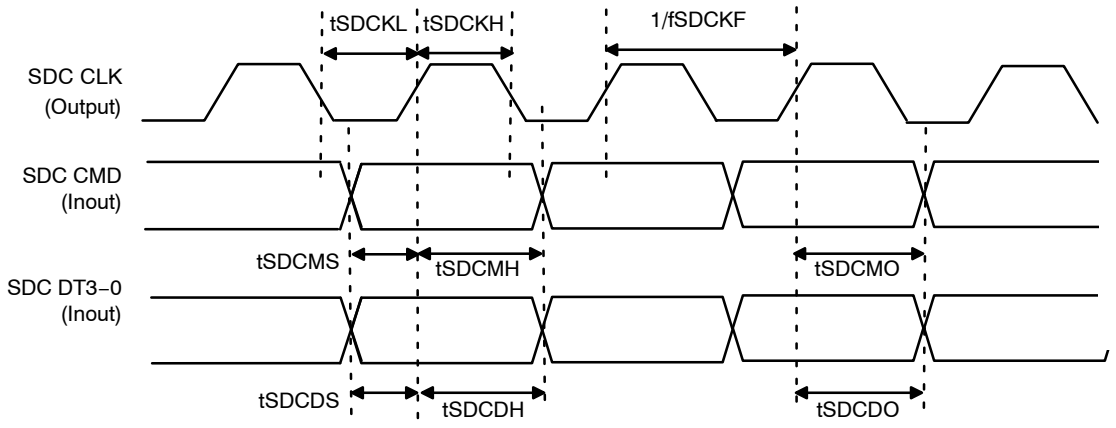


Figure 15. SD Card Interface Timing

Table 13. Ta = −40 to 85°C, V_{DD} = 3.0 to 3.6 V, V_{DD}12 = 1.14 to 1.26 V, V_{SS} = 0 V

Symbol	Parameter	Port	Min	Typ	Max	Unit
fSDCKF	SDC CLK Clock Frequency	SDC CLK	−	12	−	MHz
tSDCKH	SDC CLK "H" Period		−	83.3	−	ns
tSDCKL	SDC CLK "L" Period		−	83.3	−	
tSDCMS	Command Input Setup Time	SDC CLK SDC CMD	6	−	−	
tSDCMH	Command Input Hold Time		6	−	−	
tSDCMO	Command Output Settle Time		0	−	14	
tSDCDS	Data Input Setup Time	SDC CLK SDC DT0, 1, 2 and 3	6	−	−	
tSDCDH	Data Input Hold Time		6	−	−	
tSDCDO	Data Output Settle Time		0	−	14	

DIGITAL AUDIO DATA INPUT AND OUTPUT INTERFACE

This SoC implements 5 IIS interfaces as digital audio inputs, and 1 IIS interface as a digital audio output that can output 3 ch Stereo simultaneously. There is 1 PCM interface implemented as a digital audio input and output.

- Digital audio input and output interface supported format

Table 14.

In, Out	Master, Slave	Mode	Data Length	Slot Length	**256 fs Clock** (Note 34)
Input	Master or Slave	IIS, Left Justified, Right Justified, Long Flame (Note 35), Short Flame (Note 35)	16 bits or 24 bits	32 fs, 48 fs (Note 36) or 64 fs	Internal clock output or External clock input
Output	Master or Slave	IIS, Left Justified, Right Justified	16 bits or 24 bits	32 fs or 64 fs	Internal clock output

34. This SoC generates two audio input 256 fs clocks and one audio output 256 fs clock internally.
GP08_0 can output by selecting one of those clocks.
Only the 256 fs clock for audio output can be output from any terminal from GP07 to GP13.
35. Long Frame or Short Frame format can be supported only by PCM interface.
36. When the IIS Master Input is selected, 48 fs can't be selected as the slot length.

- IIS format port
(Supported format: IIS, Left Justified or Right Justified)

Table 15.

In/Out	LRCK	BCK	DATA	**256 fs Clock** (Note 37)
Input (Note 38)	GP07_5, GP10_2, GP10_5, GP12_1, GP13_3	GP07_6, GP10_3, GP10_6, GP12_2, GP13_4	GP07_7 or M3_SWCK, GP10_4, GP10_7, GP12_3, GP13_5	GP08_0
Output	GP07_0	GP07_1	GP07_2 (Front LR), GP07_3 (Rear LR), GP07_4 (Subwoofer LR),	GP08_0 or Any port from GP07 to GP13

37. This SoC generates two audio input 256 fs clocks and one audio output 256 fs clock internally.
GP08_0 can output by selecting one of those clocks.
Only the 256 fs clock for audio output can be output from any terminal from GP07 to GP13.
38. The digital audio input can input 5 different digital audio signals at the same time.
In addition to them, it is possible to select up to two audio input signals from 7 systems including analog audio input and digital microphone input at the same time.

- PCM interface port
(Supported format: IIS, Left Justified, Right Justified, Long Flame or Short Flame)

Table 16.

PCM LRCK	PCM BCK	PCM DATA (In)	PCM DATA (Out)
GP09_2	GP09_3	GP09_4 (in)	GP09_5 (out)

- Others
  - Analog audio input (ADC) can support Fs from 8 kHz to 48 kHz.
  - Digital microphone input can support Fs from 8 kHz to 48 kHz.
  - Digital audio input (IIS Input) is compatible with Fs from 8 kHz to 192 kHz.
  - The analog audio output (DAC) can support Fs from 8 kHz to 96 kHz.
  - The digital audio output (IIS Output) is compatible with Fs from 8 kHz to 192 kHz.
  - The PCM interface only supports 8 kHz, 16 kHz, 11.025 kHz, 22.05 kHz or 44.1 kHz

Sampling rate conversion may not be supported depending on the combination of input/output Fs in each of the main data SRC and sub data SRC. See Figure 16 and Figure 17.

Output \ Input		Input Fs (kHz)														
		192	176.4	128	96	88.2	64	48	44.1	32	24	22.05	16	12	11.025	8
Output Fs (kHz)	192	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	176.4	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	128	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	96	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	88.2	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	64	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	48	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	44.1	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	32	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
	24			○	○	○	○	○	○	○	○	○	○	○	○	○
	22.05			○	○	○	○	○	○	○	○	○	○	○	○	○
	16				○	○	○	○	○	○	○	○	○	○	○	○
	12						○	○	○	○	○	○	○	○	○	○
	11.025						○	○	○	○	○	○	○	○	○	○
	8							○	○	○	○	○	○	○	○	○

NOTE:
'o': Sampling rate conversion is possible.
Example 1: If the input Fs is 192 kHz, the output Fs can correspond to 32 kHz to 192 kHz. Not available below 24 kHz.
Example 2: When the input Fs is 44.1 kHz, the output Fs can support all 8 kHz to 192 kHz.

Figure 16. SRC for Main Data – Input Fs and Output Fs Combination Table

Output \ Input		Input Fs (kHz)														
		192	176.4	128	96	88.2	64	48	44.1	32	24	22.05	16	12	11.025	8
Output Fs (kHz)	192	*	*	*	*	*	*	*	*	*	*	*	*			
	176.4	*	*	*	*	*	*	*	*	*	*	*	*			
	128	*	*	*	*	*	*	*	*	*	*	*	*			
	96	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
	88.2	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
	64	*	*	○	○	○	○	○	○	○	○	○	○	*	*	*
	48	*	*	○	○	○	○	○	○	○	○	○	○	*	*	*
	44.1	*	*	○	○	○	○	○	○	○	○	○	○	*	*	*
	32	*	*	*	*	○	○	○	○	○	○	○	○	*	*	*
	24	*	*	*	*	*	○	○	○	○	○	○	○	*	*	*
	22.05	*	*	*	*	*	○	○	○	○	○	○	○	*	*	*
	16				*	*	*	*	○	○	○	○	○	*	*	*
	12						*	*	*	*	*	*	*	*	*	*
	11.025						*	*	*	*	*	*	*	*	*	*
	8							*	*	*	*	*	*	*	*	*

NOTE:
'o': Sampling rate conversion is possible.
'*': Sampling rate conversion is possible, but some restriction of sub data SRC control parameters is required.

Figure 17. SRC for Sub Data – Input Fs and Output Fs Combination Table

- Digital audio format timing chart

1. IIS format
   The IIS format can transfer L ch and R ch data within the sampling period. Data transfer is synchronized with the falling edge of BCK signal. The beginning of the L ch and R ch data is 1 cycle after the BCK signal from the falling edge or rising edge of the LRCK signal. The data format is fixed to MSB first.

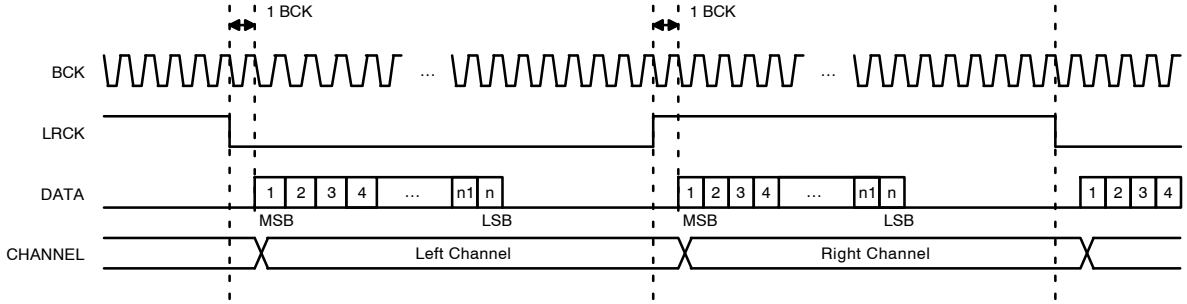


Figure 18. IIS Format Timing Chart

2. Left Justified format
   In the Left Justified format, the leading edge of the L ch data slot is the leading edge of the LRCK signal, and the leading edge of the R ch data slot is the trailing edge of the LRCK signal. If the data length is shorter than the slot length, add “0” after the data (see Figure 19). The polarity of the transfer clock (BCK) can be selected. The data format is fixed to MSB first.

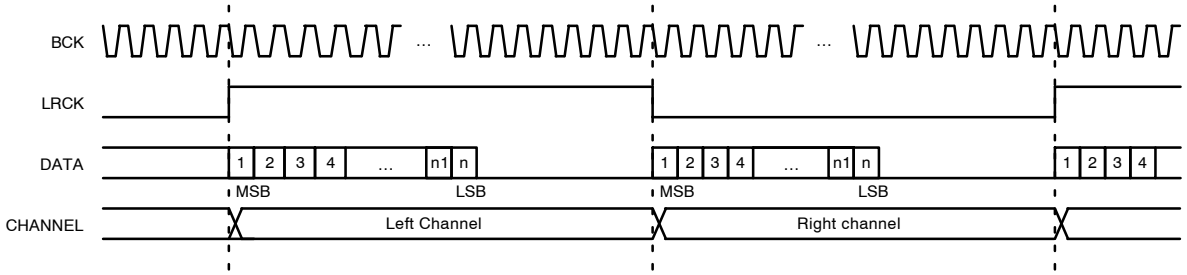


Figure 19. Left Justified Format Timing Chart

3. Right justified format
   In the Right Justified format, the rising edge of the LRCK signal becomes the beginning of the L ch data slot, and the falling edge of the LRCK signal becomes the beginning of the R ch data slot. If the data length is shorter than the slot length, add “0” before the data (see Figure 20). The polarity of the transfer clock (BCK) can be selected. The data format is fixed to MSB first.

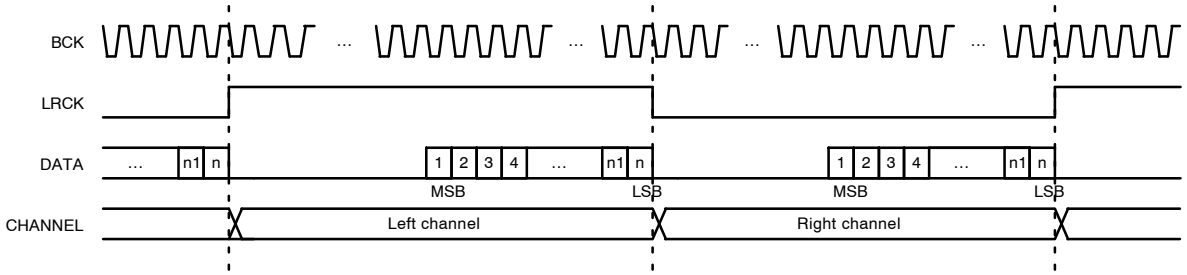


Figure 20. Right Justified Format Timing Chart

4. Long frame format
   In the Long frame format, it is possible to transfer monaural data with a data length of 16 bits. In the Long frame format, the rising edge of the LRCK signal is the head of serial PCM data. The polarity of the transfer clock (BCK) can be selected. The data format is MSB first. The pulse width of the LRCK signal can be selected within the range of BCK 2 to 16 cycles. This format can only be used with PCM interface.

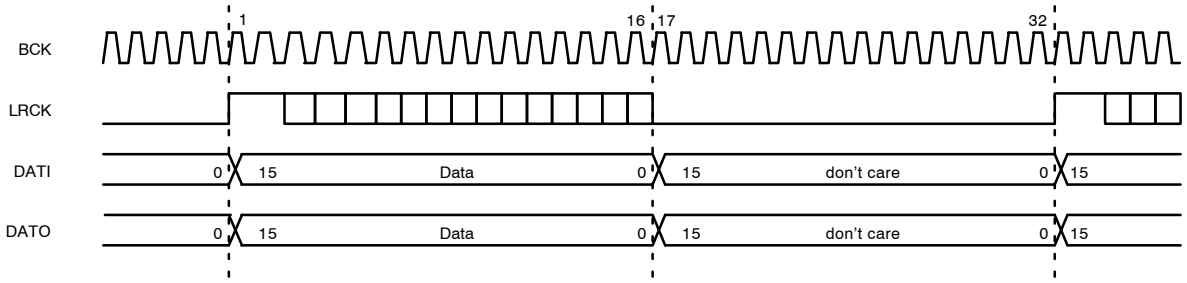


Figure 21. Long Frame Format Timing Chart

5. Short frame format
   The Short frame format can transfer monaural data with a data length of 16 bits. In the Short frame format, the falling edge of the LRCK signal is the head of serial PCM data. The polarity of the transfer clock (BCK) can be selected. The data format is MSB first. The pulse width of the LRCK signal is fixed to BCK 1 cycle. This format can only be used with PCM I/F.
   PCM I/Fでのみ対応可能

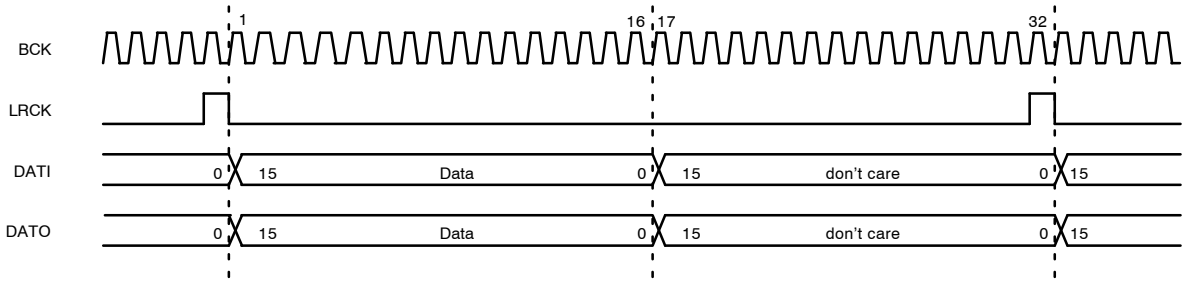


Figure 22. Short Frame Format Timing Chart

- Digital audio data input timing − AC characteristics

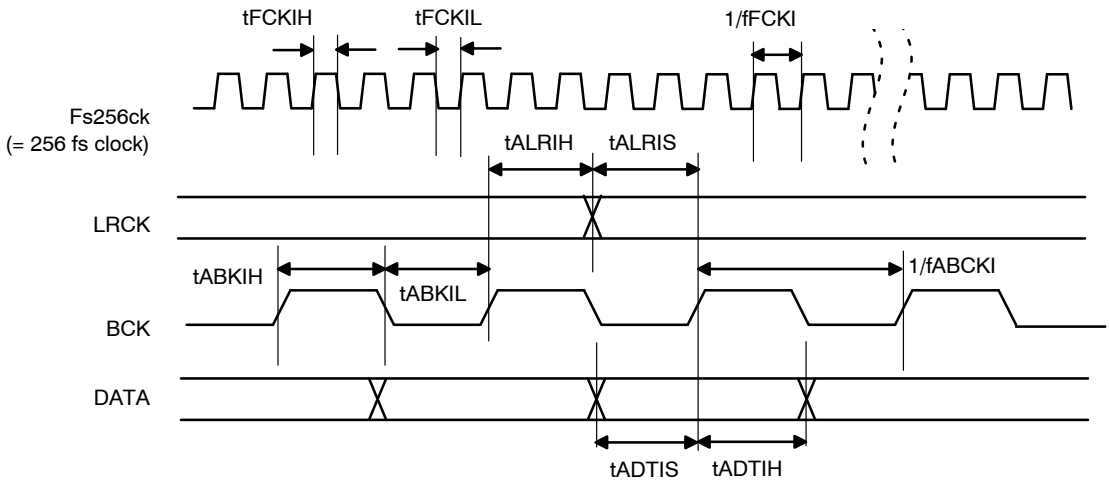


Figure 23. Digital Audio Data Input Timing Chart

Table 17. Ta = −40 to 85°C, V_{DD} = 3.0 to 3.6 V, V_{DD}12 = 1.14 to 1.26 V, V_{SS} = 0 V

Symbol	Parameter	Signal Name	Min	Typ	Max	Unit
fFCKI	Fs256 Clock Frequency	Fs256ck	2.048	–	49.152	MHz
tFCKIH	Fs256 Clock “H” Period	Fs256ck	10	–	–	ns
tFCKIL	Fs256 Clock “L” Period	Fs256ck	10	–	–	ns
fABCKI	Bit Clock Frequency (Note 39)	BCK	–	12.288	–	MHz
tABKIH	Bit Clock “H” Period (Note 39)	BCK	–	40.69	–	ns
tABKIL	Bit Clock “L” Period (Note 39)	BCK	–	40.69	–	ns
fABCKI	Bit Clock Frequency (Note 40)	BCK	–	6.144	–	MHz
tABKIH	Bit Clock “H” Period (Note 40)	BCK	–	81.38	–	ns
tABKIL	Bit Clock “L” Period (Note 40)	BCK	–	81.38	–	ns
tALRIS	LRCK Input Setup Time	LRCK, BCK	10	–	–	ns
tALRIH	LRCK Input Hold Time	LRCK, BCK	10	–	–	ns
tADTIS	Data Input Setup Time	DATA, BCK	10	–	–	ns
tADTIH	Data Input Hold Time	DATA, BCK	10	–	–	ns

39. When output Fs is set to 192 kHz and output format slot length is set to 64 fs.
40. When output Fs is set to 192 kHz and output format slot length is set to 32 fs.

- Digital audio data output timing − AC characteristics

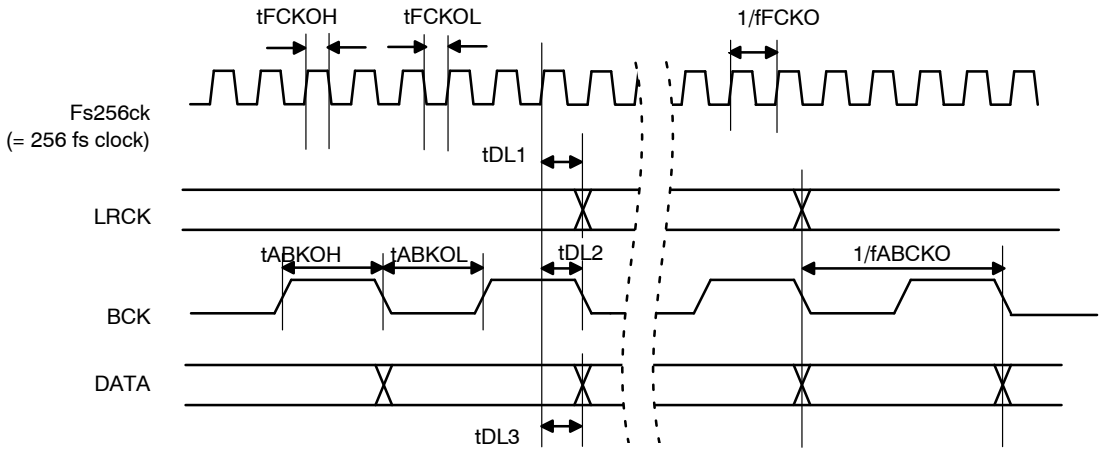


Figure 24. Digital Audio Data Output Timing Chart

Table 18. Ta = −40 to 85°C, V_{DD} = 3.0 to 3.6 V, V_{DD}12 = 1.14 to 1.26 V, V_{SS} = 0 V

Symbol	Parameter	Signal Name	Min	Typ	Max	Unit
fFCKO	Fs256 Clock Frequency	Fs256ck	−	−	49.152 (Note 41)	MHz
tFCKOH	Fs256 Clock “H” Period	Fs256ck	10.17 (Note 41)	−	−	ns
tFCKOL	Fs256 Clock “L” Period	Fs256ck	10.17 (Note 41)	−	−	ns
fABCKO	Bit Clock Frequency (Note 41)	BCK	−	12.288	−	MHz
tABKOH	Bit Clock “H” Period (Note 41)	BCK	−	40.69	−	ns
tABKOL	Bit Clock “H” Period (Note 41)	BCK	−	40.69	−	ns
fABCKO	Bit Clock Frequency (Note 42)	BCK	−	6.144	−	MHz
tABKOH	Bit Clock “H” Period (Note 42)	BCK	−	81.38	−	ns
tABKOL	Bit Clock “L” Period (Note 42)	BCK	−	81.38	−	ns
tDL1	LRCK Output Delay Time	LRCK, Fs256ck	0	−	5	ns
tDL2	BCK Output Delay Time	BCK, Fs256ck	0	−	5	ns
tDL3	DATA Output Delay Time	DATA, Fs256ck	0	−	5	ns

41. When output Fs is set to 192 kHz and output format slot length is set to 64 fs.
42. When output Fs is set to 192 kHz and output format slot length is set to 32 fs.

STREAM DATA INPUT AND OUTPUT INTERFACE

The stream data input and output interface is a 3−wire type interface, and there are two methods to stream input and stream output.

1. Stream data input: Input STBCK and STDATI during STREQO = “H” output period.
2. Stream data output: Input STBCK and output STDATO during STREQI = “H” input period.

The bit clock and data are input according to the state of the STREQO signal, or the bit clock is input according to the state of STREQI and the data is output. The data transfer unit is 2 bytes (16 bits).In the stream output method, it is possible to output both the clock (STBCKO) and the data (STDATO).

- Stream data input and output port

Use the 3 pins: GP08_0, GP08_1 and GP08_3 as the stream data input and output port.
The function of each pin is set as shown in the table below.

Table 19.

Pin Name / Function	Stream Data Input	Stream Data Output	
GP08_0/STBCK	STBCKI (input)	STBCKO (output)	STBCKI (input)
GP08_1/STDATA	STDATI (input)	STDATO (output)	STDATO (output)
GP08_3/STREQ	STREQO (output)	STREQI (input)	STREQI (input)

- Stream data input timing − AC characteristics

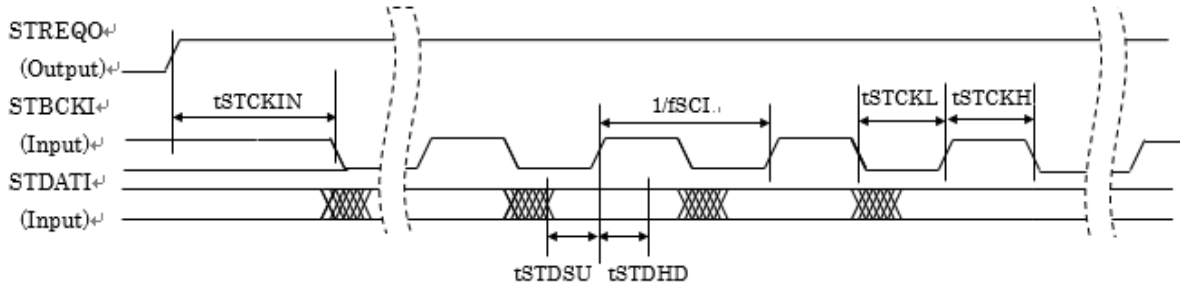


Figure 25. Stream Data Input Timing Chart

Table 20. Ta = −40 to 85°C, V_{DD} = 3.0 to 3.6 V, V_{DD}12 = 1.14 to 1.26 V, V_{SS} = 0 V

Symbol	Parameter	Signal Name	Min	Typ	Max	Unit
fSCI	STBCKI Clock Frequency	STBCKI	−	−	12	MHz
tSTCKIN	Stream Input Start Time	STREQO, STBCKI	100	−	−	ns
tSTCKH	STBCKI Clock “H” Period	STBCKI	40	−	−	ns
tSTCKL	STBCKI Clock “L” Period	STBCKI	40	−	−	ns
tSTDSU	STDATI Setup Time	STDATI, STBCKI	30	−	−	ns
tSTDHD	STDATI Hold Time	STDATI, STBCKI	30	−	−	ns

- Stream data output timing / STBCK output mode – AC characteristics

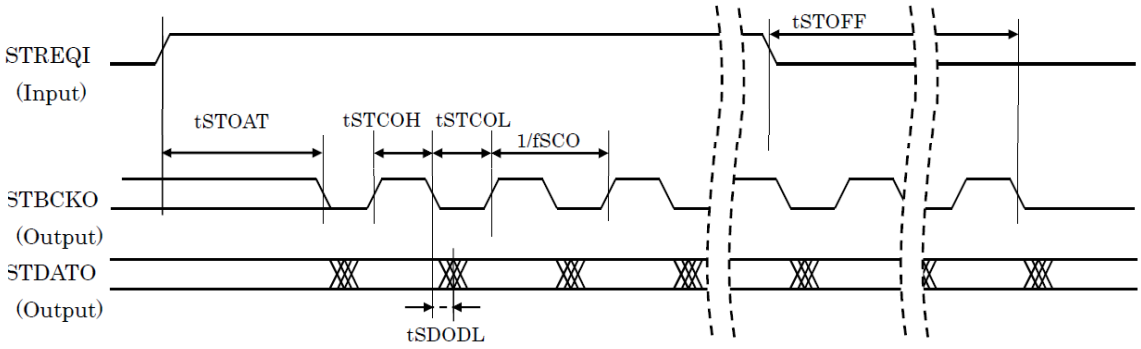


Figure 26. Stream Data Output / STBCK Output Mode – Timing Chart

Table 21. Ta = –40 to 85°C, V_{DD} = 3.0 to 3.6 V, V_{DD}12 = 1.14 to 1.26 V, V_{SS} = 0 V

Symbol	Parameter	Signal Name	Min	Typ	Max	Unit
fSCO	STBCKO Clock Frequency	STBCKO	–	–	30.72	MHz
tSTOAT	Stream Output Start Time	STREQI, STBCKO	–	–	(1/fSCO) x144	ns
tSTOFF	Stream Output Stop Time	STREQI, STBCKO	–	–	(1/fSCO) x144	ns
tSTCOH	STBCKO Clock “H” Period	STBCKO	13	–	–	ns
tSTCOL	STBCKO Clock “L” Period	STBCKO	16	–	–	ns
tSDODL	STDATO Output Delay Time	STDATO, STBCKO	0	–	3	ns

- Stream data output timing / STBCK input mode − AC characteristics

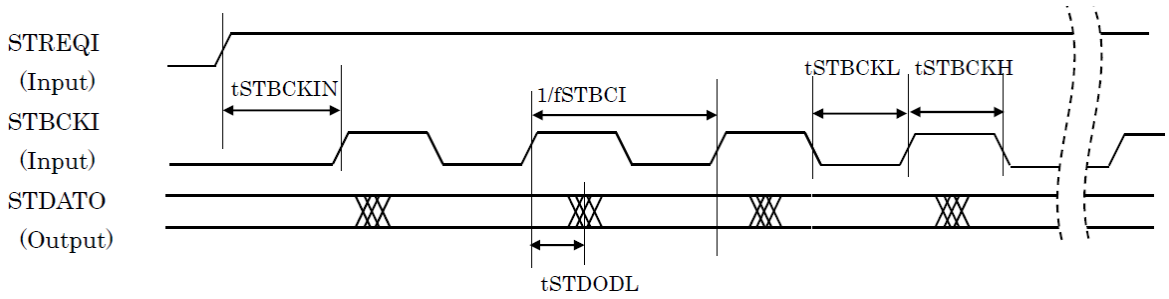


Figure 27. Stream Data Output / STBCK Input Mode Timing Chart

Table 22. Ta = −40 to 85°C, V_{DD} = 3.0 to 3.6 V, $V_{DD}12$ = 1.14 to 1.26 V, V_{SS} = 0 V

Symbol	Parameter	Signal Name	Min	Typ	Max	Unit
fSTBCI	STBCKI Clock Frequency	STBCKI	–	–	1.25	MHz
tSTBCKIN	STBCKI Input Start Time	STREQI, STBCKI	2000	–	–	ns
tSTBCKH	STBCKI Clock “H” Period	STBCKI	400	–	–	ns
tSTBCKL	STBCKI Clock “L” Period	STBCKI	400	–	–	ns
tSTDODL	STDATO Output Delay Time	STBCKI, STDATO	–	–	250	ns

NOTE:

Figure 27 shows STBCKI starting from “L”.

There are two clock input modes, and the data output timing changes as follows.

1. When starting from STBCKI = “L”, STDATO is output in synchronization with the rising edge of STBCKI.
2. When starting from STBCKI = “H”, STDATO is output in synchronization with the falling edge of STBCKI.

In either case, the output timing characteristics are the same.

DIGITAL MIC VOICE INPUT INTERFACE

This SoC has one digital microphone voice input interface.

- Digital mic interface port

Table 23.

Function	MEMSMIC DCK (Output)	MEMSMIC DIN (Input)
Port Assignment	GP08_0 or GP10_0 or GP13_4	GP08_1 or GP10_1 or GP13_5

- Digital mic interface timing – AC characteristics.

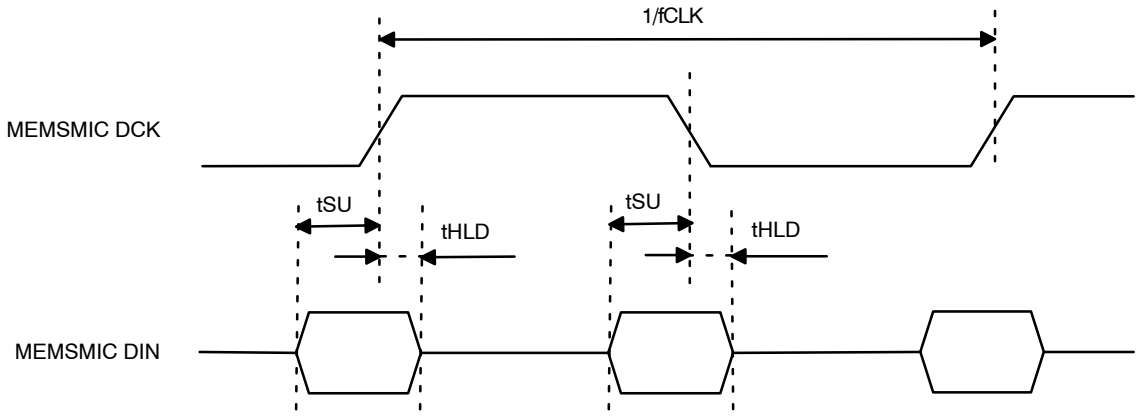


Figure 28. Digital Mic Input and Output Timing Chart

Table 24. Ta = −40 to 85°C, V_{DD} = 3.0 to 3.6 V, $V_{DD}12$ = 1.14 to 1.26 V, V_{SS} = 0 V

Symbol	Parameter	Signal Name	Min	Typ	Max	Unit
fCLK	MEMSMIC DCK Clock frequency (Note 43)	MEMSMIC_DCK	–	–	3.072	MHz
	MEMSMIC DCK Clock Duty Cycle	MEMSMIC_DCK	–	50	–	%
tSU	Data Input Setup Time	MEMSMIC_DIN, MEMSMIC_DCK	80	–	–	ns
tHLD	Data Input Hold Time	MEMSMIC_DIN, MEMSMIC_DCK	0	–	–	

43. Clock frequency can be changed by internal clock and register setting.

PSEUDO SRAM INTERFACE

This SoC has one Pseudo−SRAM interface.

- Pseudo−SRAM interface port

Table 25.

Signal Function	Port Assignment No.1.	Port Assignment No.2
PSRCLK	GP10_6	GP12_4
PSRCEn	GP10_4	GP12_2
PSRSI/SIO0	GP10_7	GP12_5
PSRSO/SIO1	GP10_3	GP12_1
/SIO2	GP10_2	GP12_0
/SIO3	GP10_5	GP12_3

44. You may only use one of the pin function assignments – select option No. 1 or option No. 2. Mixing of the two options is prohibited.

- Pseudo SRAM interface timing − AC characteristics

When Serial Interface is Selected:

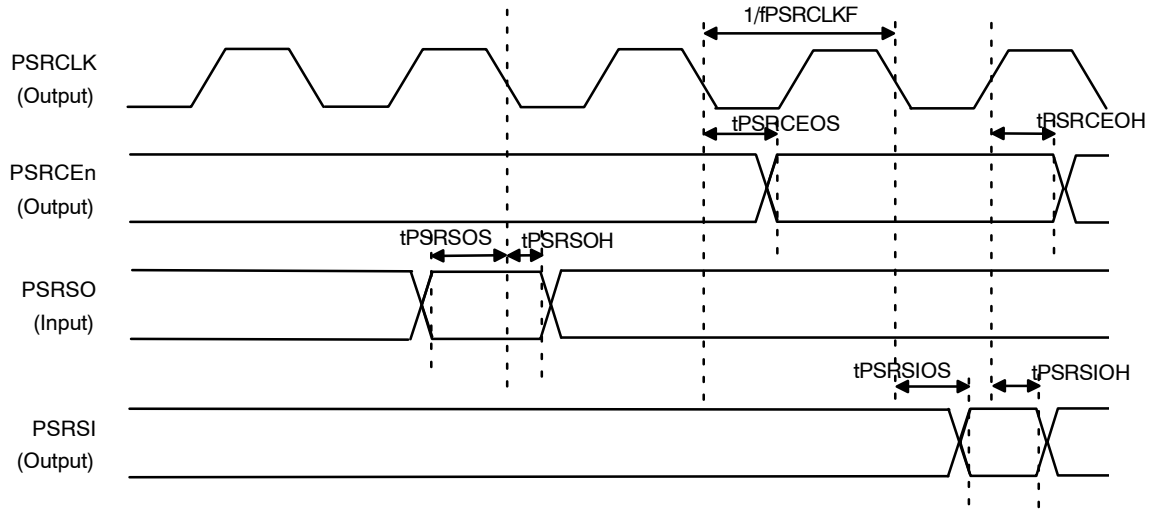


Figure 29. Pseudo SRAM Interface Timing Chart – Serial Interface Selected

When Quad Interface is Selected:

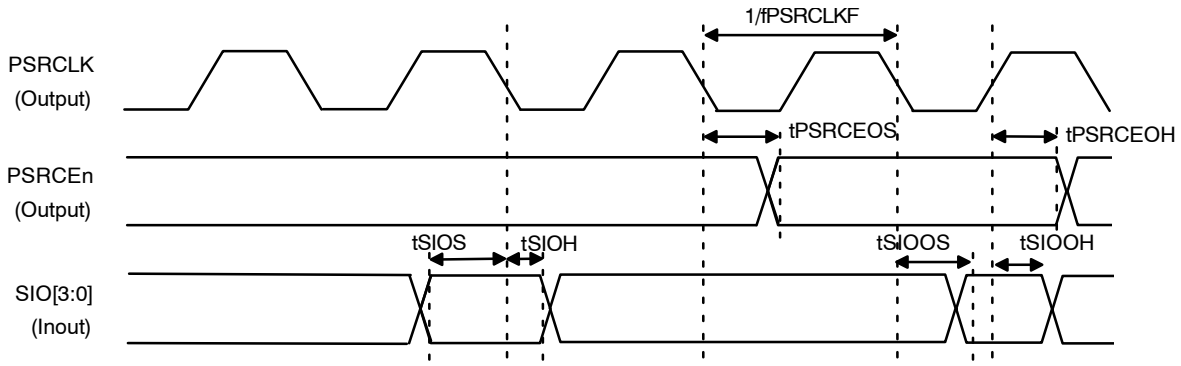


Figure 30. Pseudo SRAM Interface Timing Chart – Quad Interface Selected

Table 26. Ta = −40 to 85°C, V_{DD} = 3.0 to 3.6 V, V_{DD}12 = 1.14 to 1.26 V, V_{SS} = 0 V, External Load 50 pF

Symbol	Parameter	Signal Name	Min	Typ	Max	Unit
fPSRCLKF	PSRCLK Clock Frequency	PSRCLK	–	–	30	MHz
tPSRCSOS	Chip Select Output Settle Time	PSRCEn	–	–	1.1	ns
tPSRCSOH	Chip Select Output Hold Time	PSRCEn	13	–	–	
tPSRSOS	Data Input Setup Time (Serial Interface Selected)	PSRSO	11.1	–	–	
tPSRSOH	Data Input Hold Time (Serial Interface Selected)	PSRSO	0.9	–	–	
tPSRSIOS	Data Output Settle Time (Serial Interface Selected)	PSRSI	–	–	8.2	
tPSRSIOH	Data Output Hold Time (Serial Interface Selected)	PSRSI	13	–	–	
tSIOS	Data Input Setup Time (Quad Interface Selected)	SIO[3:0]	15.6	–	–	
tSIOH	Data input Hold Time (Quad Interface Selected)		0.9	–	–	
tSIOOS	Data Output Settle Time (Quad Interface Selected)		–	–	8.2	
tSIOOH	Data Output Hold Time (Quad Interface Selected)		13	–	–	

AUDIO DATA INPUT OR OUTPUT CHARACTERISTICS

AC ELECTRICAL CHARACTERISTICS (Ta = 25°C, VDD = 3.3 V, VDD12 = 1.2 V
DVSS = AVSS − N* = UVSS1 = UVSS2 = XVSS = XVSS12 = 0 V (Note *: N = 0 to 5))

Symbol	Parameter	Pin Name	Condition	Min	Typ	Max	Unit
AUDIO−ADC AND INPUT AMP (Fs = 48.0 kHz, Audio Signal Frequency: 1 kHz, Measurement Range = 10 Hz to 20 kHz (Using A−filter))							
ASS + ADC							
	Full Scale Analog Input Level (Note 45)	L1IN, R1IN, L2IN, R2IN, L3INP, L3INN, R3INP, R3INN, L4INP, L4INN, R4INP, R4INN		2.605	2.805 (0.85*VDD)	3.005	Vpp
	Input Impedance			20	30	−	kΩ
	Gain Setting Level			−12	−	19	dB
	Gain Setting Step			−	1	−	dB
	Gain Setting Step Error			−0.5	−	0.5	dB
S/N	Signal to Noise Ratio		0 dB data, 20 kHz − LPF	90	98	−	dB
DR	Dynamic Range		−60 dB data, 20 kHz − LPF	90	98	−	dB
THD+N	Total Harmonic Distortion		Input condition: −3 dBFS	−	−85	−80	dB
CT1	Cross Talk1		Between channels	−	−100	−85	dB
CT2	Cross Talk2		Between sources	−	−100	−85	dB
ADC DIGITAL FILTER							
	Passband Frequency		±0.04 dB	0	−	0.4535	Fs
	Stopband Frequency			0.5465	−	−	Fs
	Passband Ripple			−	−	±0.04	dB
	Stopband Attenuation		>24.1 kHz	−69	−	−	dB
	HPF Cut Off Frequency for DC Offset Cancellation			−	0.00002	−	Fs
MIC AMP (Choose one from 4 Gain Setting Levels)							
	Input Impedance	MICINP, MICINN		20	30	−	kΩ
	Gain Setting (Note 46)			0	−	30	dB
AUDIO−DAC (Fs = 96.0 kHz, Audio Signal Frequency: 1 kHz, Measurement Range = 10 Hz to 20 kHz (Using A−filter))							
DAC							
	Full Scale Analog Output Level	DACOUT1L, DACOUT1R, DACOUT2L, DACOUT2R, DACOUTS		2.605	2.805 (0.85*VDD)	3.005	Vpp
S/N	Signal to Noise Ratio		0 dB data, 20 kHz − LPF	−	106	−	dB
DR	Dynamic Range		−60 dB data, 20 kHz − LPF	−	106	−	dB
THD+N	Total Harmonic Distortion		0 dB data, 20 kHz − LPF	−	−85	−80	dB
CT	Cross Talk		0 dB data, 20 kHz − LPF	−	−100	−85	dB
DF							
	Passband Frequency		±0.015 dB	0	−	0.4535	Fs
	Stopband Frequency			0.5465	−	−	Fs
	Passband Ripple			−	−	±0.04	dB
	Stopband Attenuation			−62	−	−	dB
	HPF Cut Off Frequency for DC Offset Cancellation		−3 dB	−	0.0000385	−	Fs

45. The value of 1/2 of the above specification is used when the part is used with differential input.
46. Gain Setting can be one of 4 mode: 0 dB, +18 dB, +24 dB or +30 dB.

GENERAL ADC ANALOG CHARACTERISTICS

Table 27. Ta = 25°C, VDD = 3.3 V, VDD12 = 1.2 V
DVSS = AVSS−N* = UVSS1 = UVSS2 = XVSS = XVSS12 = 0 V (*: N = 0 to 5)

Symbol	Parameter	Pin Name	Min	Typ	Max	Unit
R.S	Resolution		−	−	12	Bit
Fs	Conversion Time (Note 47)		−	−	1	MHz
VRH	Reference Voltage (High)		−	−	AVDD33	V
VRL	Reference Voltage (Low)		AVSS33	−	−	V
Vaio	Analog Signal Input Voltage Range	GP05−0, GP05−1, GP05−2, GP05−3, GP05−4, GP05−5, GP05−6, GP05−7	VRL	−	VRH	V

47. The conversion time varies depending on the Cortex−M0+ system clock frequency.

USB2.0 PHY CHARACTERISTICS

The USB2.0 PHY supports the following standards.
HS−USB

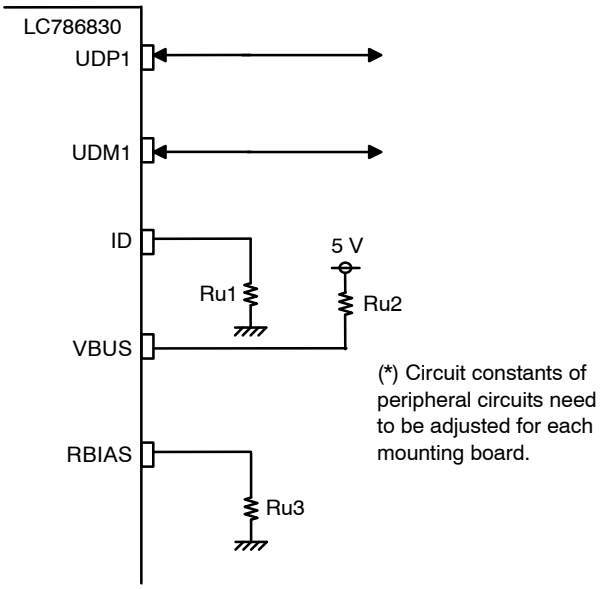
- USB2.0 High/Full Speed Controller and PHY build−in
- Universal Serial Bus Specification, Revision 2.0
- On The Go and Embedded Host Supplement to the USB Revision 2.0 Specification, Revision 2.0 (ADP is not supported)

FS−USB

- USB2.0 Full Speed Controller and PHY built−in
- Open HCI (Open Host Controller Interface) 1.0a
- Universal Serial Bus Specification 2.0 Full Speed compliance

APPLICATION

- Example of USB port circuit



NOTE: Ru1 is a resistor for pulling down the ID terminal. The reference resistance value is 2.2 kΩ.
Ru2 is a pull−up resistor for the VBUS terminal. The reference resistance value is 1.0 kΩ.
Ru3 is a pull−down resistor for the RBIAS pin. Use 270 Ω ±1%

Figure 31.

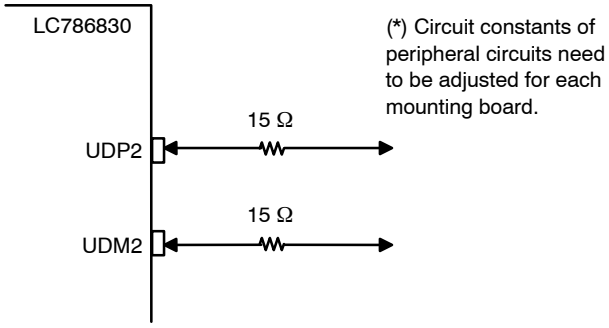


Figure 32.

- Example of Oscillator port circuit (32.768 kHz)

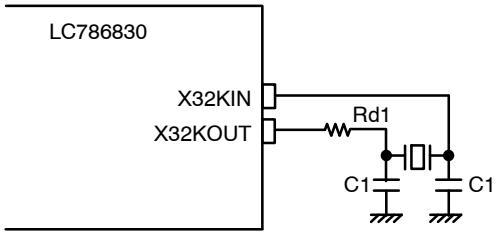


Figure 33.

- X32KIN and X32KOUT pin connection oscillator: 32.768 kHz
- For –built−in RTC
- Recommended oscillator

NIHON DEMPA KOGYO CO., LTD.

Part Number	Frequency	Recommended Constant
NX3215SA	32.768 kHz	Rd1 = 0 Ω, C1 = 18 pF

NOTE:

48. Since the oscillator circuit characteristics may change depending on the set board, consult the oscillator manufacturer to determine the above constants.
49. Disturbance of the oscillation clock due to noise or the like causes a malfunction. To prevent this, place the resistors and capacitors used in the oscillator circuit as close to the X32KIN and X32KOUT pins as possible, and ensure the wiring length is the shortest possible.
    Moreover, if the external constants change due to temperature changes, etc., the oscillation accuracy may be affected. Therefore, it is necessary to be careful when selecting components so that the external constant values do not change within the guaranteed operating temperature range.
50. For the internal configuration of X32KIN and X32KOUT pin, refer to the "Analog Pin Internal Equivalent Circuit" section.

- Example of Oscillator port circuit (24.0 MHz)

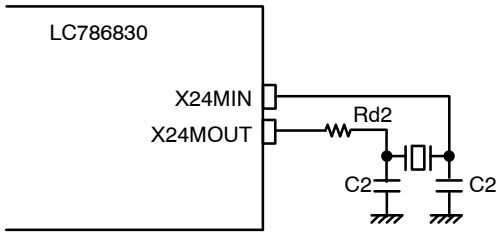


Figure 34.

- X24MIN and X24MOUT Connection oscillator: 24.0000 MHz
- For system clock and audio clock, USB controller
- Recommended oscillator

NIHON DEMPA KOGYO CO., LTD.

Part Number	Frequency	Recommended Constant
NX3225GA	24 MHz	Rd2 = 220 Ω, C2 = 6 pF

NOTE:

51. Since the oscillator circuit characteristics may change depending on the set board, consult the oscillator manufacturer to determine the above constants.
52. Regarding the accuracy of the oscillator used for X24MIN and X24MOUT, use an oscillator that satisfies the USB standard.
53. Disturbance of the oscillation clock due to noise or the like causes a malfunction. To prevent this, place parts such as resistors and capacitors used in the oscillator circuit as close to the X24MIN and X24MOUT pins as possible, and ensure the wiring length is the shortest possible.
    Moreover, if the external constants change due to temperature changes, etc., the oscillation accuracy may be affected. Therefore, it is necessary to be careful when selecting components so that the external constant values do not change within the guaranteed operating temperature range.
54. For the internal configuration of X24MIN and X24MOUT, refer to the "Analog Pin Internal Equivalent Circuit" section.

- Example of PLL port circuit

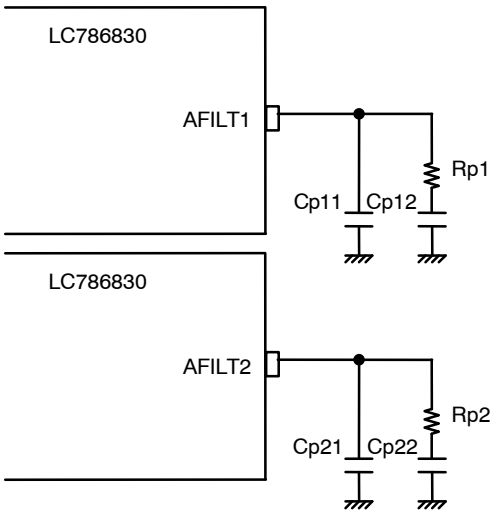


Figure 35.

AFILT1 Constant
Rp1 = 1.5 kΩ, Cp11 = 220 pF, Cp12 = 4700 pF

AFILT2 Constant
Rp2 = 2.2 kΩ, Cp21 = 220 pF, Cp22 = 6800 pF

NOTE:

55. Resistors (Rp1 and Rp2) and capacitors (Cp11, Cp12, Cp21, and Cp22) connected to AFILT1 and AFLIT2 are PLL filter circuits for audio and system clock generation. Disturbance of the oscillation clock due to noise or the like causes a malfunction. To prevent this, place the resistors and capacitors that make up the filter circuit as close to the AFILT1 and AFILT2 terminals as possible, and ensure the wiring length is the shortest possible.
    Also, if the filter constant changes due to temperature changes, the PLL oscillation becomes unstable and the audio playback clock becomes unstable, so the audio signal input (ADC operation) and output (various filters, DAC operation) become unstable. Audio playback is affected. Therefore, you must be careful when selecting components so that the filter constant does not change within the guaranteed operating temperature range.
56. For the internal configuration of AFILT1 and AFILT2, refer to the "Analog Pin Internal Equivalent Circuit" section.

- Example of LPDSP debugger port (JTAG) circuit

Table 28. LPDSP DEBUGGER INTERFACE (JTAG) PORT

LPDSP Debugger Signal Name	Port Assignment No.1	Port Assignment No.2
LPDSP_TCK	GP10_4	GP12_2
LPDSP_TMS	GP10_5	GP12_3
LPDSP_TDI	GP10_6	GP12_4
LPDSP_TDO	GP10_7	GP12_5

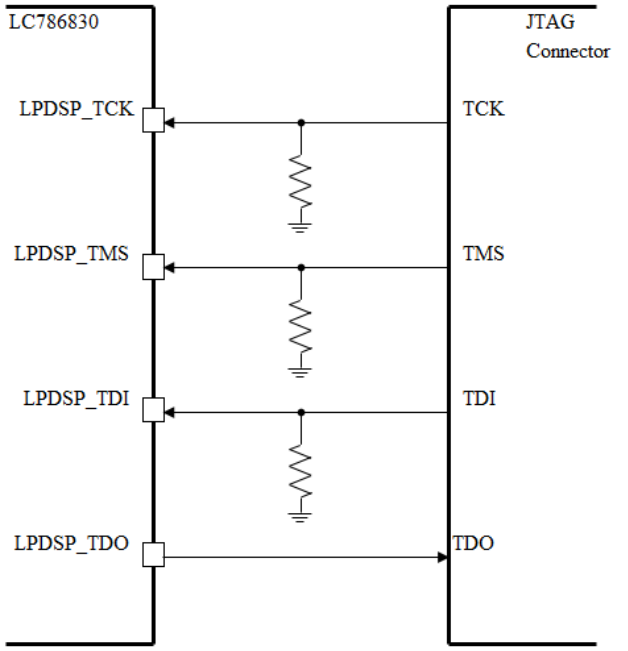


Figure 36.

NOTE:

57. LPDSP is reset by the JTAG software reset command and the JTAG hardware reset signal (TRST) issued by the debugger. Therefore, it is not essential to connect the JTAG hardware reset signal between the debugger and this SoC.
58. The LPDSP debugger function is used exclusively with other functions. At system startup, the debugger function is not selected as the pin function. To use the debugger function, the Cortex−M0+ software must implement the process to enable the debugger function.
59. LPDSP debugger function is one system implementation. You may only use one set of pin function assignments – select option No. 1 or option No. 2. Mixing of the two assignment options is prohibited.
60. An internal pull−down resistor is mounted on the pin to which the LPDSP debugger function is assigned. A built−in pull−down resistor can be used instead of the resistor mounted on the wiring with the JTAG connector.
61. The input JTAG signal should be pulled up or down to prevent it from floating if the JTAG function is not used.
62. For details of the JTAG signal connection, refer to the reference circuit provided by the ICE tool vendor.

- Example of Cortex−M0+ and Cortex−M3 debugger port (SWD) circuit

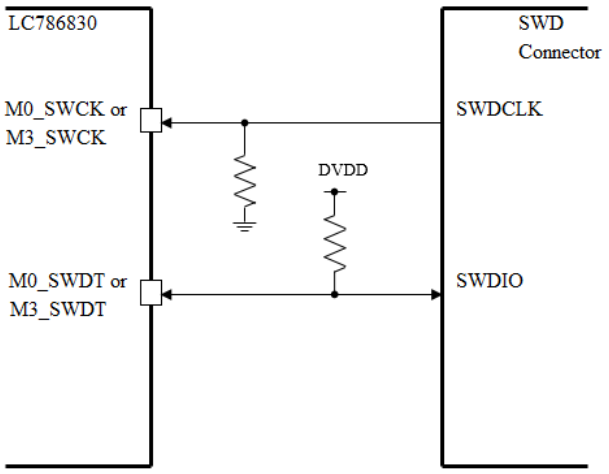


Figure 37.

NOTE:

63. This SoC does not support the trace function port (SWO).
64. In this SoC, SWDCLK signal connection terminals (M0_SWCK or M3_SWCK) have built−in pull−down resistors, and SWDIO signal connection terminals (M0_SWDT or M3_SWDT) have built−in pull−up resistors.
    A built−in pull resistor can be used instead of the pull resistor connected to the wiring with the SWD connector.
65. For details of the SWD connector signals, refer to the document provided by the ICE tool vendor.

EXAMPLE OF PERIPHERAL CIRCUIT DIAGRAM

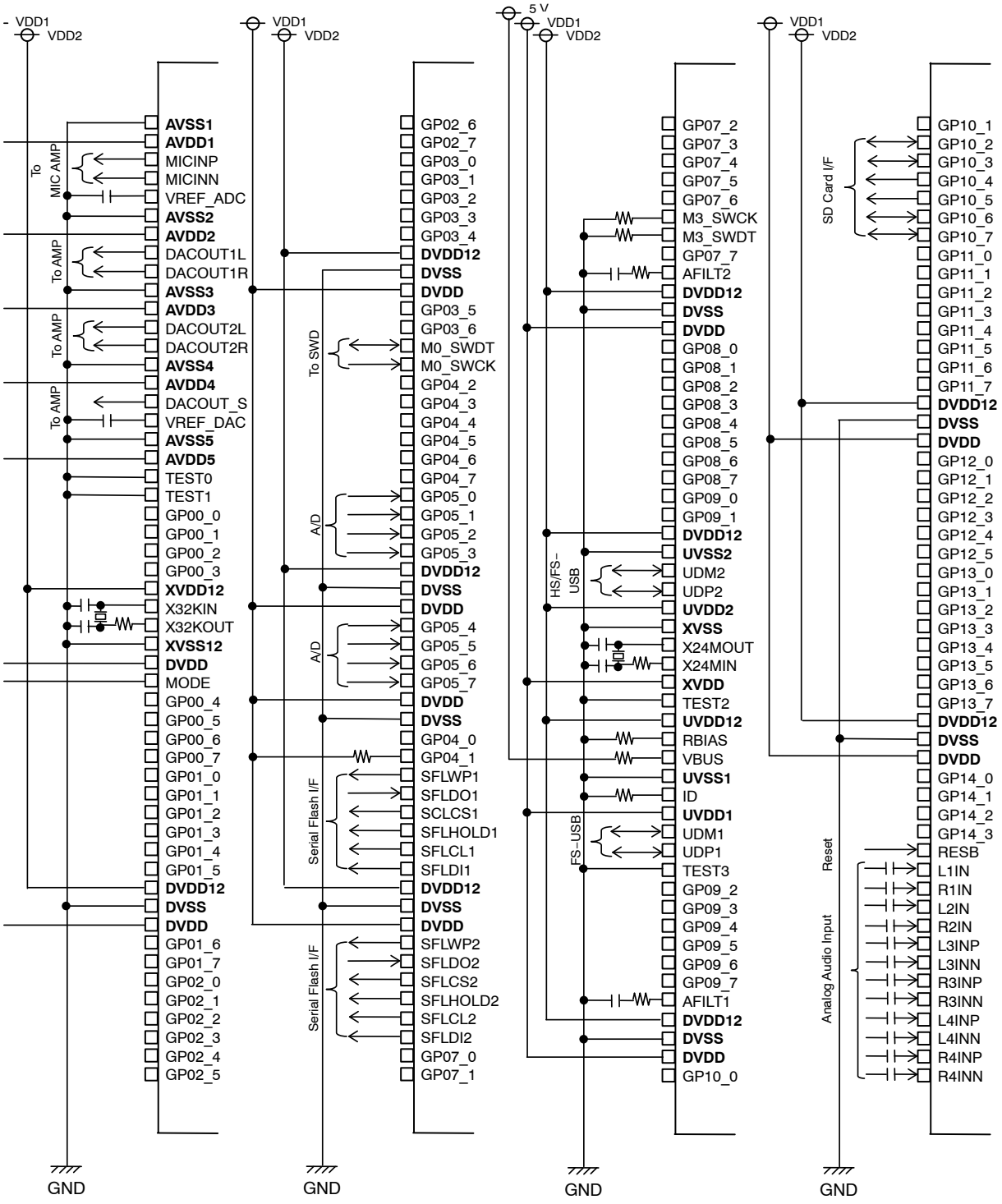


Figure 38. Example of Peripheral Circuit Diagram

LC786830 PIN FUNCTION TABLE

The LC786830 pin function table is shown below.

Table 29 is a list of the function allocation of GP00_0 to GP05_7 pins. These functions can be controlled by Cortex−M0+.

Tables 30 and 31 are a list of GP07_0 to GP14_4 pin functions. These functions can be controlled by Cortex−M3.

Table 29. GP00_0 TO GP05_7 PIN FUNCTION ASSIGNMENT TABLE

PIN Name	Pin No	PORT Function							
		General I/O	External Interrupt	Timer (Capture)	Timer (PWM)	IIC Master	SIO	UART	ADC Input
GP00_0	22	O	INTR0						
GP00_1	23	O	INTR1						
GP00_2	24	O	INTR2						
GP00_3	25	O	INTR3						
GP00_4	32	O	INTR4	Capture0					
GP00_5	33	O	INTR5	Capture0					
GP00_6	34	O	INTR6	Capture0					
GP00_7	35	O	INTR7	Capture0	PWM 0				
GP01_0	36	O				IICM 1 CLK	SIO1 CLK		
GP01_1	37	O				IICM 1 DAT A	SIO1 DI		
GP01_2	38	O					SIO1 DO		
GP01_3	39	O		Capture1	PWM 1				
GP01_4	40	O							
GP01_5	41	O							
GP01_6	45	O							
GP01_7	46	O		Capture2	PWM 2				
GP02_0	47	O							
GP02_1	48	O							
GP02_2	49	O							
GP02_3	50	O					SIO2 DO		
GP02_4	51	O				IICM 2 CLK	SIO2 CLK		
GP02_5	52	O				IICM 2 DAT A	SIO2 DI		
GP02_6	53	O						UART 1 TX	
GP02_7	54	O						UART 1 RX	
GP03_0	55	O							
GP03_1	56	O					SIO4 CLK	UART 2 TX	
GP03_2	57	O					SIO4 DI	UART 2 RX	
GP03_3	58	O					SIO4 DO		
GP03_4	59	O				IICM 3 CLK	SIO3 CLK	UART 3 TX	
GP03_5	63	O				IICM 3 DAT A	SIO3 DI	UART 3 RX	
GP03_6	64	O					SIO3 DO		
GP04_0	86	O							
GP04_1	87	Input only							
GP04_2	67	O							
GP04_3	68	O							
GP04_4	69	O							
GP04_5	70	O							
GP04_6	71	O							
GP04_7	72	O		Capture3	PWM 3				
GP05_0	73	O							AD IN0
GP05_1	74	O							AD IN1
GP05_2	75	O							AD IN2
GP05_3	76	O							AD IN3
GP05_4	80	O						UART 2 TX	AD IN4
GP05_5	81	O					SIO4 CLK	UART 2 RX	AD IN5
GP05_6	82	O					SIO4 DI	UART 3 TX	AD IN6
GP05_7	83	O					SIO4 DO	UART 3 RX	AD IN7

Table 30. GP07_0 TO GP10_7 PIN FUNCTION ASSIGNMENT TABLE

PIN Name	Pin No	Function															
		General I/O	External Interrupt	IIS Output	IIS Input	PCM I/F	STREAM DATA I/F	CDDSP I/F (Note 66)	I²C Master	SIO	UART	Digital Mic IN	SD Card I/F	PSRAM I/F	256 fs Clock In/Out	S/PDIF Output	LPDSP Debug I/F
GP07_0	103	○		IIS LRCK													
GP07_1	104	○		IIS BCK													
GP07_2	105	○		IIS Front													
GP07_3	106	○		IIS Rear													
GP07_4	107	○		IIS Sub													
GP07_5	108	○			IIS1 LRCK					SIO4 DO							
GP07_6	109	○			IIS1 BCK					SIO4 DI							
M 3_SWCK (Note 67)	110				IIS1 DATA					SIO4 CLK							
GP07_7	112	○			IIS1 DATA												
GP08_0	117	○					STREAM CLK					Digital MIC CLK			256FS In or Out	SPDIF DOUT	
GP08_1	118	○					STREAM DATA					Digital MIC DATA					
GP08_2	119	○															
GP08_3	120	○					STREAM REQ										
GP08_4	121	○															
GP08_5	122	○															
GP08_6	123	○															
GP08_7	124	○															
GP09_0	125	○									UART 1 TX						
GP09_1	126	○									UART 1 RX						
GP09_2	146	○				PCM LRCK											
GP09_3	147	○				PCM BCK											
GP09_4	148	○				PCM DI											
GP09_5	149	○				PCM DO											
GP09_6	150	○															
GP09_7	151	○	INTR0														
GP10_0	156	○									UART 2 TX	Digital MIC CLK					
GP10_1	157	○									UART 2 RX	Digital MIC DATA					
GP10_2	158	○			IIS4 LRCK						UART 3 TX		SDC DT1	SIO[2]			
GP10_3	159	○			IIS4 BCK						UART 3 RX		SDC DT0	PSRSO or SIO[1]			
GP10_4	160	○			IIS4 DATA								SDC CLK	PSRCEn			JTAG TCK
GP10_5	161	○			IIS5 LRCK				IICM2 CLK	SIO2 CLK			SDC CMD	SIO[3]			JTAG TMS
GP10_6	162	○			IIS5 BCK				IICM2 DATA	SIO2 DI			SDC DT3	PSRCLK			JTAG TDI
GP10_7	163	○			IIS4 DATA					SIO2 DO			SDC DT2	SPRSI or SIO[0]			JTAG TDO

66. For CD−DSP (LC78615E or LC78616PE) connection interface.
67. Pin functions can be assigned only when the Cortex−M3 debugger function is not used

Table 31. GP11_0 TO GP14_3 PIN FUNCTION ASSIGNMENT TABLE

PIN Name	Pin No	Function															
		General I/O	External Interrupt	Digital Audio OUT	Digital Audio IN	PCM I/F	Stream Data Trans	CDDSP I/F (Note 68)	I^2C Master	SIO	UART	Digital Mic IN	SD Card I/F	PSRAM I/F	256 fs Clock In/Out	S/PDIF Output	LPDSP Debug I/F
GP11_0	164	O								SIO5 DO							
GP11_1	165	O								SIO5 DI							
GP11_2	166	O								SIO5 CLK							
GP11_3	167	O															
GP11_4	168	O						SBCK									
GP11_5	169	O						PWI									
GP11_6	170	O						SFSY									
GP11_7	171	O						SBSY									
GP12_0	175	O	INTR1										SDC DT1	SIO[2]			
GP12_1	176	O			IIS2 LRCK								SDC DT0	PSRSO or SIO[1]			
GP12_2	177	O			IIS2 BCK								SDC CLK	PSRCEn			JTAG TCK
GP12_3	178	O			IIS2 DATA								SDC CMD	SIO[3]			JTAG TMS
GP12_4	179	O	INTR2										SDC DT3	PSRCLK			JTAG TDI
GP12_5	180	O											SDC DT2	SPRSI or SIO[0]			JTAG TDO
GP13_0	181	O								SIO1 DO							
GP13_1	182	O							IICM 1 CLK	SIO1 CLK							
GP13_2	183	O							IICM 1 DATA	SIO1 DI							
GP13_3	184	O			IIS3 LRCK					SIO2 DO							
GP13_4	185	O			IIS3 BCK				IICM 2 CLK	SIO2 CLK		Digital MIC CLK					
GP13_5	186	O			IIS3 DATA				IICM 2 DATA	SIO2 DI		Digital MIC DATA					
GP13_6	187	O							IICM 3 CLK	SIO3 CL							
GP13_7	188	O							IICM 3 DATA	SIO3 DI							
GP14_0	192	O								SIO3 DO	UART 4 RTS						
GP14_1	193	input only									UART 4 CTS						
GP14_2	194	input only									UART 4 RX						
GP14_3	195	O									UART 4 TX						

68. For CD−DSP (LC78615E or LC78616PE) connection interface.

ANALOG PIN INTERNAL EQUIVALENT CIRCUIT

The following table shows the internal equivalent circuit of the analog terminal.

Table 32.

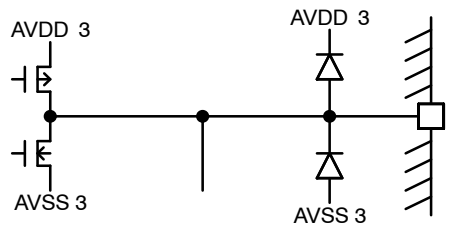
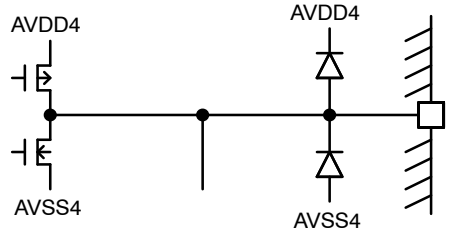
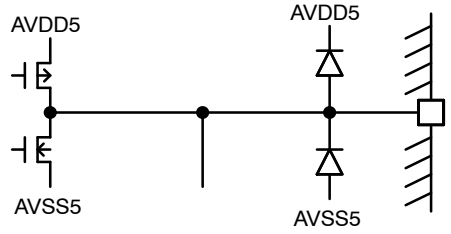
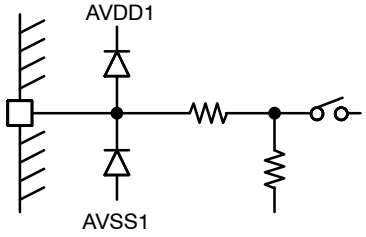
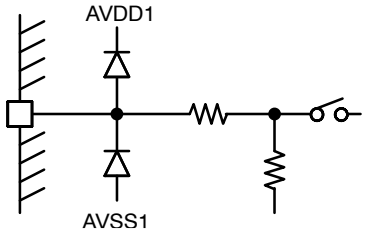
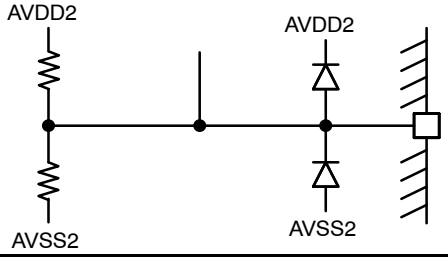
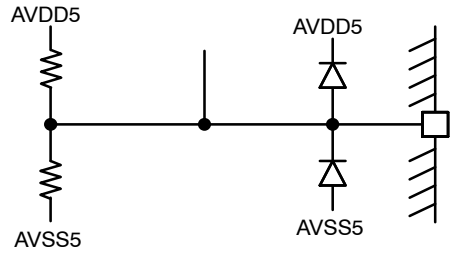
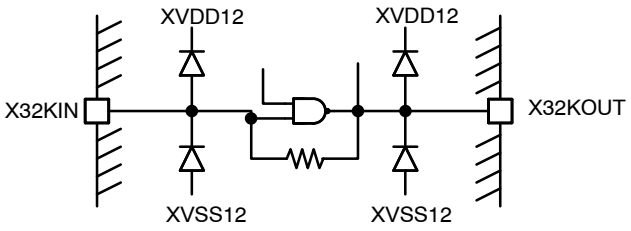
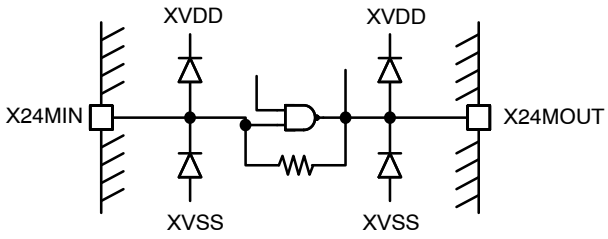
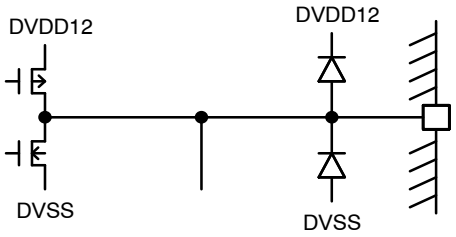
Pin Name (Pin No.)	Internal Equivalent Circuit
DACOUT1L (8) DACOUT1R (9)	
DACOUT2L (12) DACOUT2R (13)	
DACOUT_S (16)	
MICINP (3) MICINN (4)	
L1IN (197) R1IN (198) L2IN (199) R2IN (200) L3INP (201) L3INN (202) R3INP (203) R3INN (204) L4INP (205) L4INN (206) R4INP (207) R4INN (208)	
VREF_ADC (5)	

Table 32.

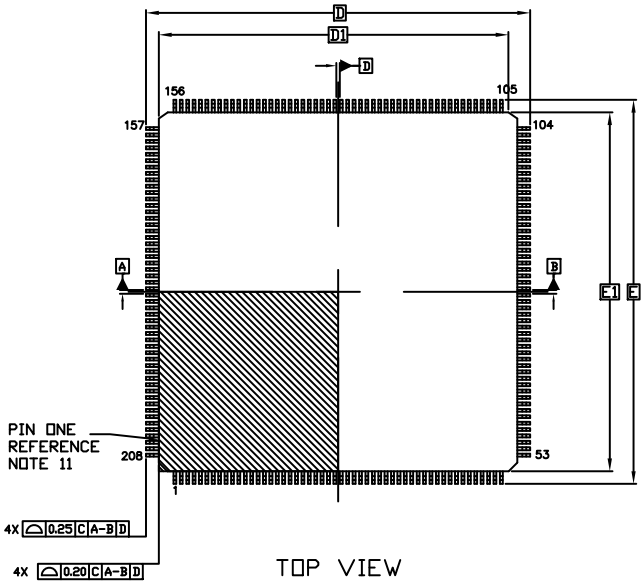
Pin Name (Pin No.)	Internal Equivalent Circuit
VREF_DAC (17)	
X32KIN (27) X32KOUT (28)	
X24MIN (134) X24MOUT (133)	
AFILT1 (152) AFILT2 (113)	

ORDERING INFORMATION

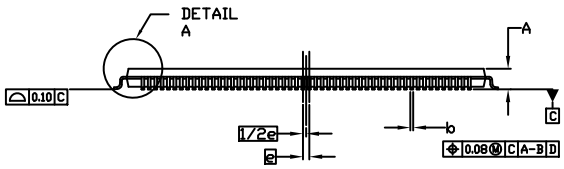
Device Order Number	Package Type	Shipping
LC786830W−2H	LQFP 208, 28X28 (Pb−Free / Halogen Free)	180 / Tray Form

LQFP 208, 28x28
CASE 561AP
ISSUE A

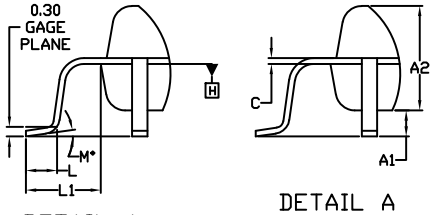
DATE 31 JAN 2018



TOP VIEW



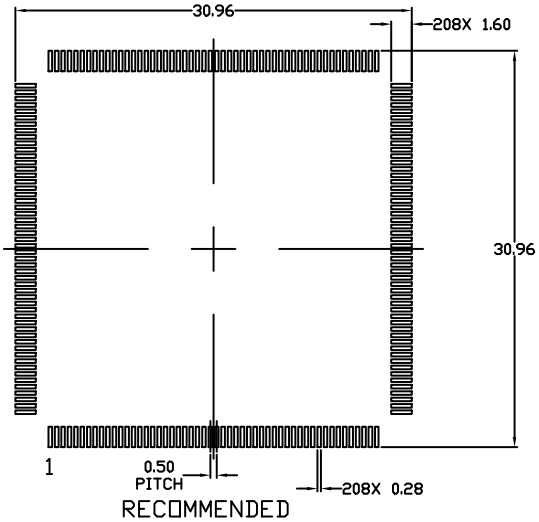
SIDE VIEW



DETAIL A DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
5. THE TOP PACKAGE BODY SIZE IS SMALLER THAN THE BOTTOM PACKAGE SIZE AND TOP PACKAGE WILL NOT OVERHANG THE BOTTOM.
6. DATUM PLANE H IS LOCATED AT THE BOTTOM MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
7. DIMENSIONS D1 AND E1 TO BE DETERMINED AT DATUM PLANE H.
8. DATUMS A-B AND D ARE DETERMINED AT DATUM PLANE H.
9. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
10. DIMENSIONS D AND E TO BE DETERMINED AT DATUM PLANE C.
11. PIN 1 IS LOCATED IN THIS AREA. MAY APPEAR AS AN EJECTOR MARK, LASER MARK, ETC.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.60
A1	0.05	---	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	---	0.20
D	30.00 BSC		
D1	28.00 BSC		
E	30.00 BSC		
E1	28.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
M	0°	---	7°



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*

XXXXXXXXXXXXXXX
XXXXXXXXXXXXXXX
XXXXXXXXXXXXXXX
XXXXXXXXXXXXXXX
AWLYYWWG

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON31374E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**LQFP 208, 28X28**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

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