ON Semiconductor

Is Now



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Low Noise, Audio Dual Operational Amplifier

LM833, NCV833

The LM833 is a standard low–cost monolithic dual general–purpose operational amplifier employing Bipolar technology with innovative high–performance concepts for audio systems applications. With high frequency PNP transistors, the LM833 offers low voltage noise (4.5 nV/ $\sqrt{\text{Hz}}$), 15 MHz gain bandwidth product, 7.0 V/ μ s slew rate, 0.3 mV input offset voltage with 2.0 μ V/°C temperature coefficient of input offset voltage. The LM833 output stage exhibits no dead–band crossover distortion, large output voltage swing, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

For an improved performance dual/quad version, see the MC33079 family.

Features

• Low Voltage Noise: $4.5 \text{ nV}/\sqrt{\text{Hz}}$

• High Gain Bandwidth Product: 15 MHz

• High Slew Rate: 7.0 V/μs

• Low Input Offset Voltage: 0.3 mV

• Low T.C. of Input Offset Voltage: $2.0 \mu V/^{\circ}C$

• Low Distortion: 0.002%

• Excellent Frequency Stability

• Dual Supply Operation

 NCV Prefix for Automotive and Other Applications Requiring Site and Change Controls

• These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V _{CC} to V _{EE})	Vs	+36	٧
Input Differential Voltage Range (Note 1)	V_{IDR}	30	V
Input Voltage Range (Note 1)	V _{IR}	±15	V
Output Short Circuit Duration (Note 2)	t _{SC}	Indefinite	
Operating Ambient Temperature Range	T _A	-40 to +85	°C
Operating Junction Temperature	TJ	+150	°C
Storage Temperature	T _{stg}	-60 to +150	°C
ESD Protection at any Pin - Human Body Model - Machine Model	V _{esd}	600 200	V
Maximum Power Dissipation (Notes 2 and 3)	P_{D}	500	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE} .
- Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see power dissipation performance characteristic).
- 3. Maximum value at $T_A \le 85$ °C.



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MARKING DIAGRAMS



PDIP-8 N SUFFIX CASE 626



LM833N = Device Code A = Assembly Location

WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb-Free Package



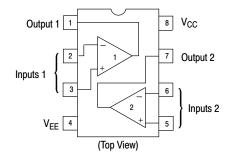
SOIC-8 D SUFFIX CASE 751



LM833 = Device Code A = Assembly Location

L = Wafer Lot Y = Year W = Work Week ■ Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
Input Offset Voltage (R _S = 10 Ω , V _O = 0 V)	V _{IO}	-	0.3	5.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω , V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	-	2.0	-	μV/°C
Input Offset Current (V _{CM} = 0 V, V _O = 0 V)	I _{IO}	-	10	200	nA
Input Bias Current (V _{CM} = 0 V, V _O = 0 V)	I _{IB}	-	300	1000	nA
Common Mode Input Voltage Range	V _{ICR}	- -12	+14 -14	+12 -	V
Large Signal Voltage Gain (R _L = 2.0 k Ω , V _O = ± 10 V)	A _{VOL}	90	110	_	dB
Output Voltage Swing: $ \begin{aligned} R_L &= 2.0 \text{ k}\Omega \text{ V}_{\text{ID}} = 1.0 \text{ V} \\ R_L &= 2.0 \text{ k}\Omega \text{ V}_{\text{ID}} = 1.0 \text{ V} \\ R_L &= 10 \text{ k}\Omega \text{ V}_{\text{ID}} = 1.0 \text{ V} \\ R_L &= 10 \text{ k}\Omega \text{ V}_{\text{ID}} = 1.0 \text{ V} \end{aligned} $	V _{O+} V _{O-} V _{O+} V _{O-}	10 - 12 -	13.7 -14.1 13.9 -14.7	- -10 - -12	V
Common Mode Rejection (V _{in} = ±12 V)	CMR	80	100	-	dB
Power Supply Rejection (V _S = 15 V to 5.0 V, -15 V to -5.0 V)	PSR	80	115	-	dB
Power Supply Current (V _O = 0 V, Both Amplifiers)	I _D	-	4.0	8.0	mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
Slew Rate (V_{in} = -10 V to +10 V, R_L = 2.0 k Ω , A_V = +1.0)		5.0	7.0	-	V/μs
Gain Bandwidth Product (f = 100 kHz)		10	15	-	MHz
Unity Gain Frequency (Open Loop)		-	9.0	-	MHz
Unity Gain Phase Margin (Open Loop)		-	60	-	0
Equivalent Input Noise Voltage (R _S = 100 Ω, f = 1.0 kHz)		-	4.5	-	nV/√ Hz
Equivalent Input Noise Current (f = 1.0 kHz)		-	0.5	-	pA/√Hz
Power Bandwidth (V_0 = 27 V_{pp} , R_L = 2.0 k Ω , THD \leq 1.0%)	BWP	-	120	-	kHz
Distortion (R _L = 2.0 k Ω , f = 20 Hz to 20 kHz, V _O = 3.0 V _{rms} , A _V = +1.0)		-	0.002	-	%
Channel Separation (f = 20 Hz to 20 kHz)	C _S	_	-120	-	dB

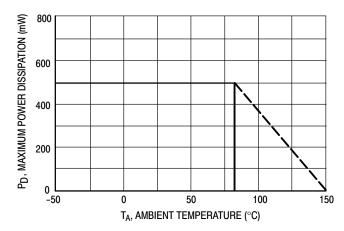


Figure 1. Maximum Power Dissipation versus Temperature

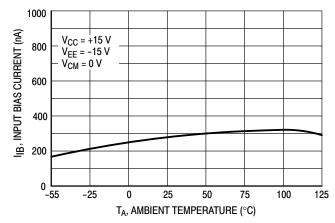


Figure 2. Input Bias Current versus Temperature

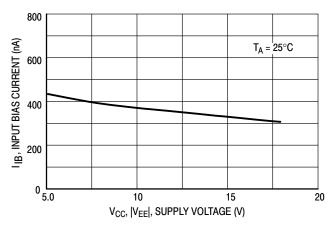


Figure 3. Input Bias Current versus Supply Voltage

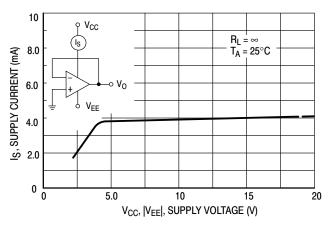


Figure 4. Supply Current versus Supply Voltage

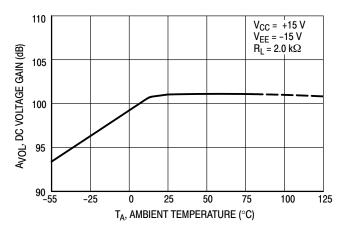


Figure 5. DC Voltage Gain versus Temperature

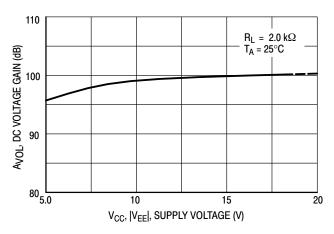


Figure 6. DC Voltage Gain versus Supply Voltage

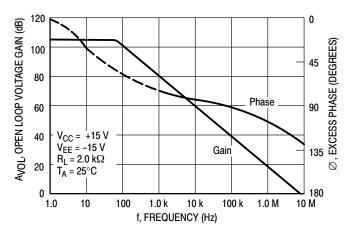


Figure 7. Open Loop Voltage Gain and Phase versus Frequency

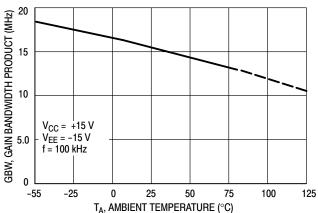


Figure 8. Gain Bandwidth Product versus Temperature

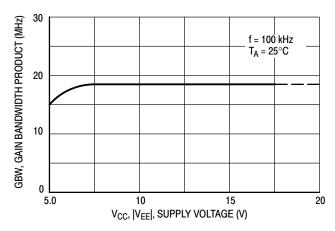


Figure 9. Gain Bandwidth Product versus Supply Voltage

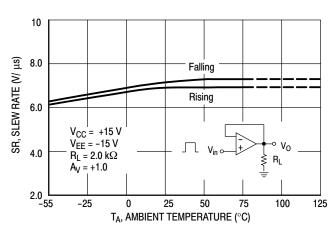


Figure 10. Slew Rate versus Temperature

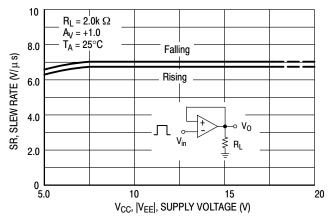


Figure 11. Slew Rate versus Supply Voltage

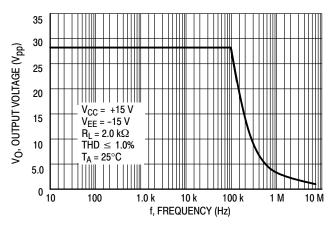


Figure 12. Output Voltage versus Frequency

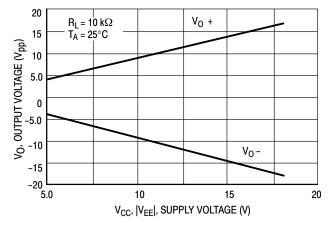


Figure 13. Maximum Output Voltage versus Supply Voltage

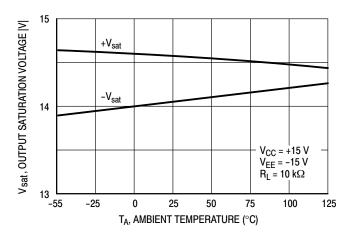


Figure 14. Output Saturation Voltage versus Temperature

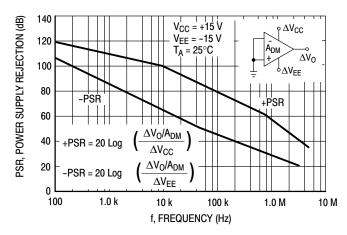


Figure 15. Power Supply Rejection versus Frequency

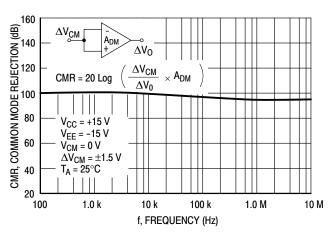


Figure 16. Common Mode Rejection versus Frequency

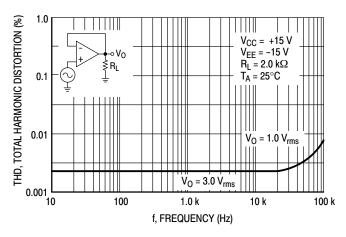


Figure 17. Total Harmonic Distortion versus Frequency

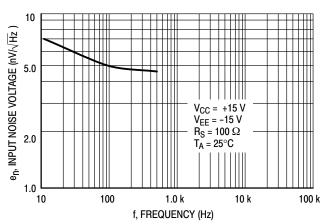


Figure 18. Input Referred Noise Voltage versus Frequency

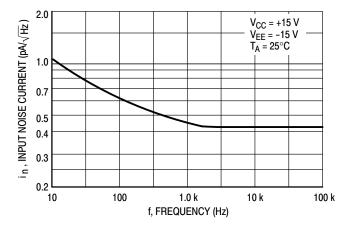


Figure 19. Input Referred Noise Current versus Frequency

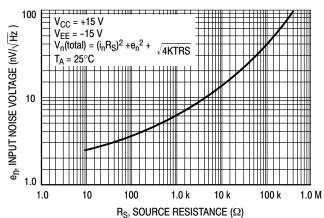


Figure 20. Input Referred Noise Voltage versus Source Resistance

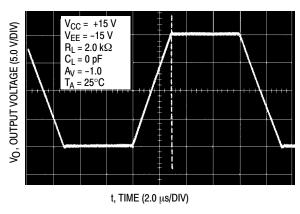


Figure 21. Inverting Amplifier

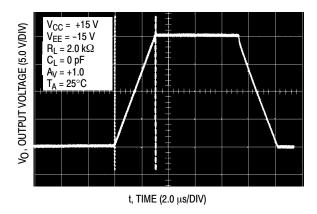


Figure 22. Noninverting Amplifier Slew Rate

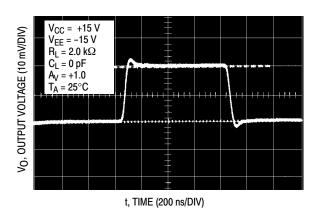


Figure 23. Noninverting Amplifier Overshoot

ORDERING INFORMATION

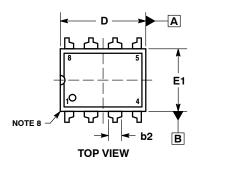
Device	Package	Shipping [†]
LM833NG	PDIP-8 (Pb-Free)	50 Units / Rail
LM833DG	SOIC-8 (Pb-Free)	98 Units / Rail
LM833DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NCV833DR2G*	SOIC-8 (Pb-Free)	2500 / Tape & Reel

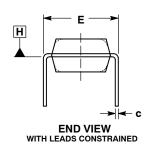
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}NCV prefix indicates qualified for automotive use.

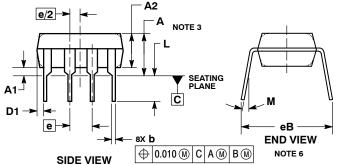
PACKAGE DIMENSIONS

PDIP-8 **N SUFFIX** CASE 626-05 **ISSUE M**









NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
 4. DIMENSIONS D, D1 AND E1 DO NOTINCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
 5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATIM C

- PLANE H WITH THE LEADS CONSTRAINED FETH ENGINEER.

 6. DIMENSION OF IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.

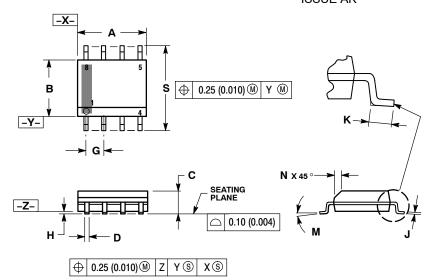
 7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.

 8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE COPINERS) CORNERS).

	INCHES		MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α		0.210		5.33
A1	0.015		0.38	
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
С	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005		0.13	
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
е	0.100 BSC		2.54 BSC	
eB		0.430		10.92
L	0.115	0.150	2.92	3.81
M		10°		10°

PACKAGE DIMENSIONS

SOIC-8 **D SUFFIX** CASE 751-07 **ISSUE AK**

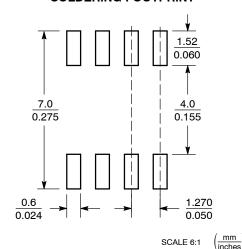


NOTES

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE
- PENDENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.80	5.00	0.189	0.197	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.053	0.069	
D	0.33	0.51	0.013	0.020	
G	1.27	1.27 BSC		0 BSC	
Н	0.10	0.25	0.004	0.010	
J	0.19	0.25	0.007	0.010	
K	0.40	1.27	0.016	0.050	
М	0 °	8 °	0 °	8 °	
N	0.25	0.50	0.010	0.020	
S	5.80	6.20	0.228	0.244	

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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IS31AP4996-GRLS2-TR STPA002OD-4WX NCP2823BFCT1G MAX9717DETA+T MAX9717CETA+T MAX9724AEBC+TG45

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