LMV821, LMV824

Single and Quad Low Voltage, Rail-to-Rail Operational Amplifiers

The LMV821 and LMV824 are operational amplifiers with low input voltage offset and drift vs. temperature. In spite of low quiescent current requirements these devices have 5 MHz bandwidth and 1.4 V/μs slew rate. In addition they provide rail−to−rail output swing into 600 Ω loads. The input common−mode voltage range includes ground, and the maximum input offset voltage is only 3.5 mV. Substantially large capacitive loads can be driven by simply adding a pullup resistor or isolation resistor.

The LMV821 (single) is available in a space−saving SC70−5 while the quad comes in SOIC and TSSOP packages.

Features

- Low Offset Voltage: 3.5 mV
- Very low Offset Drift: 1.0 μV/°C
- High Bandwidth: 5 MHz
- Rail−to−Rail Output Swing into a 600 Ω load
- Capable of driving highly capacitive loads
- Small Packages:
  - LMV821 in SC−70
  - LMV824 in SOIC−14 and TSSOP−14
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Notebook Computers
- PDAs
- Modem Transmitter/ Receivers

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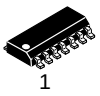
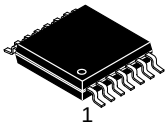
SC−70
CASE 419A



SOIC−14
CASE 751A



TSSOP−14
CASE 948G

ORDERING AND MARKING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 2 of this data sheet.

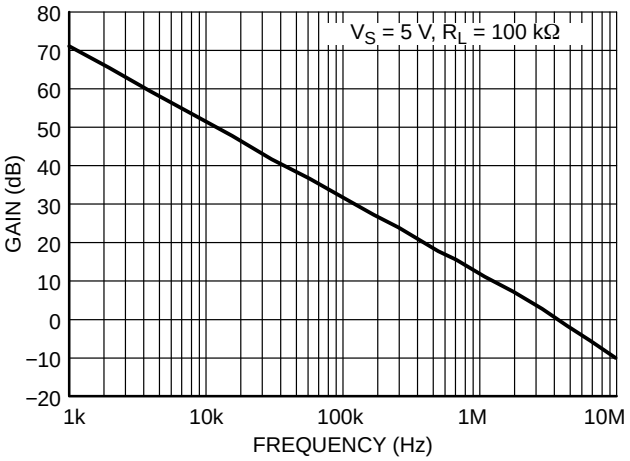


Figure 1. Gain vs. Frequency

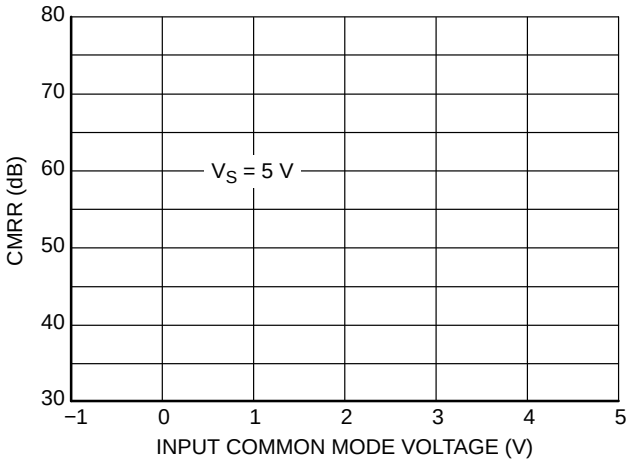
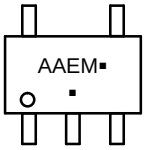


Figure 2. CMRR vs. Input Common Mode Voltage

MARKING DIAGRAMS

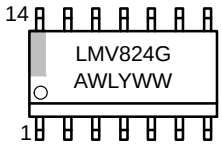
SC−70



AAE = Specific Device Code
M = Date Code
▪ = Pb−Free Package

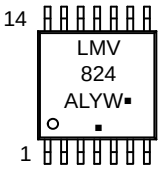
(Note: Microdot may be in either location)

SOIC−14



LMV824 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

TSSOP−14

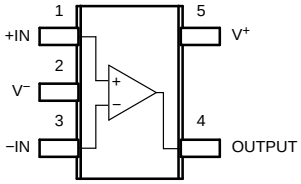


LMV824 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

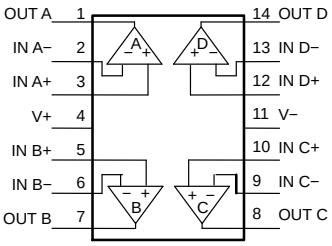
PIN CONNECTIONS

SC70−5



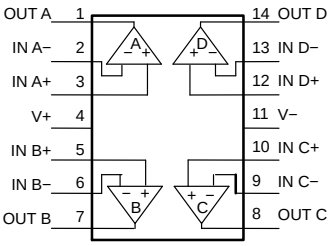
(Top View)

SOIC−14



(Top View)

TSSOP−14



(Top View)

ORDERING INFORMATION

Order Number	Number of Channels	Specific Device Marking	Package Type	Shipping†
LMV821SQ3T2G	Single	AAE	SC−70 (Pb−Free)	3000 / Tape & Reel
LMV824DR2G	Quad	LMV824	SOIC−14 (Pb−Free)	2500 / Tape & Reel
LMV824DTBR2G	Quad	LMV 824	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_S	Supply Voltage (Operating Range V_S = 2.7 V to 5.5 V)	5.5	V
V_{IDR}	Input Differential Voltage	± Supply Voltage	V
V_{ICR}	Input Common Mode Voltage Range	−0.5 to (V+) +0.5	V
	Maximum Input Current	10	mA
t_{SO}	Output Short Circuit (Note 1)	Continuous	
T_J	Maximum Junction Temperature (Operating Range −40°C to 85°C)	150	°C
θ_{JA}	Thermal Resistance		°C/W
	SC−70	280	
	SOIC−14	156	
	TSSOP−14	190	
T_{STG}	Storage Temperature	−65 to 150	°C
	Mounting Temperature (Infrared or Convection − 20 sec)	235	°C
V_{ESD}	ESD Tolerance Machine Model Human Body Model	200 2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Continuous short−circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability. Shorting output to either V+ or V− will adversely affect reliability.

2.7V DC ELECTRICAL CHARACTERISTICS Unless otherwise noted, all min/max limits are guaranteed for T_A = 25°C, V+ = 2.7 V, V− = 0 V, V_{CM} = V+/2, V_O = V+/2 and R_L > 1 MΩ. Typical specifications represent the most likely parametric norm. Min/Max specifications are guaranteed by testing, characterization, or statistical analysis.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}			1	3.5	mV
		T_A = −40°C to +85°C			4	
Input Offset Voltage Average Drift	TCV_{OS}			1		μV/°C
Input Bias Current	I_B			105	210	nA
		T_A = −40°C to +85°C			315	
Input Offset Current	I_{IO}			0.5	30	nA
		T_A = −40°C to +85°C			50	
Common−Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 1.7 V	70	85		dB
		T_A = −40°C to +85°C	68			
Power Supply Rejection Ratio	PSRR	1.5 V ≤ V+ ≤ 4 V, V − = −1 V, V_O = 0 V, V_{CM} = 0.0 V	75	85		dB
		T_A = −40°C to +85°C	70			
Input Common−Mode Voltage Range	V_{CM}	For CMRR ≥ 53 dB and T_A = −40°C to +85°C	−0.2	−0.3 to 2.0	1.9	V
Large Signal Voltage Gain	AV	R_L = 600 Ω, V_O = 0.5 V to 2.5 V	80	95		dB
		T_A = −40°C to +85°C	70			
		R_L = 2 kΩ, V_O = 0.5 V to 2.5 V	83	89		
		T_A = −40°C to +85°C	80			
Output Swing	V_{OH}	R_L = 600 Ω to 1.35 V	2.5	2.58		V
		T_A = −40°C to +85°C	2.4			
	V_{OL}	R_L = 600 Ω to 1.35 V		0.13	0.21	
		T_A = −40°C to +85°C			0.3	
	V_{OH}	R_L = 2 kΩ to 1.35 V	2.6	2.66		
		T_A = −40°C to +85°C	2.5			
	V_{OL}	R_L = 2 kΩ to 1.35 V		0.08	0.12	
		T_A = −40°C to +85°C			0.2	
Output Current	I_O	Sourcing, V_O = 0 V	12			mA
		Sinking, V_O = 2.7 V	12	26		
Supply Current	I_{CC}	LMV821 (Single)		0.242	0.3	mA
		T_A = −40°C to +85°C			0.5	
		LMV824 (All Four Channels)		1	1.3	
		T_A = −40°C to +85°C			1.5	

2.5V DC ELECTRICAL CHARACTERISTICS Unless otherwise noted, all min/max limits are guaranteed for T_A = 25°C, V+ = 2.5 V, V− = 0 V, V_{CM} = V+/2, V_O = V+/2 and R_L > 1 MΩ. Typical specifications represent the most likely parametric norm. Min/Max specifications are guaranteed by testing, characterization, or statistical analysis.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	T_A = −40°C to +85°C		1	3.5	mV
					4	
Output Swing	V_{OH}	R_L = 600 Ω to 1.25 V	2.3	2.37		V
		T_A = −40°C to +85°C	2.2			
	V_{OL}	R_L = 600 Ω to 1.25 V		0.13	0.20	
		T_A = −40°C to +85°C			0.3	
	V_{OH}	R_L = 2 kΩ to 1.25 V	2.4	2.46		
		T_A = −40°C to +85°C	2.3			
	V_{OL}	R_L = 2 kΩ to 1.25 V		0.08	0.12	
		T_A = −40°C to +85°C			0.20	

2.7V AC ELECTRICAL CHARACTERISTICS Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V+ = 2.7 V, V− = 0 V, V_{CM} = 1.0 V, V_O = V+/2 and RL > 1 MΩ. Typical specifications represent the most likely parametric norm. Min/Max specifications are guaranteed by testing, characterization, or statistical analysis.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Slew Rate	SR	(Note 2)		1.5		V/uS
Gain Bandwidth Product	GBWP			5		MHz
Phase Margin	θ_m			55		°
Gain Margin	G_m			12.9		dB
Input−Referred Voltage Noise	e_n	f = 1 kHz, V_{CM} = 1 V		12		nV/$\sqrt{Hz}$
Input−Referred Current Noise	i_n	f = 1kHz		0.2		pA/$\sqrt{Hz}$
Total Harmonic Distortion	THD	f = 1 kHz, AV = −2, R_L = 10 kΩ , V_O = 1.8 V_{PP}		0.023		%
Amplifier−to−Amplifier Isolation		(Note 3)		135		dB

2. Connected as voltage follower with input step from 0.5 V to 1.5 V. Number specified is the average of the positive and negative slew rates.
3. Input referred, R_L = 100 kΩ connected to V+/2. Each amp excited in turn with 1kHz to produce V_O = 3 V_{PP}. For Supply Voltages < 3 V, V_O = V+.

5V DC ELECTRICAL CHARACTERISTICS Unless otherwise noted, all min/max limits are guaranteed for T_A = 25°C, V+ = 5 V,V− = 0 V, VCM = V+/2, V_O = V+/2 and R_L > 1 MΩ. Typical specifications represent the most likely parametric norm. Min/Max specifications are guaranteed by testing, characterization, or statistical analysis.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}			1	3.5	mV
		T_A = −40°C to +85°C			4	
Input Offset Voltage Average Drift	TCV_{OS}			1		μV/°C
Input Bias Current	I_B			119	245	nA
		T_A = −40°C to +85°C			380	
Input Offset Current	I_{IO}			0.5	30	nA
		T_A = −40°C to +85°C			50	
Common−Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 4.0 V	72	90		dB
		T_A = −40°C to +85°C	70			
Power Supply Rejection Ratio	PSRR	1.7 V ≤ V+ ≤ 4 V, V − = 1 V, V_O = 0 V, V_{CM} = 0.0 V	75	85		dB
		T_A = −40°C to +85°C	70			
Input Common−Mode Voltage Range	V_{CM}	For CMRR ≥ 58 dB and T_A = − 40°C to +85°C	−0.2	−0.2 to 4.3	4.2	V
Large Signal Voltage Gain	A_V	R_L = 600 Ω, V_O = 1.0 V to 4.0 V	87	100		dB
		T_A = −40°C to +85°C	73			
		R_L = 2 kΩ, V_O = 1.0 V to 4.0 V	84	99		
		T_A = −40°C to +85°C	82			
Output Swing	V_{OH}	R_L = 600 Ω to 2.5 V	4.75	4.84		V
		T_A = −40°C to +85°C	4.7			
	V_{OL}	R_L = 600 Ω to 2.5 V		0.17	0.33	
		T_A = −40°C to +85°C			0.4	
	V_{OH}	RL = 2 kΩ to 2.5 V	4.85	4.9		
		T_A = −40°C to +85°C	4.8			
	V_{OL}	R_L = 2 kΩ to 2.5 V		0.1	0.15	
		T_A = −40°C to +85°C			0.2	
Output Current	I_O	Sourcing, Vo = 0 V	20	45		mA
		T_A = −40°C to +85°C	10			
		Sinking, Vo = 5 V	20	40		
		T_A = −40°C to +85°C	15			
Supply Current	I_{CC}			0.3	0.4	mA
		T_A = −40°C to +85°C			0.6	
		LMV822 (Both Applications)		0.5	0.7	
		T_A = −40°C to +85°C			0.9	
		LMV824 (All Four Applications)		1	1.3	
		T_A = −40°C to +85°C			1.5	

5V AC ELECTRICAL CHARACTERISTICS Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V+ = 5 V, V− = 0 V, V_{CM} = 2.0 V, V_O = V+/2 and R_L > 1 MΩ. Typical specifications represent the most likely parametric norm. Min/Max specifications are guaranteed by testing, characterization, or statistical analysis.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Slew Rate	SR	(Note 4)		2		V/μS
Gain Bandwidth Product	GBWP			5.6		MHz
Phase Margin	θ_m			63		°
Gain Margin	G_m			11.7		dB
Input−Referred Voltage Noise	e_n	f = 1 kHz, V_{CM} = 1 V		11		nV/$\sqrt{Hz}$
Input−Referred Current Noise	i_n	f = 1 kHz		0.21		pA/$\sqrt{Hz}$
Total Harmonic Distortion	THD	f = 1 kHz, A_V = −2, R_L = 10 kΩ , V_O = 4.11 VPP		0.012		%
Amplifier−to−Amplifier Isolation		(Note 5)		135		dB

4. Connected as voltage follower with input step from 0.5 V to 3.5 V. Number specified is the average of the positive and negative slew rates.
5. Input referred, R_L = 100 kΩ connected to V+/2. Each amp excited in turn with 1 kHz to produce V_O = 3 V_{PP}. (For Supply Voltages < 3 V, V_O = V+).

TYPICAL PERFORMANCE CHARACTERISTICS

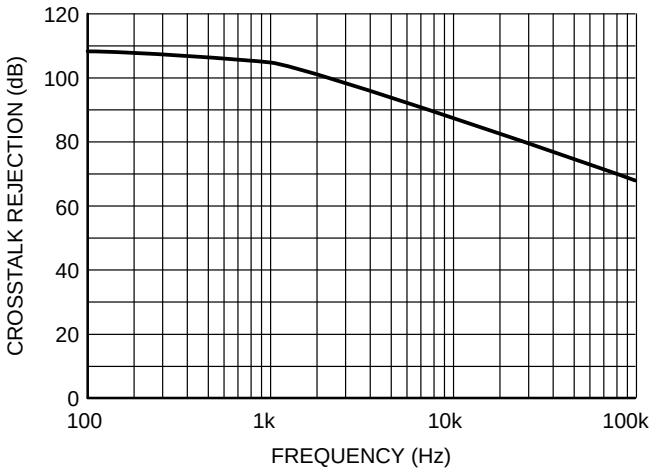


Figure 3. Crosstalk Rejection vs. Frequency

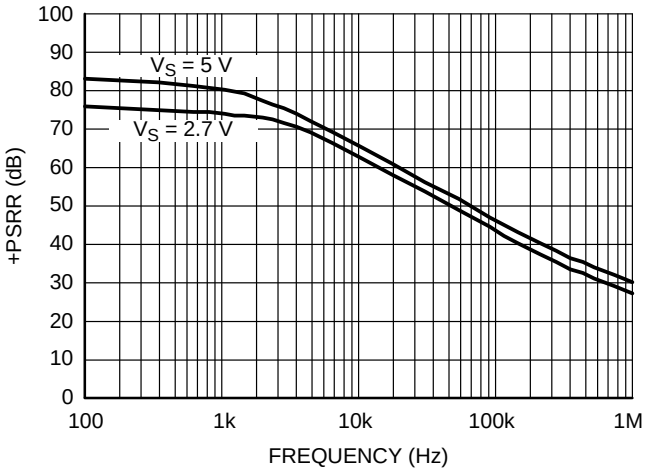


Figure 4. +PSRR vs. Frequency

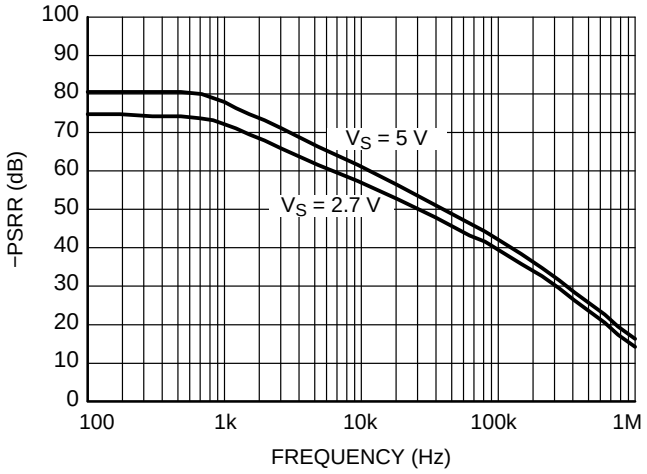


Figure 5. −PSRR vs. Frequency

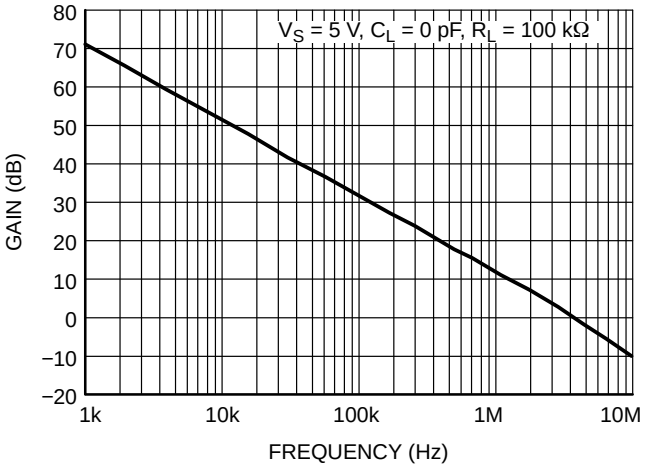


Figure 6. Gain vs. Frequency

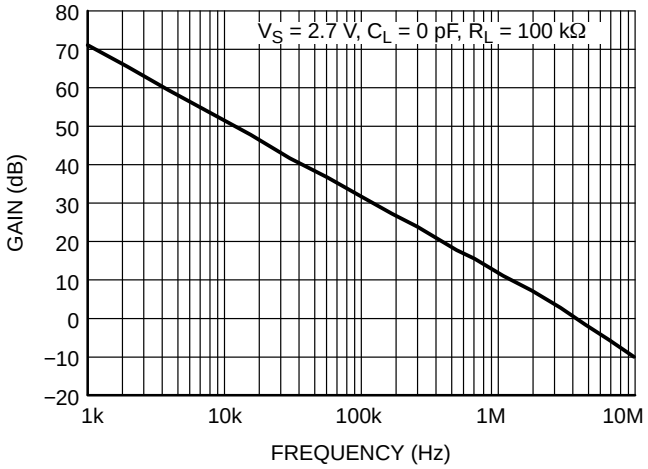


Figure 7. Gain vs. Frequency

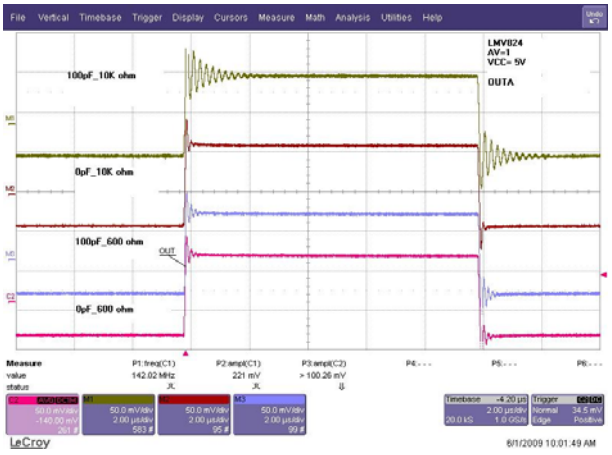


Figure 8. Non−Inverting Stability vs. Capacitive Load

TYPICAL PERFORMANCE CHARACTERISTICS

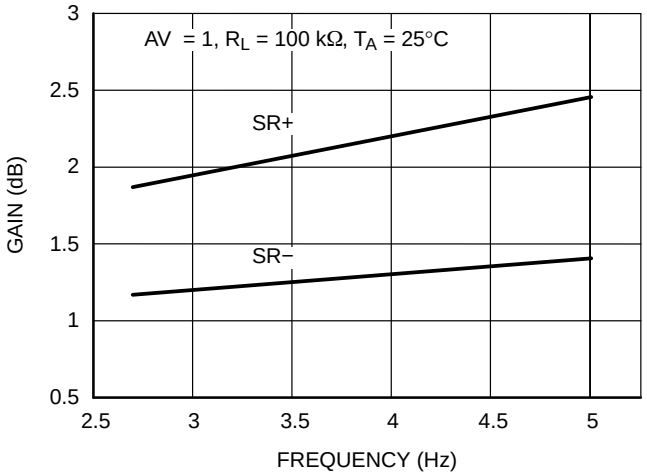


Figure 9. Gain vs. Frequency

Figure 10. Non−Inverting Large Signal Step Response

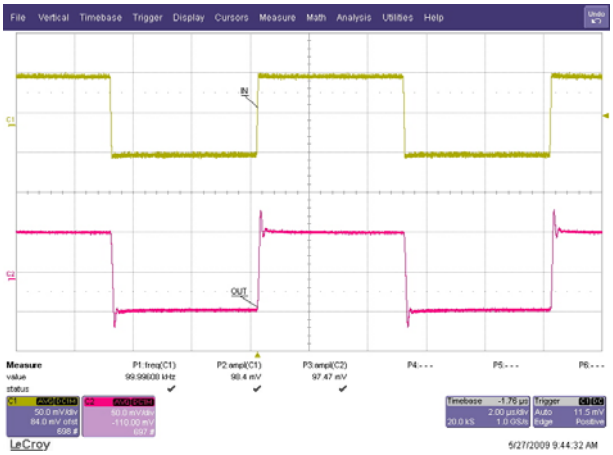


Figure 11. Non−Inverting Small Signal Step Response

Figure 12. Inverting Large Signal Step Response

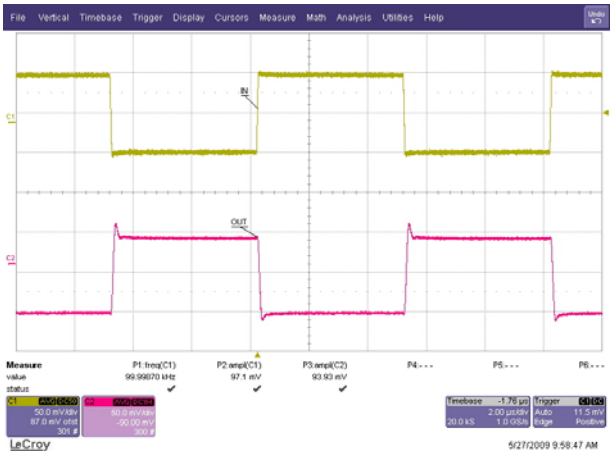


Figure 13. Inverting Small Signal Step Response

APPLICATIONS INFORMATION

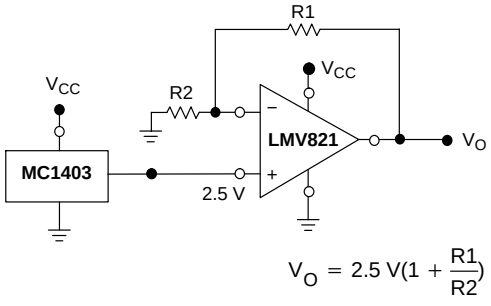


Figure 14. Voltage Reference

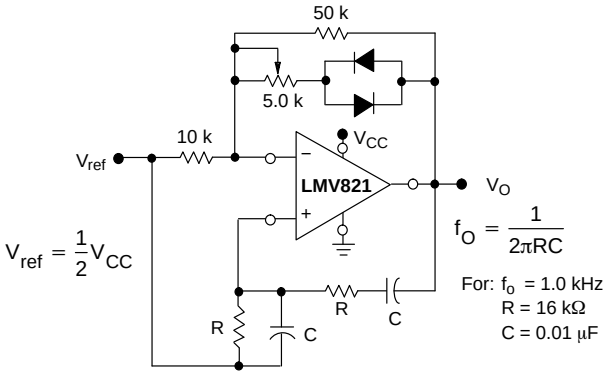
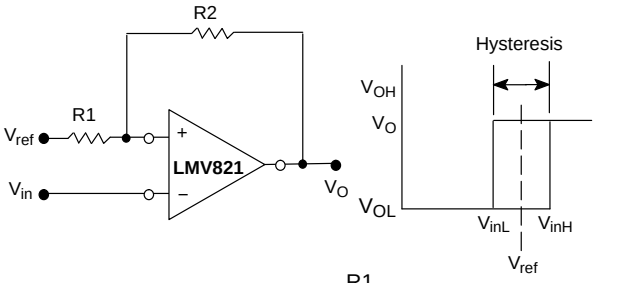


Figure 15. Wien Bridge Oscillator

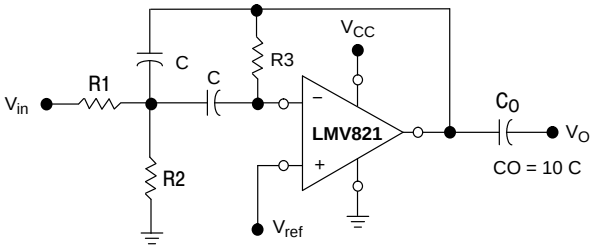


$$V_{in}L = \frac{R1}{R1 + R2}\ (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{in}H = \frac{R1}{R1 + R2}\ (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}\ (V_{OH} - V_{OL})$$

Figure 16. Comparator with Hysteresis



Given: f_o = center frequency
$A(f_o)$ = gain at center frequency

Choose value f_o, C

Then : $R3 = \frac{Q}{\pi f_O C}$

$$R1 = \frac{R3}{2\ A(f_O)}$$

$$R2 = \frac{R1\ R3}{4Q^2\ R1 - R3}$$

For less than 10% error from operational amplifier, $((Q_O\ f_O)/BW) < 0.1$ where f_o and BW are expressed in Hz. If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Figure 17. Multiple Feedback Bandpass Filter

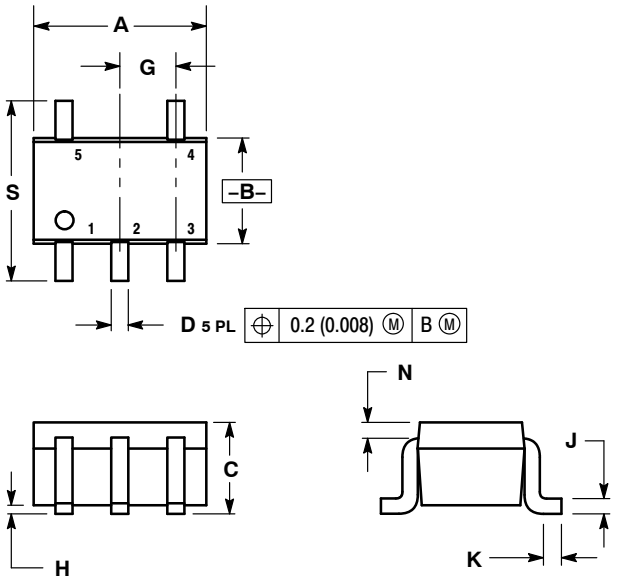
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L

SCALE 2:1

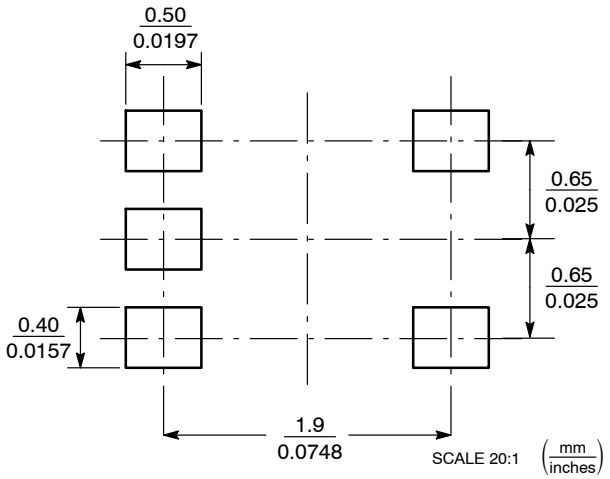
DATE 17 JAN 2013



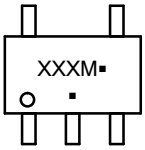
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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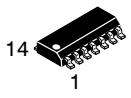
DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

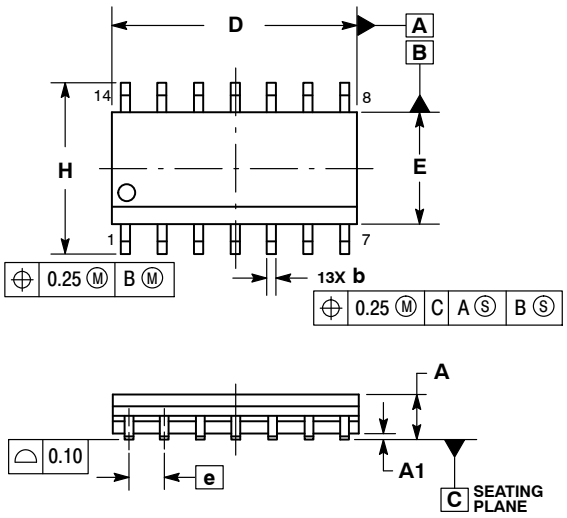
ON Semiconductor®

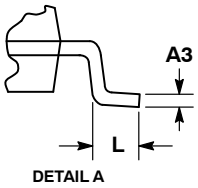


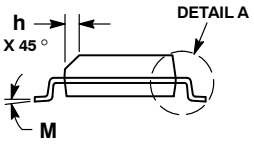
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



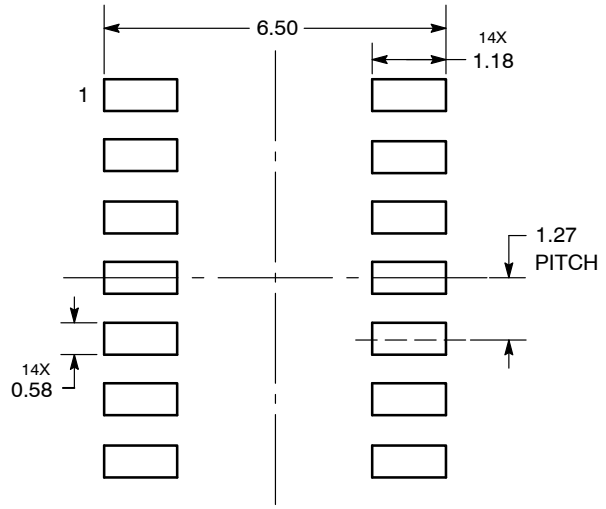




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

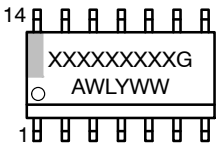
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

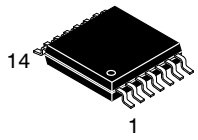
STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

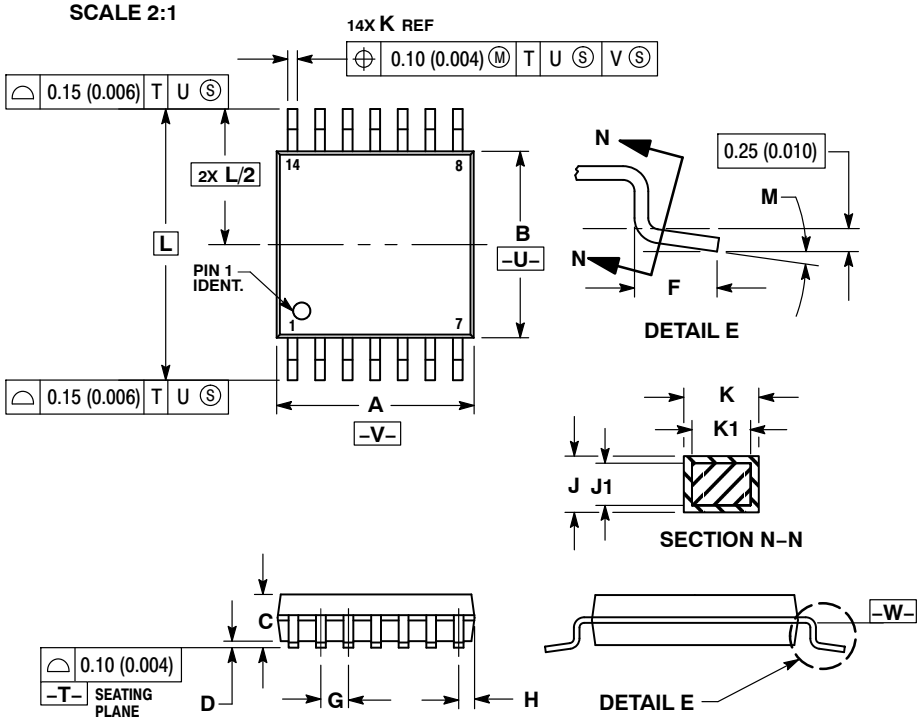
ON Semiconductor®

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



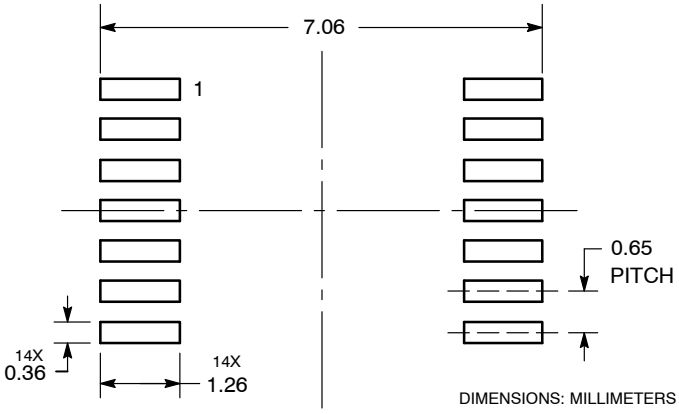
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

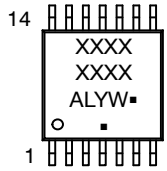
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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