Ordering number : ENA1997

LV4924VH

ON Semiconductor®

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Bi-CMOS IC

Class-D Audio power Amplifier Power cell BTL 10W×2ch

Overview

The LV4924VH is a 2-channel full-bridge driver for digital power amplifiers. It requires a PWM modulator IC in the previous stage. This IC is a power cell that takes in PWM signals as an input and is used to form a digital amplifier system for TVs, amusement equipment, and other such systems.

Features

- BTL output, class D amplifier system
- High-efficiency class D amplifier
- Muting function reduces impulse noise at power on / off
- Protection circuits incorporated for over-current, thermal, supply voltage drop, output offset detector
- Built-in bootstrap diodes

Specification

- Output 15W (V_D=16V, R_L=8Ω, f_{IN}=1kHz, AES17, THD+N=10%)
- Output 10W (V_D=13V, R_L=8Ω, f_{IN}=1kHz, AES17, THD+N=10%)
- Efficiency : 89% (V_D=13V, R_L=8Ω, f_{IN}=1kHz, P_O=10W)
- THD+N : 0.1% (V_D=13V, R_L=8Ω, f_{IN}=1kHz, P_O=1W, Filter: AES17)

Maximum Ratings / Absolute Maximum Ratings /Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_D	Externally applied voltage	22	V
Maximum PWM pin voltage	V_{IN}	PWM_A1,PWM_A2,PWM_B1,PWM_B2	6	V
Maximum pull-up pin voltage	Vpup max	NPN Open collector pin	20	V
Allowable power dissipation	Pd max	Exposed Die-pad Soldered *1	4.6	W
Maximum junction temperature	Tj max		150	°C
Operating temperature	Topr		-25 to 75	°C
Storage temperature	Tstg		-50 to 150	°C

*1 Customer bread board rev.1.0: 90.0mm × 70.0 mm × 1.6 mm (two-layer) Material: glass epoxy

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Recommended supply voltage range	V_D	Externally applied voltage	9	13	20	V
Recommended PWM pin voltage	V_{IN}	PWM_A1,PWM_A2,PWM_B1,PWM_B2	0	3.3	5	V
Recommended pull-up supply voltage	Vpup	NPN Open collector pin	-	-	18	V
Recommended load resistance	R_L	Speaker load	4	8	-	Ω

Electrical Characteristics Ta=25°C, V_D=13V, R_L=8Ω, L=22μH (TOKO: A7040HN-220M), C=0.33μF (Matsuo: 553M6302-334K)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}	$\overline{STBY}$=H, $\overline{MUTE}$=H, f_{IN}=384kHz, Duty=50%	30	38	45	mA
Current at MUTE	Imute	$\overline{STBY}$=H, $\overline{MUTE}$=L, V_{IN}=GND	2	4	6	mA
Standby current	Ist	$\overline{STBY}$=L, $\overline{MUTE}$=L, V_{IN}=GND	-	-	10	μA
H input voltage	V_IH	PWM_A, PWM_B, $\overline{STBY}$, $\overline{MUTE}$	2.3	-	5.5	V
L input voltage	V_IL	PWM_A, PWM_B, $\overline{STBY}$, $\overline{MUTE}$	0	-	1.0	V
H input current	I_IH	V_{IN}=5V	-	-	60	μA
L input current	I_IL	V_{IN}=GND	-20	-	-	μA
Output pin leakage current	IOFF	NPN Open collector output OFF-stage 5.0V pull-up	-	-	1	μA
Output pin current	IOL	NPN Open collector output ON-stage, V_{OL}=0.4V	0.5	-	-	mA
Power Tr ON resistance [*1]	Rds ON	Id=1A	-	220	-	mΩ
Turn ON delay time	td ON	f_{IN}=384kHz, Duty=50%	-	30	50	ns
Turn OFF delay time	td OFF	f_{IN}=384kHz, Duty=50%	-	30	50	ns
Rise-up time	tr	f_{IN}=384kHz, Duty=50%	-	5	20	ns
Fall time	tf	f_{IN}=384kHz, Duty=50%	-	5	20	ns

*1 : The maximum power transistor ON resistance(R_{DS}ON) is 270mΩ(design guarantee value).

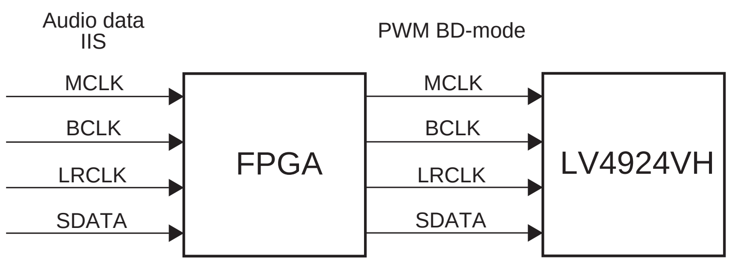
Note : The value of these characteristics were measured in Our test environment. The actual value in an end system will vary depending on the printed circuit board pattern, the components used, and other factors.

Electrical Characteristics

(Reference value: The table below shows the reference value when FPGA equivalent to the Our reference model is used.)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output 1	P_O1	THD+N=10%, f_{IN}=1kHz, AES17	-	10	-	W
Output 2	P_O2	V_D=16V, THD+N=10%, f_{IN}=1kHz, AES17	-	15	-	W
Total harmonic distortion	THD+N	P_O=1W, f_{IN} =1kHz, AES17	-	0.1	-	%

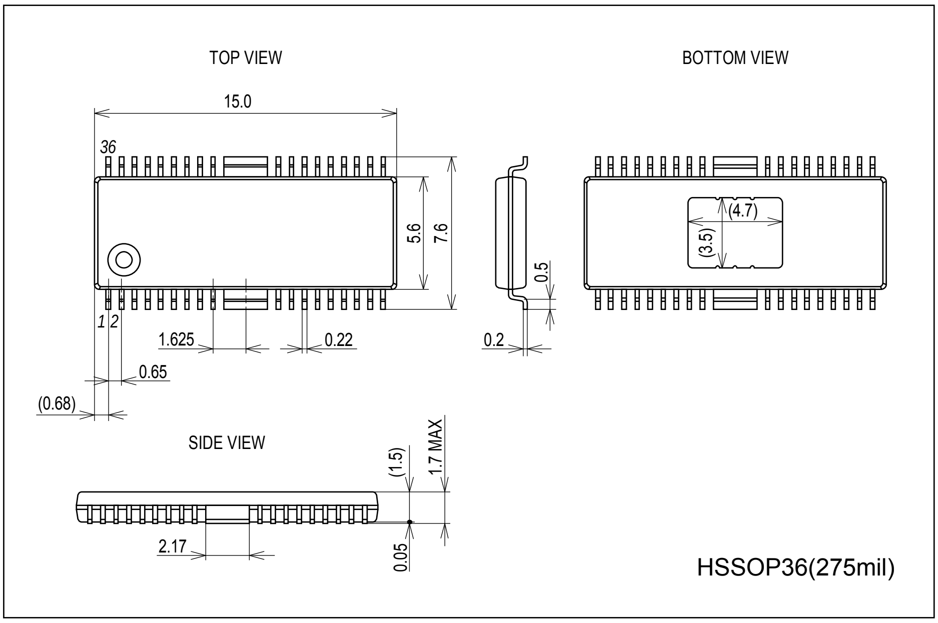
Note : The value of these characteristics were measured in Our test environment. The actual value in an end system will vary depending on the printed circuit board pattern, the components used, and other factors.



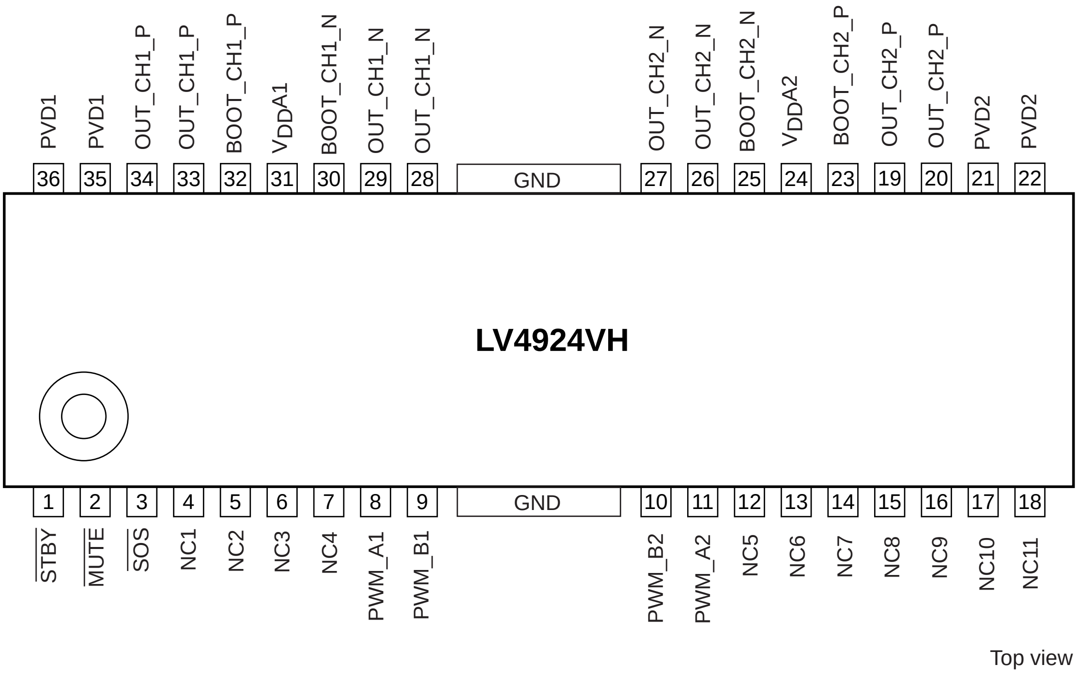
Package Dimensions

unit : mm (typ)

3417

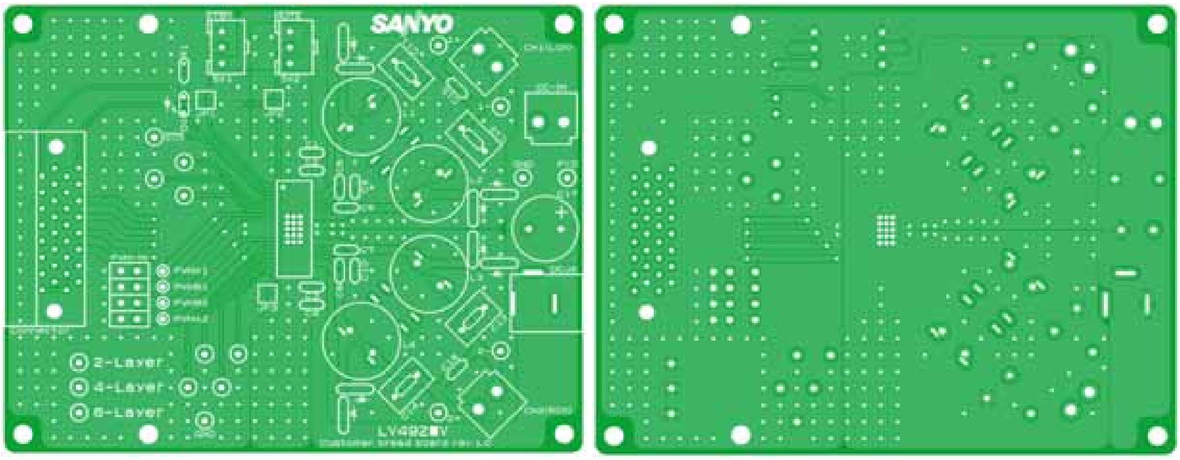


Pin Assignment



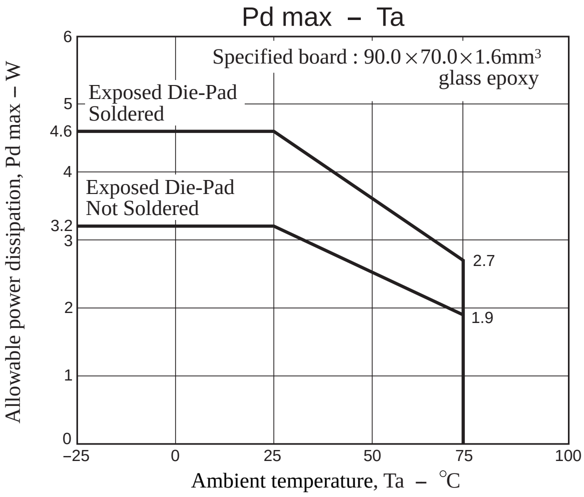
Reference data for thermal design

Overall view of substrate



Mounted on a specified board (Customer bread board rev.1.0): 90.0mm × 70.0 mm × 1.6 mm (two-layer) Material: glass epoxy

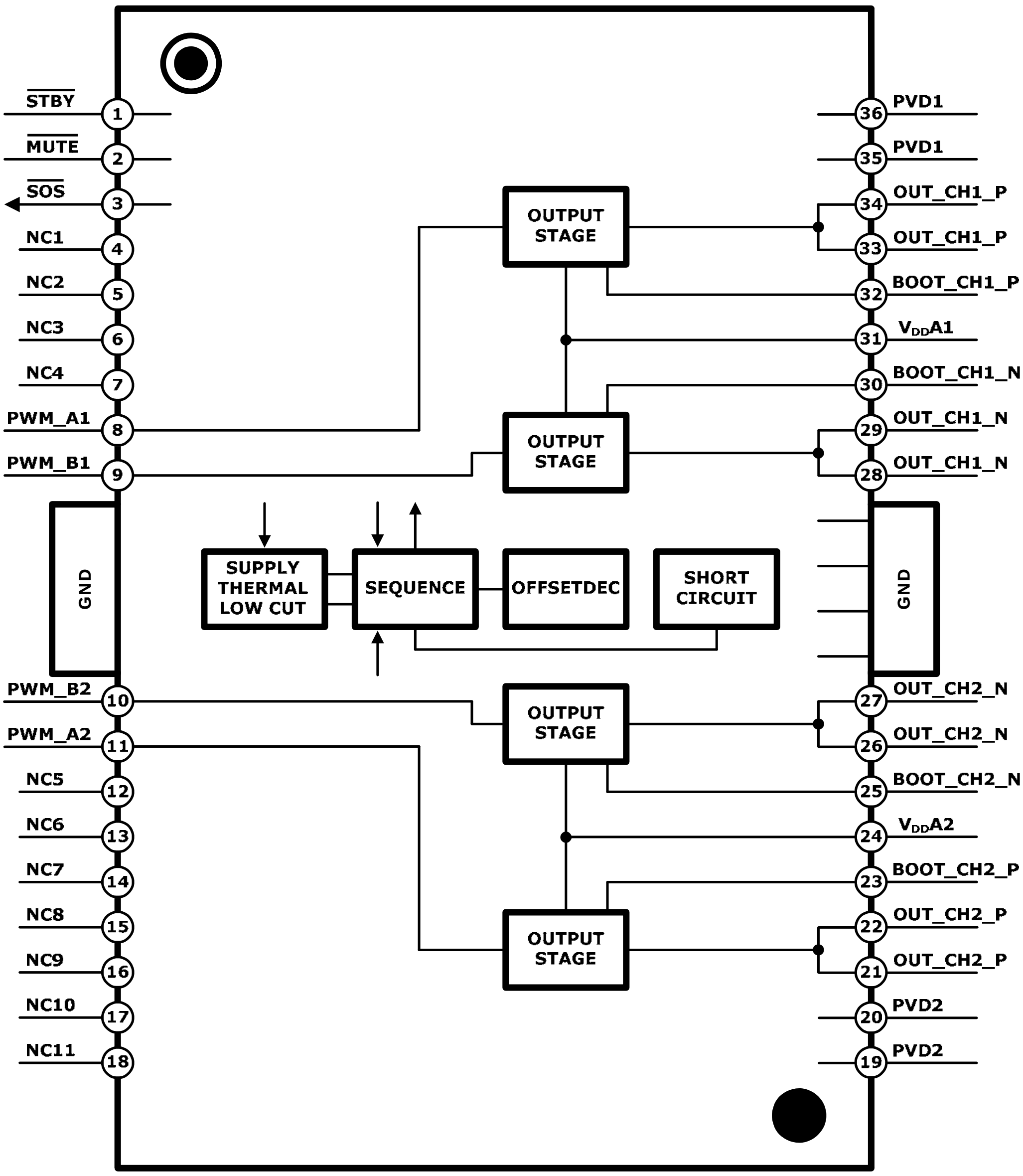
Pd max-Ta



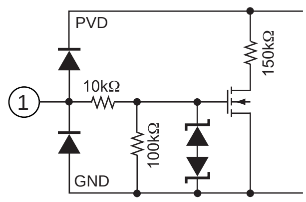
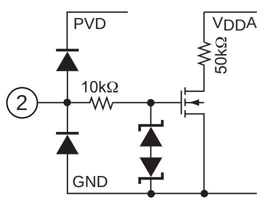
1. Data of the Exposed Die-Pad (heat spreader) substrate as mounted represents the value in the state where the exposed Die-Pad surface is wet for 90% or more.
2. For the set design, derating design should be made while ensuring allowance.
   Stresses to become an object of derating are the voltage, current, junction temperature, power loss and mechanical stresses including vibration, impact and tension.
   Accordingly, these stresses must be as low or small as possible in the design.
   Approximate targets for general derating are as follows:
   (1) Maximum value 80% or less for the voltage rating.
   (2) Maximum value 80% or less for the current rating.
   (3) Maximum value 80% or less for the temperature rating.

3. After set design, be sure to verify the design with the product.
   Also check the soldered state of the Exposed Die-Pad, etc. and verify the reliability of the soldered joint.
   If any void or deterioration is observed in these sections, thermal conduction to the substrate is deteriorated, resulting in thermal damage of IC.

Block Diagram



Pin Equivalent Circuit

Pin No.	Pin name	I/O	Description	Equivalent Circuit
1	$\overline{\text{STBY}}$	I	Standby mode control	
2	$\overline{\text{MUTE}}$	I	Muting control	

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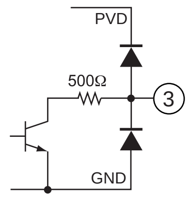
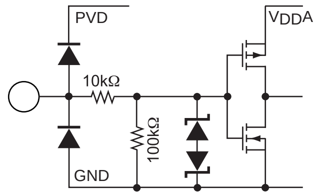
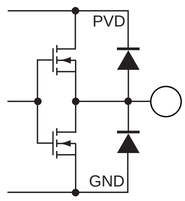
Pin No.	Pin name	I/O	Description	Equivalent Circuit
3	$\overline{SOS}$	I	Internal protection circuit detection output (OR output of the thermal detection, over-current, voltage drop protection, offset detection circuit) of an NPN open collector output type	
4 5 6 7	NC1 NC2 NC3 NC4	- - - -	Non connection Non connection Non connection Non connection	
8 9 10 11	PWM_A1 PWM_B1 PWM_B2 PWM_A2	I I I I	PWM input (plus input) of OUT_CH1_P PWM input (negative input) of OUT_CH1_N PWM input (negative input) of OUT_CH2_N PWM input (plus input) of OUT_CH2_P	
FIN	GND	-	ground	
12 13 14 15 16 17 18	NC5 NC6 NC7 NC8 NC9 NC10 NC11	- - - - - - -	Non connection Non connection Non connection Non connection Non connection Non connection Non connection	
19, 20	PVD2	-	Power pin	
21, 22 26, 27 28, 29 33, 34	OUT_CH2_P OUT_CH2_N OUT_CH1_N OUT_CH1_P	O O O O	Output pin, Channel 2 plus Output pin, Channel 2 minus Output pin, Channel 1 minus Output pin, Channel 1 plus	
23	BOOT_CH2_P	I/O	Bootstrap I / O pin, channel 2 plus	
24	$V_{DD}A2$	O	Internal power supply decoupling capacitor connection	
25	BOOT_CH2_N	I/O	Bootstrap I / O pin, channel 2 minus	
30	BOOT_CH1_N	I/O	Bootstrap I / O pin, channel 1 minus	
31	$V_{DD}A1$	O	Internal power supply decoupling capacitor connection	
32	BOOT_CH1_P	I/O	Bootstrap I / O pin, channel 1 plus	
35, 36	PVD1	-	Power pin	

Description of functions

System Standby

The built-in 5V regulator is turned ON / OFF by changing over "H" and "L" of "STBY". The regulator is turned OFF with "STBY" at "L" and ON with "STBY" at "H".
This signal also causes initialization of the internal logic initialization with "L" and the normal mode with "H".

MUTE Function

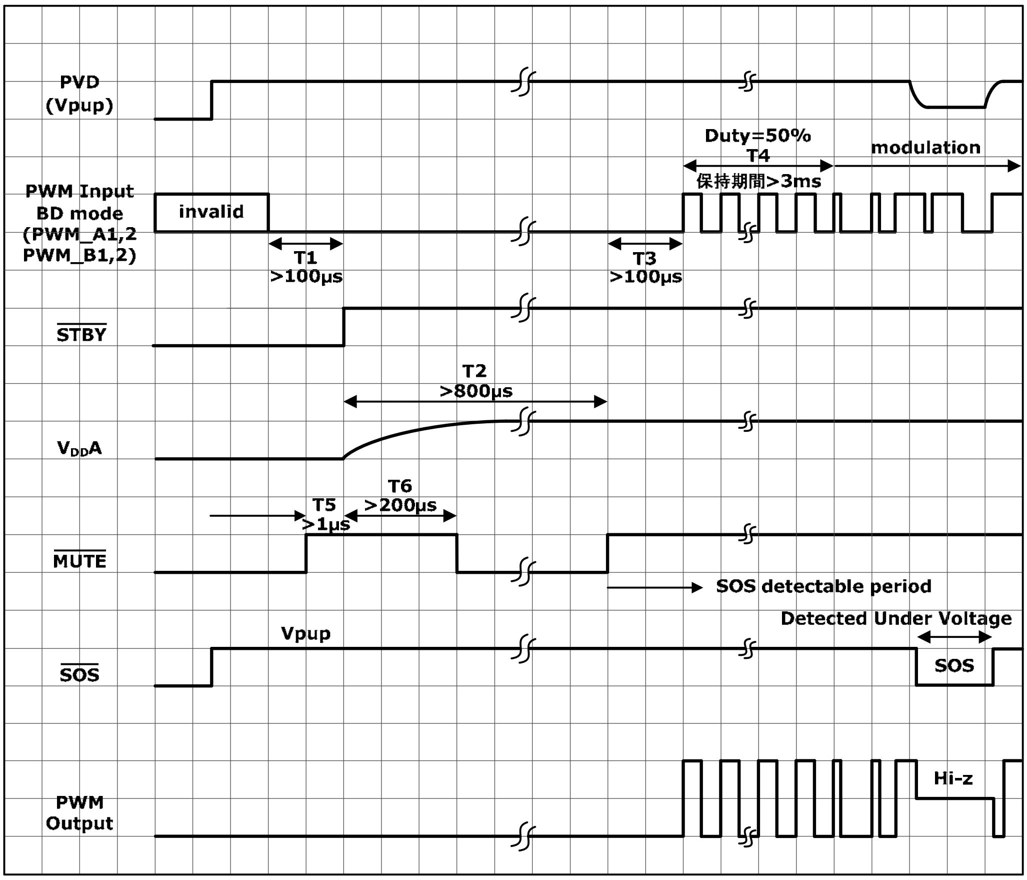
The MUTE function is mainly for muting of the output and for reduction of pop noise at power ON.

Muting the output

The output PWM can be turned ON / OFF by changing over "H" and "L" of "MUTE". The PWM output is stopped (putting all of PWM outputs at high impedance) with "MUTE" at "L" and enters the normal operation mode with "MUTE" at "H".

Sequence at power ON

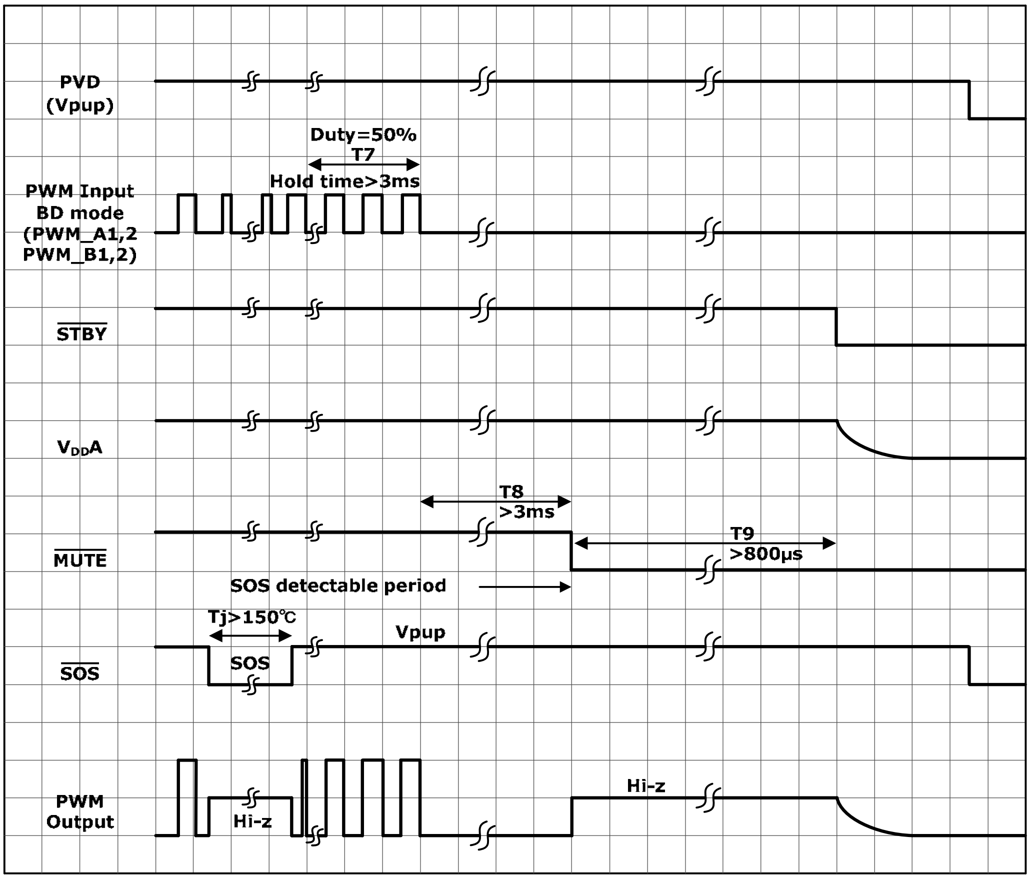
To reduce the pop noise, turn ON power supply while controlling in the following timing (PWM=BD mode).
In particular, all of inputs of PWM must be held at "L" at canceling of MUTE function.



* Please observe the following items for the destruction prevention of the output transistor.
(1) Under all conditions must control the period at the "H" level about the PWM input so as not to become more than 200μs when period of the "H" level MUTE and STBY signals both.

Sequence at power OFF

To reduce the pop noise, turn OFF power supply while controlling in the following timing (PWM=BD mode).



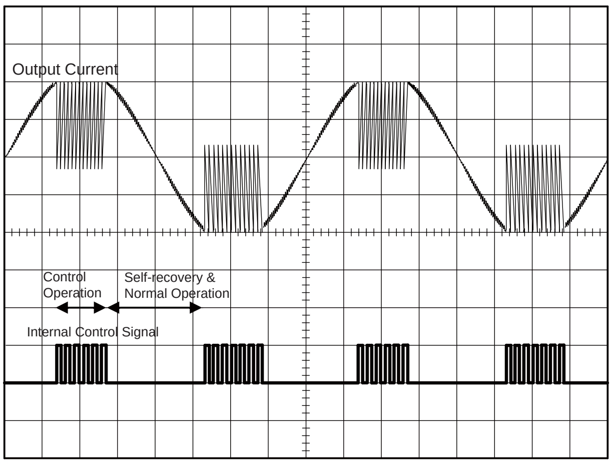
Protection Circuit

LV4924VH incorporates the over-current protection circuit, thermal protection circuit, supply voltage drop protection circuit and output offset detection protection circuit. Activation of any one of these circuits causes the $\overline{\text{SOS}}$ output pin to become active and thus "L".

Over-current protection circuit

This circuit is a protection circuit* to protect the output transistor from the over-current and compatible with any mode of lightning, ground fault, and load short-circuit.

Protection is done when the detection current value (about 6A) set inside IC is reached, forcing the output transistor to remain OFF for about 20μs. After forced OFF, the transistor returns automatically to the normal operation and performs protection again if the over-current continues to flow.



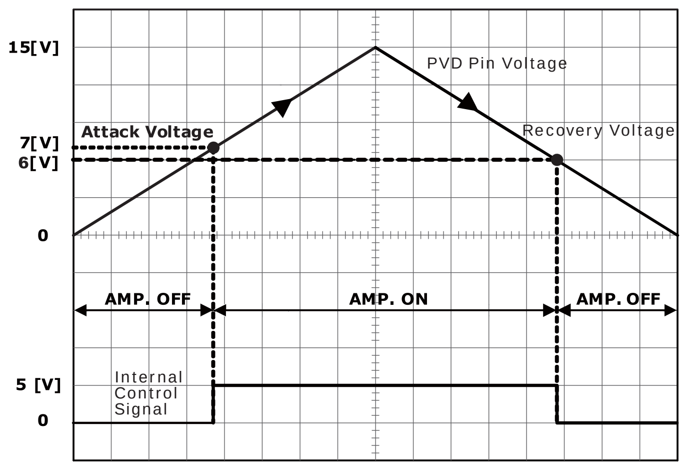
* The over-current protection circuit functions only to avoid the abnormal state, such as output short-circuit, etc., temporarily, and does not guarantee to offer the protection to prevent damage to IC.

Thermal protection circuit

This circuit detects the temperature (150°C or more) inside LSI for protection. While this protection circuit is active, the output Tr is turned OFF on both high- and low-sides, putting the output in the high-impedance state. This operation is also provided with the hysteresis.

Supply voltage drop protection circuit

To avoid unstable operation at low voltages, this circuit monitors the PVD pin voltage and turns ON the amplifier when this voltage exceeds the Attack voltage (V_D = 7V typ.). In addition, to avoid unstable operation when the PVD pin voltage has dropped because of certain reasons, the Recover voltage (V_D = 6V typ.) is set. Both Attack and Recover voltages have the hysteresis (about 1V) to prevent continuous ON / OFF operation of the supply voltage drop protection circuit.

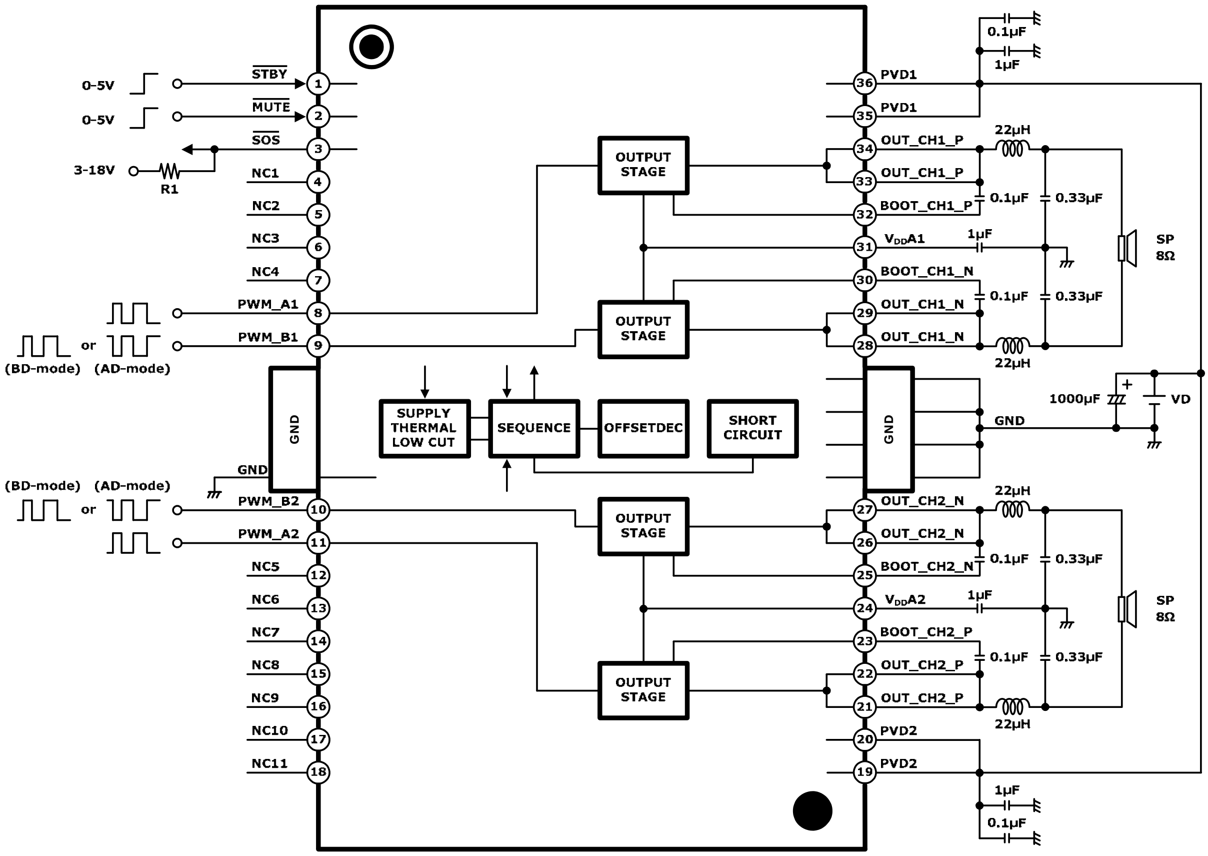


Output offset detection protection circuit

This circuit is a protection circuit intended to alleviate burn of the loudspeakers when DC outputs to the BTL output for a certain period or more.

The circuit detects the case in which each BTL input of each channel continues to disagree (for about 300ms), turns OFF the output Tr on both high- and low-sides, and puts the output in the high-impedance state.

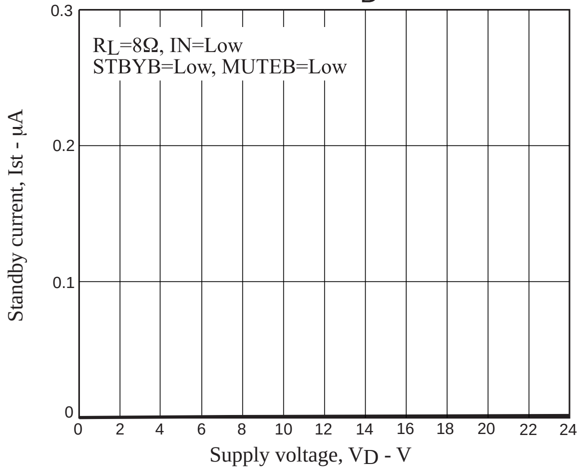
Application Circuit



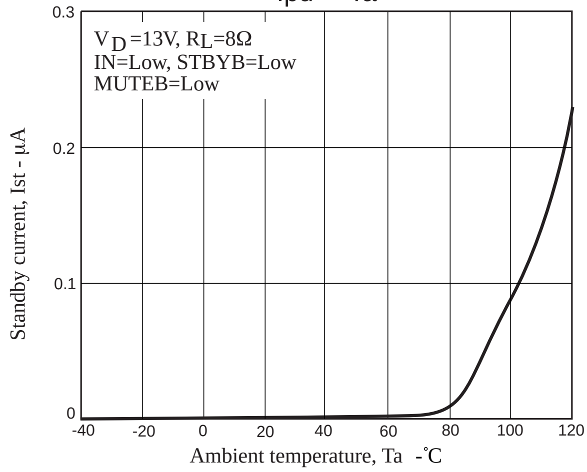
* $\overline{\text{SOS}}$ of pin 3 is the open collector output.
Therefore, to monitor this output with CPU, it is necessary to pull up (resistor: R1) at power supply of CPU, etc.
When the output is not to be used (not to be monitored), it is not necessary to pull-up the resistor.

Characteristics Data: L=22µH (TOKO: A7040HN-220M), C=0.33µF (Matsuo: 553M6302-334K)

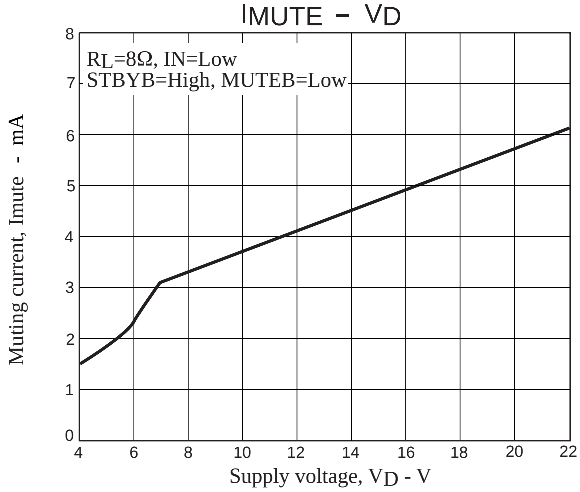
Ist – V_D



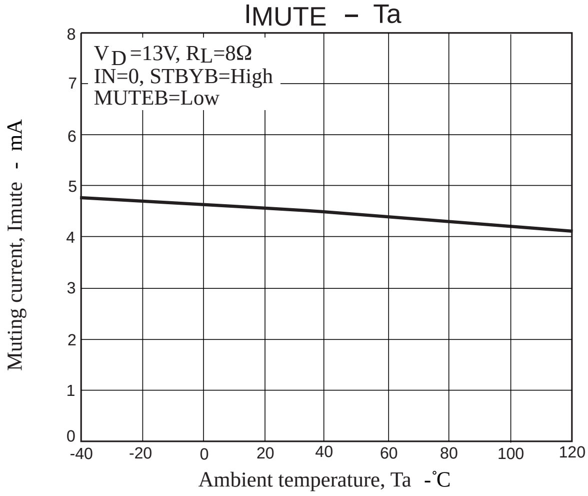
Ipd – Ta



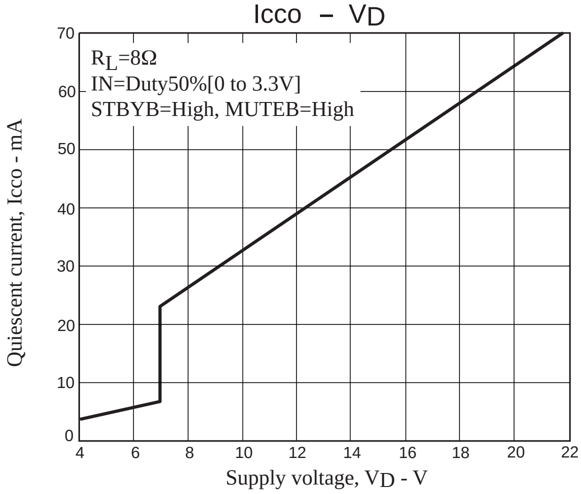
I_{MUTE} – V_D



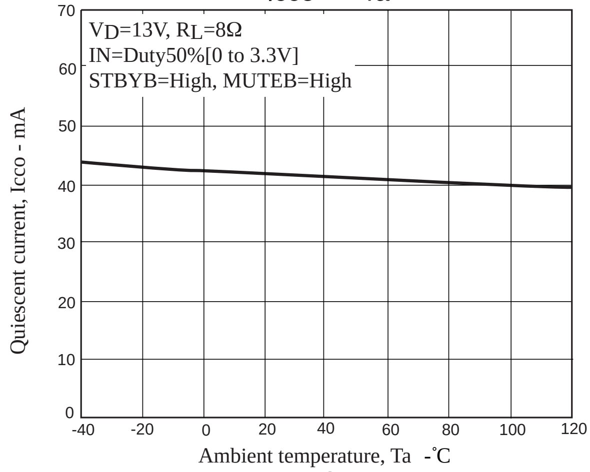
I_{MUTE} – Ta



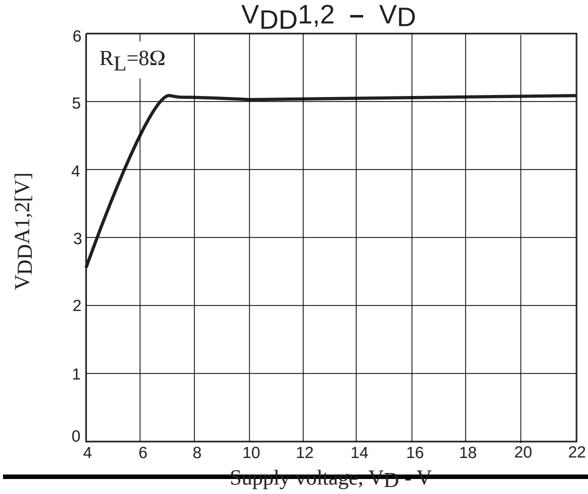
Icco – V_D



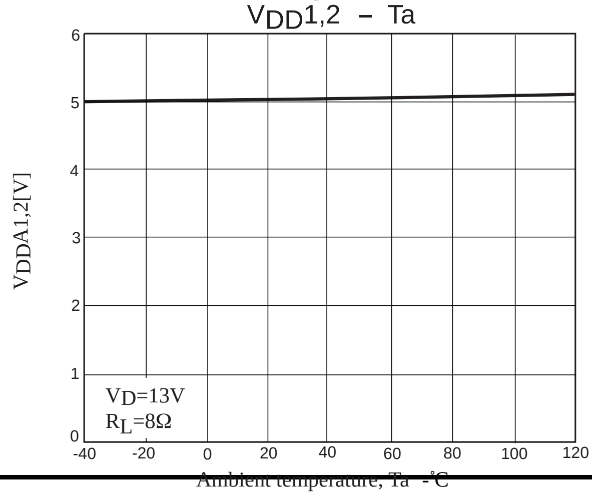
Icco – Ta



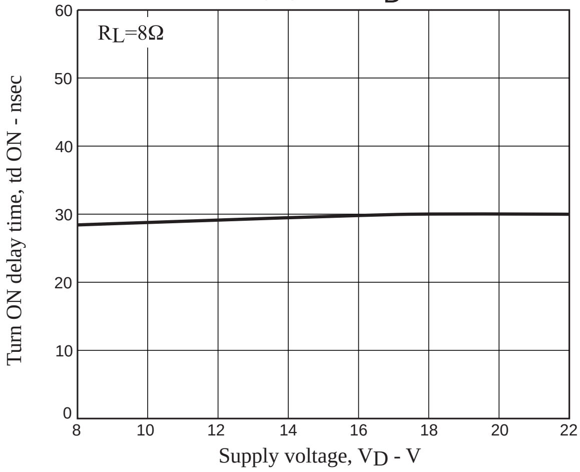
V_{DD}1,2 – V_D



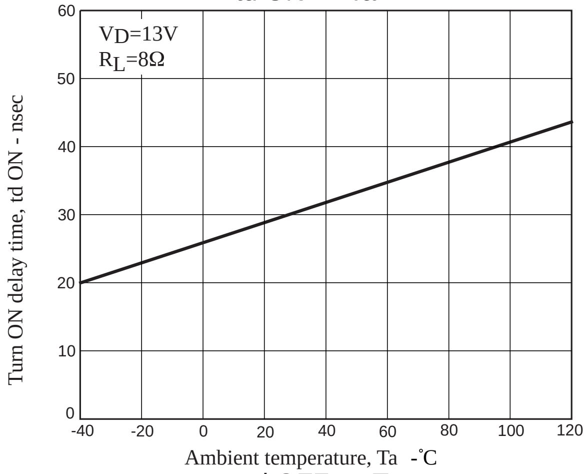
V_{DD}1,2 – Ta



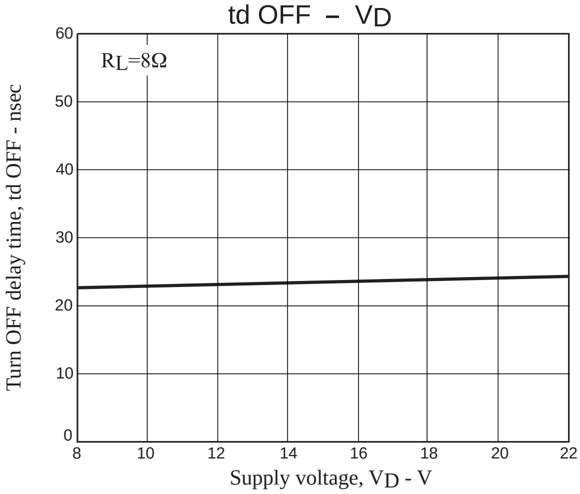
td ON – V_D



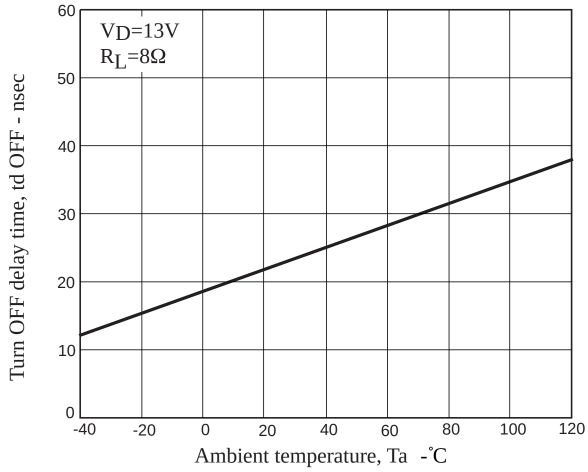
td ON – Ta



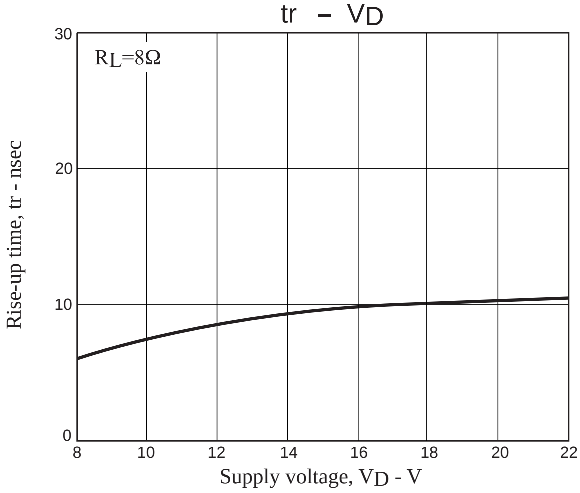
td OFF – V_D



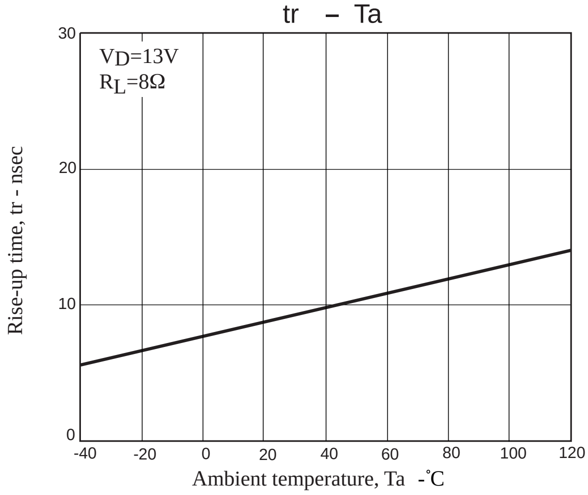
td OFF – Ta



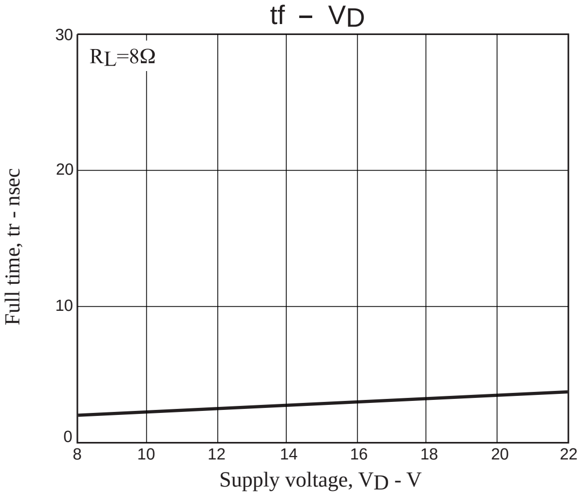
tr – V_D



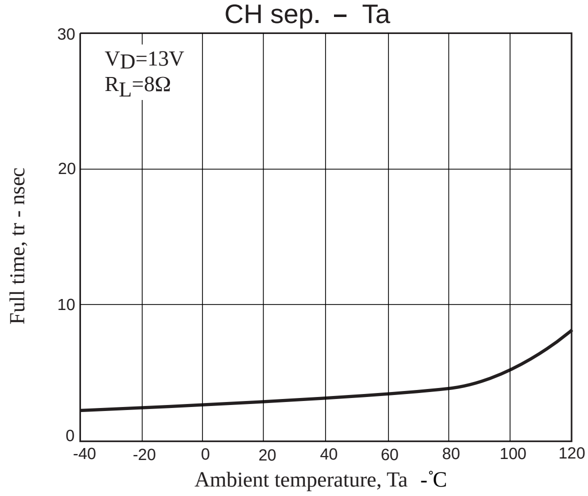
tr – Ta

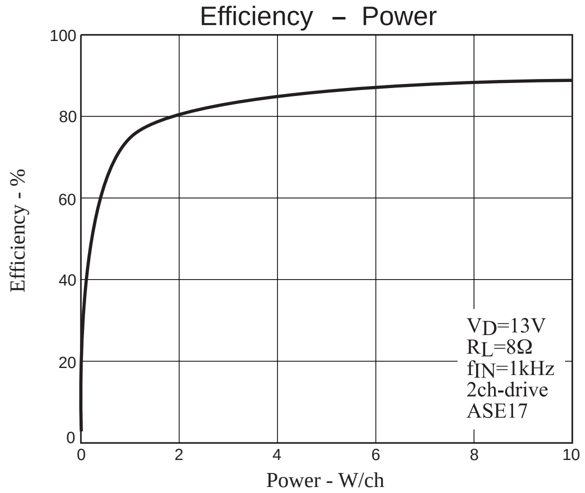


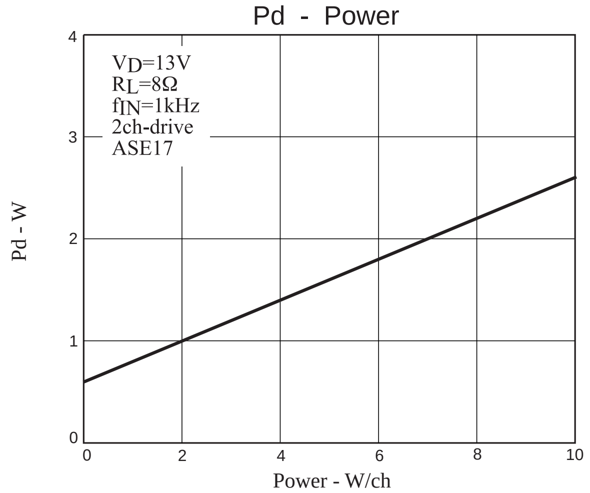
tf – V_D

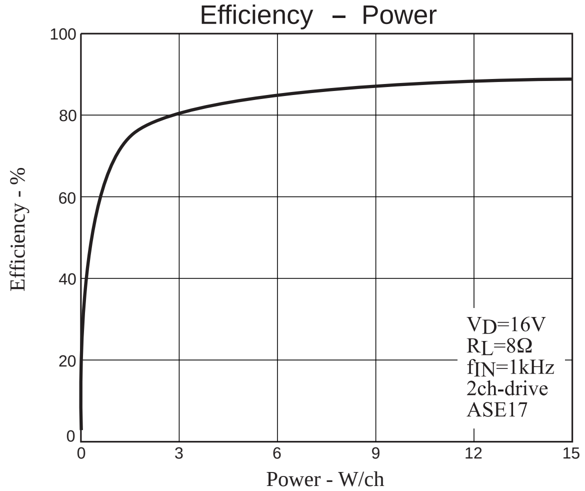


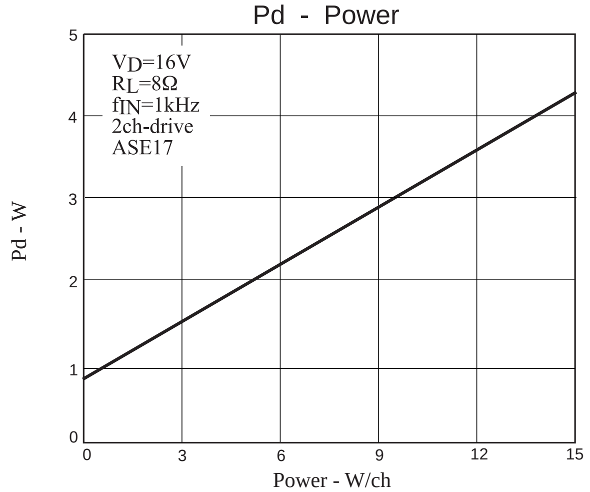
CH sep. – Ta

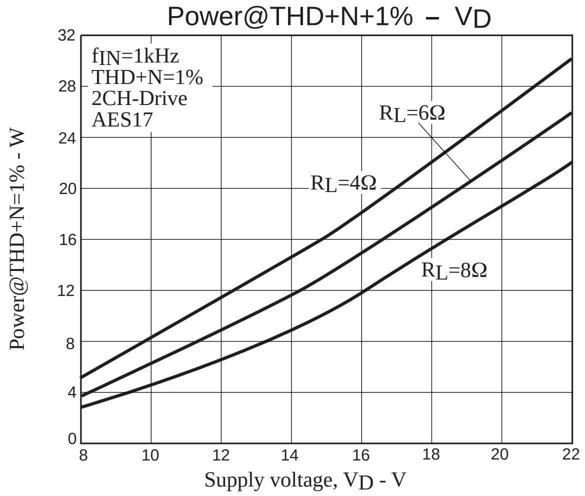


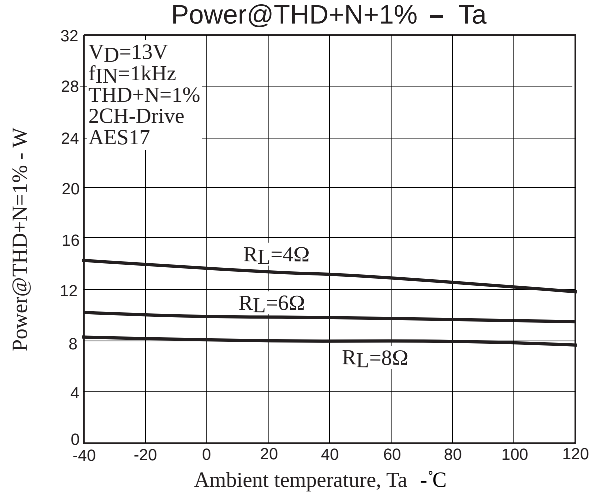

Efficiency – Power
Efficiency - %
Power - W/ch
VD=13V
RL=8Ω
fIN=1kHz
2ch-drive
ASE17

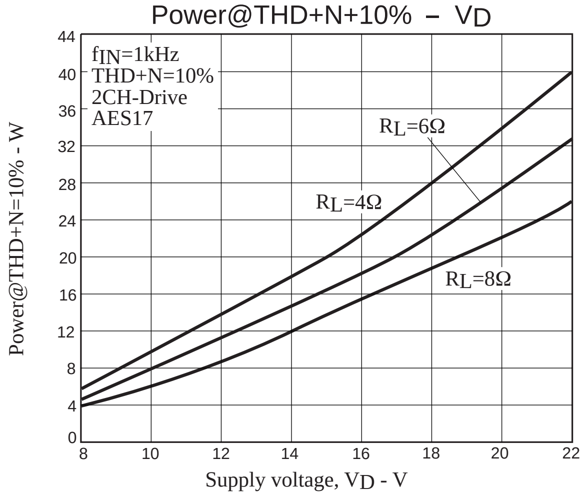

Pd - Power
Pd - W
Power - W/ch
VD=13V
RL=8Ω
fIN=1kHz
2ch-drive
ASE17

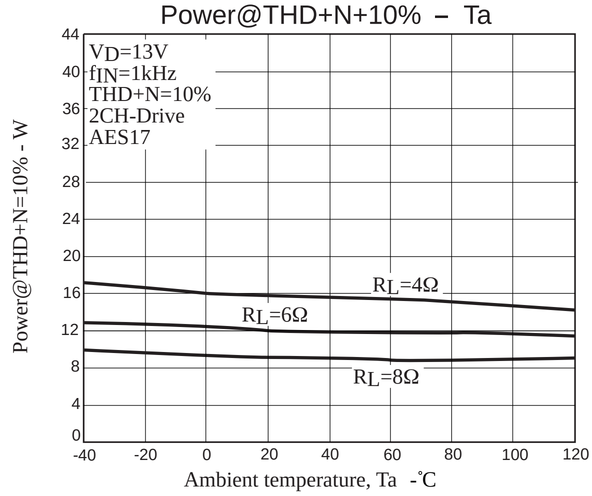

Efficiency – Power
Efficiency - %
Power - W/ch
VD=16V
RL=8Ω
fIN=1kHz
2ch-drive
ASE17


Pd - Power
Pd - W
Power - W/ch
VD=16V
RL=8Ω
fIN=1kHz
2ch-drive
ASE17

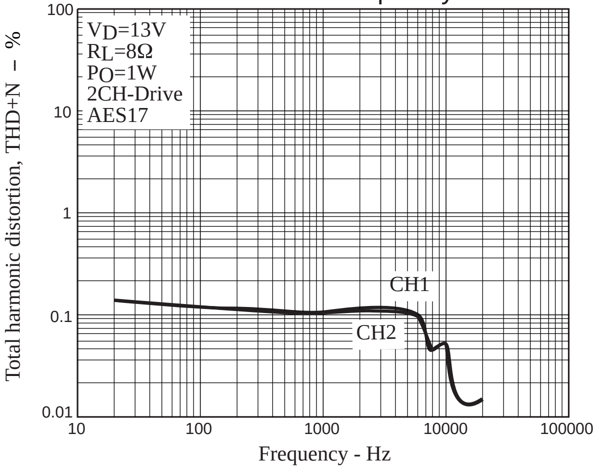

Power@THD+N+1% – VD
Power@THD+N=1% - W
Supply voltage, VD - V
fIN=1kHz
THD+N=1%
2CH-Drive
AES17
RL=6Ω
RL=4Ω
RL=8Ω


Power@THD+N+1% – Ta
Power@THD+N=1% - W
Ambient temperature, Ta -°C
VD=13V
fIN=1kHz
THD+N=1%
2CH-Drive
AES17
RL=4Ω
RL=6Ω
RL=8Ω

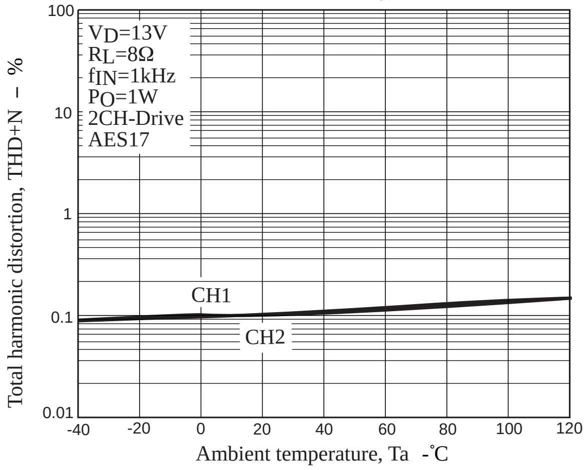

Power@THD+N+10% – VD
Power@THD+N=10% - W
Supply voltage, VD - V
fIN=1kHz
THD+N=10%
2CH-Drive
AES17
RL=6Ω
RL=4Ω
RL=8Ω


Power@THD+N+10% – Ta
Power@THD+N=10% - W
Ambient temperature, Ta -°C
VD=13V
fIN=1kHz
THD+N=10%
2CH-Drive
AES17
RL=4Ω
RL=6Ω
RL=8Ω

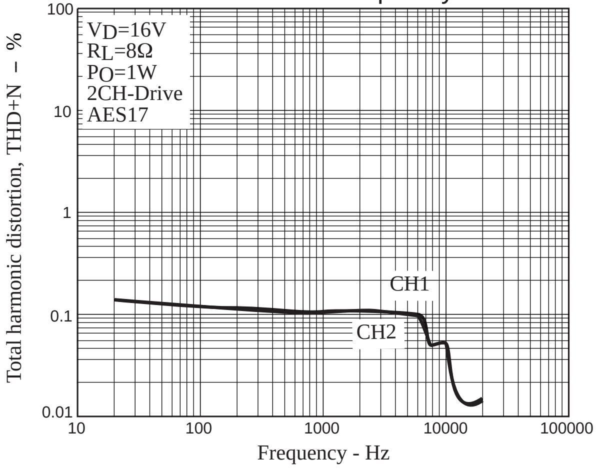
THD+N – Frequency



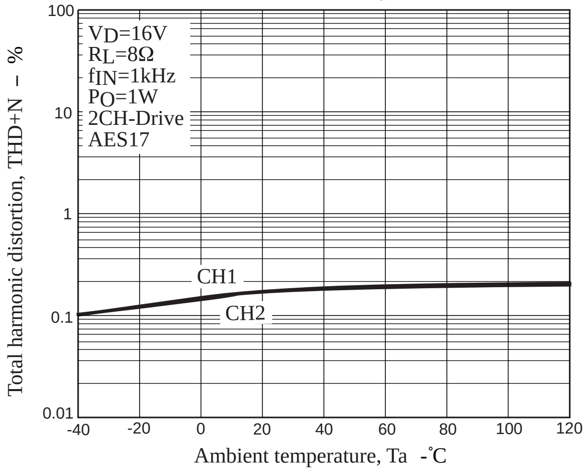
THD+N – Ta



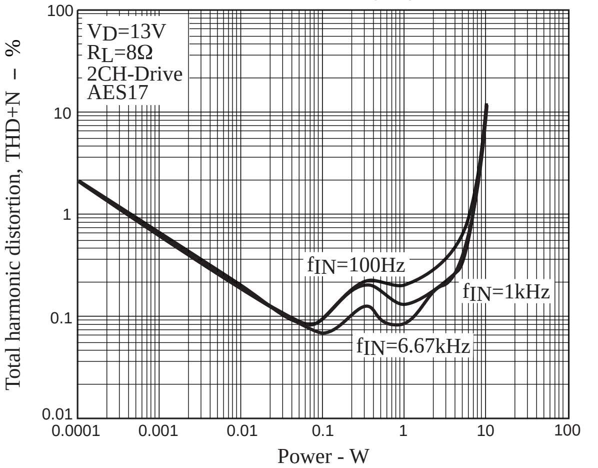
THD+N – Frequency



THD+N – Ta



THD+N – Power



THD+N – Power