LV5692P

Bi-CMOS IC

System Power Supply IC for Automotive Infotainment Multiple Output Linear Voltage Regulator

Overview

The LV5692P is a multiple output linear regulator IC, which allows reduction of quiescent current. The LV5692P is specifically designed to address automotive infotainment systems power supply requirements. The LV5692P integrates 5 linear regulator outputs, a liner regulator controller which gives USB supply with external P-channel FET, a high side power switch, over current protection, overvoltage protection and thermal shutdown circuitry.

Function

• Five channel regulator and one channel P-FET pre-driver (for USB-power)

For V_{DD}: V_{OUT} is 3.3V, I_Omax is 300mA For DSP: V_{OUT} is 3.3V, I_Omax is 300mA For CD: V_{OUT} is 8.0V, I_Omax is 1300mA For illumination: V_{OUT} is 8.4V, I_Omax is 500mA For audio systems: V_{OUT} is 8.4V, I_Omax is 500mA For USB (controller) : V_{OUT} is flexible (configurable with external resistor), I_Omax is 1000mA

HZIP15J

- and output is 0.5V, IOmax is 500mA • Over current protector
- Overvoltage protector (Without VDD-OUT) Clamp voltage is 21V (typical)
- Thermal Shut down 175°C (typical)
- Quiescent current 50µA (Typ. when only VDD is in operation)

• High side switch: Voltage difference between input

(Warning) The protector functions only improve the IC's tolerance and they do not guarantee the safety of the IC if used under the conditions out of safety range or ratings. Use of the IC such as use under over current protection range or thermal shutdown state may degrade the IC's reliability and eventually damage the IC.

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.



Specifications

Absolute Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditio	ons	Ratings	Unit
Power supply voltage	V _{CC} max			36	V
Power dissipation	Pd max	IC unit	Ta ≤ 25°C	1.5	W
		At using AI heat sink		5.6	W
		At infinity heat sink		32.5	W
Peak voltage	V _{CC} peak	Regarding Bias wave, refer to below the		50	V
Junction temperature	Tj max			150	°C
Operating temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at $Ta=25^{\circ}\mathrm{C}$

Parameter	Conditions	Ratings	Unit
Power supply voltage rating 1	V _{DD} output ON, DSP output ON	7 to 16	V
Power supply voltage rating 2	ILM output ON	10.8 to 16	V
Power supply voltage rating 3	Audio output ON, CD output ON	10 to 16	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at $Ta = 25^{\circ}C$, $V_{CC} = V_{CC}1 = 14.4V$

Devenuelar	0 sets at	Conditions	Ratings			Linit
Parameter	Symbol Conditions	min	typ	max	Unit	
Current drain	ICC	V_{DD} no load, CTRL1/2/3 = $\lceil L/L/L \rfloor$		50	100	μA
CTRL1 Input						
Low input voltage	V _{IL} 1		0		0.3	V
Middle input voltage	V _{IM} 1		1.1	1.65	2.1	V
High input voltage	V _{IH} 1		2.5		5.5	V
Input impedance	R _{IH} 1		280	400	520	kΩ
CTRL2 Input						
Low input voltage	V _{IL} 2		0		0.3	V
Middle1 input voltage	V _{IM1} 2		0.8	1.06	1.4	V
Middle2 input voltage	V _{IM2} 2		1.9	2.13	2.4	V
High input voltage	V _{IH} 2		2.9	3.2	5.5	V
Input impedance	R _{IH} 2		280	400	520	kΩ
CTRL3 input.						
Low input voltage	V _{IL} 3		0		0.3	V
High input voltage	V _{IH} 3		2.5		5.5	V
Input impedance	R _{IH} 3		280	400	520	kΩ
V _{DD} 3.3V output						
Output voltage	V _O 1	I _O 1 = 200mA	3.16	3.3	3.45	V
Output current	I _O 1	$V_0 1 \ge 3.1 V$	300			mA
Line regulation	∆V _{OLN} 1	$7.5V < V_{CC}1 < 16V, \ I_O1$ = 200mA		30	100	mV
Load regulation	ΔV_{OLD} 1	$1mA < I_{O}1 < 200mA$		70	150	mV
Ripple rejection	R _{REJ} 1	f = 120Hz, I _O 1 = 200mA	30	40		dB
USB output: CTRL3 = $[H]$ (When external power FET 2SJ650, it external resists 27k Ω , and 9.1k Ω is set)						
USB output voltage	V _O 2	I _O 2 = 1000mA	4.75	5	5.25	V
USB output current	I _O 2	$V_0 2 \ge 4.75 V$	1000			mA
Line regulation	ΔV_{OLN}^2	$10V < V_{CC} < 16V, I_O2$ = 1000mA		50	90	mV
Load regulation	∆V _{OLD} 2	$10mA < I_{O}2 < 1000mA$		100	150	mV
Dropout voltage	V _{DROP} 2	I _O 2 = 1000mA		1.0	1.5	V
Ripple rejection	R _{REJ} 1	f = 120Hz, I _O 2 = 1000mA	40	50		dB

Continued on next page.

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Parameter Symbol Conditions Ratings Main Main Main Main Main Main AUDIO (6.4V) Output ; CTRL1 = [W or H] max max max max max AUDIO output voltage 1 V ₀ 3 $[0_3 = 400mA$ 8.0 8.4 8.8 V. AUDIO output current $[0_3$ $[0_3 = 400mA$ 6.0 3.0 9.0 max Line regulation Δ^V_{OLN} 3 $10V < V_{CC} < 16V, I_0^3 = 400mA$ 0.0 0.0 100 Dropout voltage 1 V_{DROP3} $[0_3 = 400mA$ 0.0 0.0 0.0 0.0 Dropout voltage 2 V_{DROP3} $[0_3 = 400mA$ 0.0 0.0 0.0 0.0 ILM duptu voltage 1 V_{DROP3} $[0_3 = 400mA$ 0.0 0.0 0.0 0.0 0.0 ILM duptu voltage 1 V_{DROP4} $[0_4 = 400mA$ 0.0 0.0 0.0 0.0 0.0 ILM duptu voltage 1 V_{OLV4} $[0.8 + 200mA] 0.0 0.0 0.0 $	Continued from preceding page.						
Hammedia Optimize Control of Mathematical Stress min typ max Other AUDIO (84.V) Output; CTRL1 = $[M + I]$ I/Q3 = 400mA 8.0 8.4 8.8 V AUDIO output current I/Q3 I/Q3 = 8.0V 600 min mV AUDIO output current I/Q3 10V < VC_C < 16V, I/Q3 = 400mA	Parameter	Symbol	Conditions	Ratings			Linit
AUDIO (8.4V) Output ; CTRL1 = $[M \circ J]$ VQ3 IQ3 = 400mA 8.0 8.4 8.8 V AUDIO output current IQ3 VQ3 ≥ 8.0V 500 mA Line regulation $\Delta V_{QL}3$ 10V < $V_{CC} < 16V, I_Q3 = 400mA$ 0.0 90 mV Load regulation $\Delta V_{QL}3$ 1mA < I_Q3 < 400mA	Faranieter	Conditions		min	typ	max	Onit
AUDIO output voltage 1 VQ3 IQ3 = 400mA 8.0 8.4 8.8 V AUDIO output current IQ3 VQ3 ≥ 8.0V 500 mA Line regulation ΔV_{QLN3} 10V < V_CC < 16V, IQ3 = 400mA	AUDIO (8.4V) Output ; CTRL1 =	M or H					
AUDIO output current 1_0^3 $V_O 3 \ge 8.0V$ 500 (mA) Line regulation $\Delta V_O LN^3$ $100 < V_{CC} < 16V, 1_0 3 = 400mA$ (mA) (mA) Load regulation $\Delta V_O LD^3$ $1mA < 1_0 3 < 400mA$ (mA) (mV) Dropout voltage 1 $V_D RO p^3$ $1_0 3 = 400mA$ (mA) (mA) (mA) Dropout voltage 2 $V_D RO p^3$ $1_0 3 = 400mA$ (mA) (mA) (mA) Ripple rejection $R_{RE,J3}$ f = 120Hz, $1_0 3 = 400mA$ (mA) (mB) (mB) Line regulation $R_{RE,J3}$ f = 120Hz, $1_0 3 = 400mA$ (mB) (mA) (mB) Line regulation $R_{RE,J4}$ $I_0 4 = 400mA$ (mB) (mA) (mA) Line regulation ΔV_{DLN4} $10.8V < V_{CC} < 16V, 1_0 4 = 400mA$ (mO) (mB) (mA) Load regulation ΔV_{DLN4} $10.8V < V_{CC} < 16V, 1_0 4 = 400mA$ (mO) (mB) (mA) Load regulation ΔV_{DLM4} $10.8V < V_{CC} < 16V, 1_0 4 = 400mA$ (mO) (mO) (mB)	AUDIO output voltage 1	V _O 3	I _O 3 = 400mA	8.0	8.4	8.8	V
Line regulation ΔV_{OLN}^3 $10V < V_{CC} < 16V, I_O^3 = 400mA$ 30 90 mV Load regulation ΔV_{OLD}^3 $1mA < I_O^3 < 400mA$ mV Dropout voltage 1 V_{DROP}^3 $I_O^3 = 400mA$ 0.0 Dropout voltage 2 V_{DROP}^3 $I_G^3 = 200mA$ <td< td=""><td>AUDIO output current</td><td>I_O3</td><td>$V_O3 \ge 8.0V$</td><td>500</td><td></td><td></td><td>mA</td></td<>	AUDIO output current	I _O 3	$V_O3 \ge 8.0V$	500			mA
Load regulation $\Delta V_{OLD}3$ ImA < $l_O3 < 400mA$ () () () () Dropout voltage 1 $V_{DRO}3$ $l_O3 = 400mA$ () () () () Dropout voltage 2 $V_{DRO}3$ $l_G3 = 200mA$ () () () () Ripple rejection R _{REJ} 3 f = 120Hz, $l_O3 = 400mA$ () () () () ILM (4.V) Output; CTRL2 = [MI + H] I () () () () () () ILM (0.4V) Output; CTRL2 = [MI + H] I ()	Line regulation	$\Delta V_{OLN}3$	$10V < V_{CC} < 16V, \ I_O3$ = 400mA		30	90	mV
Dropout voltage 1 V_{DROPA} I_{O3} = 400mA 0.4 0.8 V Dropout voltage 2 V_{DROPA^3} I_{O3} = 200mA 0.2 0.4 V Ripple rejection R_REJ3 f = 120H2, I_{O3} = 400mA 40 50 dB LLM (84V) Output ; CTRL2 = [M + H] dB LLM output voltage VQ4 IQ4 = 400mA 8.0 8.4 8.8 V Llen regulation ΔV_{OLN4} 10.8V < V_{CC} < 16V, I_{Q4} = 400mA mA Load regulation ΔV_{OLD4} 1mA < I_{Q4} < 400mA	Load regulation	$\Delta V_{OLD}3$	$1mA < I_{O}3 < 400mA$		70	150	mV
$\begin{array}{ c c c c } \hline Dropout voltage 2 & V_{DROPA}^* & I_03 = 200mA & 0 & 0.2 & 0.4 & V \\ \hline Rippie rejection & R_{RE,J}3 & f = 120Hz, I_03 = 400mA & 40 & 50 & dB \\ \hline ILM (s.4V) Output; CTRL2 = [M + H] \\ \hline ILM output voltage & V_04 & I_04 = 400mA & 8.0 & 8.4 & 8.8 & V \\ \hline ILM output voltage & V_04 & I_04 = 400mA & 6.0 & 8.4 & 8.8 & V \\ \hline ILM output current & I_04 & 0.8V < V_{CC} < 16V, I_04 = 400mA & 0.0 & 0 & mV \\ \hline Load regulation & \Delta V_{OL}V4 & 10.8V < V_{CC} < 16V, I_04 = 400mA & 0.0 & 70 & 150 & mV \\ \hline Dropout voltage 1 & V_{DROP4} & I_04 = 400mA & 0.0 & 70 & 150 & mV \\ \hline Dropout voltage 1 & V_{DROP4} & I_04 = 400mA & 0.0 & 1.0 & 1.5 & V \\ \hline Dropout voltage 1 & V_{DROP4} & I_04 = 400mA & 0.0 & 0.7 & 1.05 & V \\ \hline Dropout voltage 2 & V_{DROP4} & I_04 = 200mA & 0.0 & 0.7 & 1.05 & V \\ \hline Rippie rejection & R_{RE,J4} & f = 120Hz, I_04 = 400mA & 40 & 50 & 0 & dB \\ \hline AMP_HS-SW; CTRL2 = [M 2 or H] & & & & & & & & & & & & & & & & & & $	Dropout voltage 1	V _{DROP} 3	I _O 3 = 400mA		0.4	0.8	V
Ripple rejection R _{REJ} 3 f = 120Hz, $I_{O}3 = 400mA$ 40 50 dB LLM (8.4V) Output ; CTRL2 = [MI + J] ILM output voltage Vo4 $I_{O}4 = 400mA$ 8.0 8.4 8.8 V ILM output current $I_{O}4$ $I_{O}4 = 400mA$ 500 6.8.4 8.8.8 V Line regulation Λ^V_{OLN4} $10.8V < V_{CC} < 16V, I_{O}4 = 400mA$ 6.0 8.0 8.0 8.0 9.0 mV Load regulation Δ^V_{OLD4} $1mA < I_{O}4 < 400mA$ 6.0 7.0 15.0 mV Dropout voltage 1 V_{DROP4} $I_{O}4 = 400mA$ 6.0 1.0 1.5 V Dropout voltage 2 V_{DROP4} $I_{O}4 = 200mA$ 4.0 50 0 0 B AMP_HS-SW; CTRL2 = [M2 or H] I I 1.04 = 400mA 4.0 50 0 0 Output voltage 0 V_{DROP4} $I_{O}4 = 200mA$ 4.0 50 V 0 0 0 0 Output voltage	Dropout voltage 2	V _{DROP} 3'	I _O 3 = 200mA		0.2	0.4	V
ILM (8.4V) Output; CTRL2 = [MI + J] ILM output voltage V ₀ 4 I ₀ 4 = 400mA 8.0 8.4 8.8 V ILM output current I ₀ 4 500 mA Line regulation $\Delta V_{0LN}4$ 10.8V < V _{CC} < 16V, I ₀ 4 = 400mA 3.0 90 mV Load regulation $\Delta V_{0LD}4$ 1mA < I ₀ 4 < 400mA	Ripple rejection	R _{REJ} 3	f = 120Hz, I _O 3 = 400mA	40	50		dB
ILM output voltage Vo4 Io4 = 400mA 8.0 8.4 8.8 V ILM output current Io4 500 mA mA Line regulation ΔV_{OLN} 4 10.8V < V_{CC} < 16V, Io4 = 400mA	ILM (8.4V) Output ; CTRL2 = [M1	l or H」					
ILM output current IQ4 500 mA Line regulation ΔV_{OLN4} 10.8V < V_{CC} < 16V, IQ4 = 400mA	ILM output voltage	V _O 4	I _O 4 = 400mA	8.0	8.4	8.8	V
Line regulation ΔV_{OLN4} $10.8V < V_{CC} < 16V, 1_0 4 = 400mA$ 30 90 mV Load regulation ΔV_{OLD4} $1mA < I_04 < 400mA$ 70 150 mV Dropout voltage 1 V_{DROP4} $I_04 = 400mA$ 1.0 1.5 V Dropout voltage 2 $V_{DROP4'}$ $I_04 = 200mA$ 40 50 dB AMP_HS-SW; CTRL2 = [M2 or H] 10.5 V_{CC}	ILM output current	I _O 4		500			mA
Load regulation $\Delta V_{OLD}4$ ImA < lo4 < 400mA 70 150 mV Dropout voltage 1 $V_{DROP}4$ lo4 = 400mA 1.0 1.0 1.5 V Dropout voltage 2 $V_{DROP}4^{1}$ lo4 = 200mA 40 50 V dB Ripple rejection RREJ4 f = 120Hz, lo4 = 400mA 40 50 V dB AMP_HS-SW; CTRL2 = [M2 or H] f = 120Hz, lo4 = 400mA 40 50 V dB Output voltage V_{05} lo5 = 500mA 40 50 V dB Output current lo5 $V_{05} \leq V_{0c} - 1.0$ 350 V mA DSP output current lo5 $V_{05} \leq V_{0c} - 1.0$ 3.0 M mA DSP output voltage V_{07} $I_{07} = 200mA$ 3.1 3.3 3.5 V DSP output current I_{07} $I_{07} = 200mA$ 3.0 9.0 mV Load regulation $\Delta V_{0LN}7$ $I_{07} < 200mA$ 3.0 9.0 mV	Line regulation	$\Delta V_{OLN}4$	$10.8V < V_{CC} < 16V, I_{O}4 = 400 \text{mA}$		30	90	mV
Dropout voltage 1 V_{DROP4} $I_04 = 400mA$ 1.0 1.5 V Dropout voltage 2 $V_{DROP4'}$ $I_04 = 200mA$ 0.0 0.07 1.05 V Ripple rejection R_{REJ4} f = 120Hz, $I_04 = 400mA$ 400 500 dB AMP_HS-SW; CTRL2 = $[M2 \text{ or } H]$ V_{C1} V_{CC} V_{CC} V_{CC} V_{C} Output voltage V_05 $I_05 = 500mA$ V_{CC} V_{CC} V M Output current I_05 $V_{05 \leq V_{CC}$ V_{CC} V_{CC} M M DSP output voltage V_07 $I_07 = 200mA$ 3.1 3.3 3.5 V DSP output voltage V_07 $I_07 = 200mA$ 3.1 3.3 3.5 V DSP output voltage V_07 $I_07 = 200mA$ 3.0 3.0 M M Line regulation ΔV_{OLN7} $I_0V < V_{CC} < 16V, I_07 = 200mA$ 3.0 M M Load regulation ΔV_{OLD7} <td>Load regulation</td> <td>$\Delta V_{OLD}4$</td> <td>$1mA < I_{O}4 < 400mA$</td> <td></td> <td>70</td> <td>150</td> <td>mV</td>	Load regulation	$\Delta V_{OLD}4$	$1mA < I_{O}4 < 400mA$		70	150	mV
Dropout voltage 2 $V_{DROP4'}$ $I_04 = 200mA$ $(-1, -1, -1, -1, -1, -1, -1, -1, -1, -1, $	Dropout voltage 1	V _{DROP} 4	I _O 4 = 400mA		1.0	1.5	V
Ripple rejection R _{REJ} 4 f = 120Hz, I_04 = 400mA 40 50 dB AMP_HS-SW; CTRL2 = $[M2 \text{ or } H]$ V_05 I_05 = 500mA V _{CC} -1.0 V _{CC} -0.5 V Output voltage V_05 V_05 < V _{CC} -1.0 350 V MA DSP(3.3V output); CTRL1 = $[M \ or \ H]$ V V MA MA DSP output voltage V_07 I_07 = 200mA 3.1 3.3 3.5 V DSP output voltage V_07 I_07 = 200mA 3.0 3.0 mA DSP output voltage V_07 I_07 = 200mA 3.1 3.3 3.5 V DSP output voltage V_07 I_07 = 200mA 3.0 3.0 mA Line regulation $\Delta V_{OLN}7$ 10V < V _{CC} < 16V, I_07 = 200mA 3.0 3.0 mV Ripple rejection R _{RE} J7 f = 120Hz, I_07 = 200mA 400 500 MD CD output voltage V_08 I_08 = 1000mA 7.6 8.0 8.4 V CD output voltage V_08	Dropout voltage 2	V _{DROP} 4'	I _O 4 = 200mA		0.7	1.05	V
AMP_HS-SW; CTRL2 = $\lceil M2 \text{ or H} ceil Output voltage V05 I05 = 500mA VCC-1.0 VCC-0.5 V Output current I05 V05 \leq VCC-1.0 350 M mA DSP(3.3V output); CTRL1 = \lceil M \cup H ceil U 350 V mA DSP output voltage V07 I07 = 200mA 3.1 3.3 3.5 V DSP output voltage V07 I07 = 200mA 3.1 3.3 3.5 V DSP output current I07 I07 = 200mA 3.0 M mA Line regulation \DeltaVOLN7 10V < VCC < 16V, I07 = 200mA 300 M mV Load regulation \DeltaVOLD7 1mA < I07 < 200mA 400 500 mV Ripple rejection RREJ7 f = 120Hz, I07 = 200mA 400 500 dB CD output voltage V08 I08 = 1000mA 7.6 8.0 8.4 V CD output voltage V08 I08 = 1000mA 7.6 8.0 M <$	Ripple rejection	R _{REJ} 4	f = 120Hz, I _O 4 = 400mA	40	50		dB
Output voltage V_05 $I_05 = 500$ mA $V_{CC}-1.0$ $V_{CC}-0.5$ V Output current I_05 $V_{05} \le V_{CC}-1.0$ 350 Image matrix mA DSP(3.3V output); CTRL1 = [M or J] J J_07 $I_07 = 200$ mA 3.1 3.3 3.5 V DSP output voltage V_07 $I_07 = 200$ mA 3.0 J_0 mA DSP output current I_07 $I_07 = 200$ mA 3.0 J_0 mA Line regulation ΔV_{0LN7} $10V < V_{CC} < 16V, I_07 = 200$ mA 3.0 90 mV Load regulation ΔV_{0LD7} $10V < V_{CC} < 16V, I_07 = 200$ mA 3.0 90 mV Ripple rejection R_{REJ7} f = 120Hz, I_07 = 200 mA 40 50 dB CD(8.0V output); CTRL1 = [H] V_{08} $I_08 = 1000$ mA 40 50 dB CD output voltage V_08 $I_08 = 1000$ mA 7.6 8.0 8.4 V CD output current I_08 $10.5V < V_$	AMP_HS-SW; CTRL2 = [M2 or H	J					
Output current IO5 VO5 \leq VCC-1.0 350 mA DSP(3.3V output); CTRL1 = [M \lor HJ DSP output voltage VO7 IO7 = 200mA 3.1 3.3 3.5 V DSP output voltage VO7 IO7 = 200mA 3.1 3.3 3.5 V DSP output current IO7 IO7 = 200mA 300 mA mA Line regulation ΔV_{OLN7} 10V < VCC < 16V, IO7 = 200mA	Output voltage	V _O 5	I _O 5 = 500mA	V _{CC} -1.0	V _{CC} -0.5		V
DSP(3.3V output); CTRL1 = $[M \cup H]$ DSP output voltage V ₀ 7 I ₀ 7 = 200mA 3.1 3.3 3.5 V DSP output current I ₀ 7 300 M MA Line regulation $\Delta V_{OLN}7$ 10V < V _{CC} < 16V, I ₀ 7 = 200mA 300 90 mV Load regulation $\Delta V_{OLN}7$ 10V < V _{CC} < 16V, I ₀ 7 = 200mA 300 90 mV Load regulation $\Delta V_{OLD}7$ 1mA < I ₀ 7 < 200mA	Output current	I _O 5	$V_O 5 \le V_{CC}$ -1.0	350			mA
$\begin{array}{c c c c c c c c } DSP \ output \ voltage & V_07 & I_07 = 200 \text{mA} & 3.1 & 3.1 & 3.3 & 3.5 & V \\ \hline DSP \ output \ current & I_07 & & & & & & & & & & & & & & & & & & &$	DSP(3.3V output); CTRL1 = M c	or H_					
$\begin{array}{c c c c c c c c } DSP \mbox{ output current } & I_07 & I0V < V_{CC} < 16V, I_07 = 200mA & 300 & MV & 300 & mV \\ \hline Line \mbox{ regulation } & \Delta V_{OLD}7 & I0V < V_{CC} < 16V, I_07 = 200mA & 0 & 70 & 150 & mV \\ \hline Load \mbox{ regulation } & \Delta V_{OLD}7 & ImA < I_07 < 200mA & 40 & 50 & 0 & dB \\ \hline CD(8.0V \mbox{ output}); \mbox{ CTRL1 = [H]} & & & & & & & & \\ \hline CD \mbox{ output voltage } & V_08 & I_08 = 1000mA & 7.6 & 8.0 & 8.4 & V \\ \hline CD \mbox{ output current } & I_08 & I0.5V < V_{CC} < 16V, I_08 = 1000mA & 50 & 100 & mV \\ \hline Line \mbox{ regulation } & \Delta V_{OLN}8 & 10.5V < V_{CC} < 16V, I_08 = 1000mA & 50 & 100 & mV \\ \hline Load \mbox{ regulation } & \Delta V_{OLD}8 & 10mA < I_08 < 1000mA & 0 & 100 & 200 & mV \\ \hline \end{array}$	DSP output voltage	V _O 7	I _O 7 = 200mA	3.1	3.3	3.5	V
	DSP output current	1 ₀ 7		300			mA
	Line regulation	$\Delta V_{OLN}7$	$10V < V_{CC} < 16V, I_{O}7$ = 200mA		30	90	mV
Ripple rejection $R_{REJ}7$ f = 120Hz, I_07 = 200mA 40 50 dB CD(8.0V output); CTRL1 = [H] CD output voltage V_{O8} I_{O8} = 1000mA 7.6 8.0 8.4 V CD output voltage V_{O8} I_{O8} = 1000mA 7.6 8.0 8.4 V CD output current I_{O8} I_{O8} 10.5V < $V_{CC} < 16V, I_{O8} = 1000mA$ 1300 MA Line regulation ΔV_{OLN8} $10.5V < V_{CC} < 16V, I_{O8} = 1000mA$ 50 100 mV Load regulation ΔV_{OLD8} $10mA < I_{O8} < 1000mA$ 100 200 mV	Load regulation	$\Delta V_{OLD}7$	$1mA < I_{O}7 < 200mA$		70	150	mV
CD(8.0V output); CTRL1 = [H] CD output voltage V_{O8} I_{O8} = 1000mA 7.6 8.0 8.4 V CD output current I_{O8} I_{O8} 1300 mA Line regulation ΔV_{OLN8} $10.5V < V_{CC} < 16V, I_{O8} = 1000mA$ 50 100 mV Load regulation ΔV_{OLD8} $10mA < I_{O8} < 1000mA$ 100 200 mV	Ripple rejection	R _{REJ} 7	f = 120Hz, I _O 7 = 200mA	40	50		dB
	CD(8.0V output); CTRL1 = [H]						
	CD output voltage	V _O 8	I _O 8 = 1000mA	7.6	8.0	8.4	V
Line regulation $\Delta V_{OLN} 8$ 10.5V < V_{CC} < 16V, I_O 8 = 1000 mA 50 100 mV Load regulation $\Delta V_{OLD} 8$ 10mA < I_O 8 < 1000 mA	CD output current	I _O 8		1300			mA
Load regulation △V _{OLD} 8 10mA < I _O 8 < 1000mA 100 200 mV	Line regulation	ΔV _{OLN} 8	$10.5V < V_{CC} < 16V, I_O 8 = 1000 mA$		50	100	mV
	Load regulation	ΔV _{OLD} 8	10mA < I _O 8 < 1000mA		100	200	mV
Dropout voltage V IO8 = 1000mA 1.0 1.5 V	Dropout voltage	V _{DROP} 8	I _O 8 = 1000mA		1.0	1.5	V
Ripple rejection $R_{REJ}8$ f = 120Hz, I_08 = 1000mA4050dB	Ripple rejection	R _{REJ} 8	f = 120Hz, I _O 8 = 1000mA	40	50		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Package Dimensions

unit : mm

HZIP15J CASE 945AC

ISSUE A



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

• Allowable power dissipation derating curve



• Waveform applied during surge test



CTRL Pin Output Truth T

CTRL1	CD	DSP	AUDIO
L	OFF	OFF	OFF
М	OFF	ON	ON
Н	ON	ON	ON

CTRL3	USB
L	OFF
Н	ON

CTRL2	EXT	ILM
L	OFF	OFF
M1	OFF	ON
M2	ON	OFF
Н	ON	ON

Example of CTRL2 application circuit



note) The control terminal is input 3.3V correspondence. Please set it by the input resistance at 5V input.

Block Diagram



Pin Fu	Inction		
Pin No.	Pin name	Description	Equivalent Circuit
1	ILM	ILM output pin ON when CTRL2 = M1, H 8.4V/0.5A	$(15) + V_{CC}$ $(1) + V_{CC}$ $(2) + V_{CC}$ $(3) + V_{CC}$ $(2) + V_{CC}$ $(3) + V_{CC}$ $(4) + V_{CC}$ $(3) + V_{CC}$ $(4) + V_{CC}$ $(3) + V_{CC}$ $(4) + V_{CC}$ $(4) + V_{CC}$ $(5) + V_{CC}$ $(5) + V_{CC}$ $(5) + V_{CC}$ $(6) + V_{CC}$ (6)
2	GND	GND pin	
3	CD	CD output pin ON when CTRL1 = H 8.0V/1.3A	(15) (3) (3) (3) (3) (45) (2) (15)
4	CTRL1	CTRL1 input pin Three value input	
5	AUDIO	AUDIO output pin ON when CTRL1 = M, H 8.4V/0.5A	(15)

Continued on next page.

Continued fi	om preceding pag	e.	
Pin No.	Pin name	Description	Equivalent Circuit
6	CTRL2	CTRL2 input pin Four-value input	
7	DSP	DSP output pin ON when CTRL1 = M, H 3.3V/0.3A	(15) (7)
8	CTRL3	CTRL3 input pin Two-value input	(15)
9	FB	USB-FB pin 1.26V	$(15) \qquad VCC$

Continued on next page.

Continued fr	ontinued from preceding page.					
Pin No.	Pin name	Description	Equivalent Circuit			
10	USBGT	Pch-FET gate connect pin 12.0V				
11	EXT	EXT output pin ON when CTRL2 = M2, H V _{CC} -0.5V/500mA				
12	RSNS	USB current detection resistance connection pin 14.3V	$(15) \qquad \qquad$			
13	V _{DD}	V _{DD} output pin 3.3V/0.3A	$\begin{array}{c} 15 \\ \hline 13 \\ \hline 240 k\Omega \\ \hline 140 k\Omega \\ \hline 2 \\ \hline \end{array} \begin{array}{c} 140 k\Omega \\ \hline 140 k\Omega \\ \hline 140 k\Omega \\ \hline \end{array} \begin{array}{c} 1k\Omega \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \begin{array}{c} 0 \\ \hline 0 \\ \hline 0 \\ \hline \end{array} \end{array}$			
14	V _{CC} 1	V _{DD} power supply pin				
15	V _{CC}	Power supply pin				
			2 GND			

Timing Chart



Recommended Operation Circuit



Peripheral parts list

Name of part	Description	Recommended value	Remarks
C2, C4, C6, C8, C11, C16	Output stabilization capacitor	10µF or more*	Electrolytic capacitor
C1, C3, C5, C7, C10, C15	Output stabilization capacitor	0.22µF or more*	Ceramic capacitor
C12, C13	Capacity for phase amends	C12=1000pF (C13=0pF: TBD)	Ceramic capacitor
C18, C20	Power supply bypass capacitor	100µF or more	These capacitors must be placed near
C17, C19	Oscillation prevention capacitor	$0.22 \mu F$ or more	the V_{CC} and GND pins.
C14	EXT output stabilization capacitor	2.2µF or more	
R1, R2	Resistor for ILM voltage adjustment	R1/R2=9.1k Ω /27k Ω for 5.0V	A resistor with resistance accuracy as low as less than $\pm 1\%$ must be used.
R3	Resistor for AUDIO voltage setting	0.1Ω for Ipeak=3A	Panasonic ERJB1CFR10U(Reference)
M1	USB output Pch-FET	2SJ650	
D1	Diode for prevention of backflow		
D2, D3	Diode for internal element protection	SB1003M3	

note)The circuit diagram and the values are only tentative which are subject to change.

* : Make sure that the capacitors of the output pins are 10μF or higher and ESR is 10Ω or lower in total and temperature characteristics and accuracy are taken into consideration. Also the E-cap should have good high frequency characteristics.

• USB output voltage setting method



The FB voltage is determined by the internal band gap voltage of the IC (typ = 1.26V)

Formula for USB voltage calculation

$$USB = \frac{1.26[V]}{R_1} \times R_2 + 1.26[V]$$
$$\frac{R_2}{R_1} = \frac{(USB-1.26)}{1.26}$$

Please design so that the ratio of R1 and R2 may fill the above-mentioned expression for the set USB voltage.

$$\frac{\frac{R_2}{R_1}}{\frac{R_2}{R_1}} = \frac{(5.0-1.26)}{1.26} \cong 2.968$$
$$\frac{\frac{R_2}{R_1}}{\frac{R_2}{R_1}} = \frac{27k\Omega}{9.1k\Omega} \cong 2.967$$

$$USB = 1.26V \times 2.967 + 1.26V \cong 4.998V$$

• How to set USB overcurrent limit value (OCP)

OCP of the USB works when the voltage of RSNS is under V_{CC}-0.3V. The peak current value of OCP is calculated as follws: Ipeak(A) =0.3/R3. (ex.) R3= $0.1\Omega \rightarrow$ Ipeak=3A

• Since this IC does not detect the heat generation of the external FET, keep the temperature of the FET as low as possible so as not to exceed the eatings.

• Recommended FET: 2SJ650.

(note)The above values were obtained under typcal conditions. The values may fluctuate in manufacturing processes due to external resistor and IC variation.



Warning

The internal circuit of USBGT and RSNS consist of components that support 5V. Do not bias 7V or above between V_{CC} and these pins to prevent the IC from destruction.

Caution for implementing LV5692P to a system board

The package of LV5692P is HZIP15J which has some metal exposures other than connection pins and heatsink as shown in the diagram below. The electrical potentials of (2) and (3) are the same as those of pin 15 and pin 1, respectively. (2) (=pin 15) is the V_{CC} pin and (3) (=pin 1) is the ILM (regulator) output pin. When you implement the IC to the set board, make sure that the bolts and the heatsink are out of touch from (2) and (3). If the metal exposures touch the bolts which has the same electrical potential with GND, GND short occurs in ILM output and V_{CC}. The exposures of (1) are connected to heatsink which has the same electrical potential with substrate of the IC chip (GND). Therefore, (1) and GND electrical potential of the set board can connect each other.

• HZIP15J outline



LV5692P





HZIP15J Heat sink attachment

Heat sinks are used to lower the semiconductor device junction temperature by leading the head generated by the device to the outer environment and dissipating that heat.

- a. Unless otherwise specified, for power ICs with tabs and power ICs with attached heat sinks, solder must not be applied to the heat sink or tabs.
- b. Heat sink attachment
 - \cdot Use flat-head screws to attach heat sinks.
 - Use also washer to protect the package.
 - · Use tightening torques in the ranges 39-59Ncm(4-6kgcm).
 - If tapping screws are used, do not use screws with a diameter larger than the holes in the semiconductor device itself.
 - \cdot Do not make gap, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
 - Take care a position of via hole .
 - \cdot Do not allow dirt, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
 - · Verify that there are no press burrs or screw-hole burrs on the heat sink.
 - \cdot Warping in heat sinks and printed circuit boards must be no more than
 - 0.05 mm between screw holes, for either concave or convex warping.
 - \cdot Twisting must be limited to under 0.05 mm.
 - · Heat sink and semiconductor device are mounted in parallel.
 - Take care of electric or compressed air drivers
 - The speed of these torque wrenches should never exceed 700 rpm, and should typically be about 400 rpm.
- c. Silicone grease
 - \cdot Spread the silicone grease evenly when mounting heat sinks.
 - · Our company recommends YG-6260 (Momentive Performance Materials Japan LLC)
- d. Mount
 - First mount the heat sink on the semiconductor device, and then mount that assembly on the printed circuit board.
 When attaching a heat sink after mounting a semiconductor device into the printed circuit board, when tightening up a heat sink with the screw, the mechanical stress which is impossible to the semiconductor device and the pin doesn't hang.
- e. When mounting the semiconductor device to the heat sink using jigs, etc.,
 - Take care not to allow the device to ride onto the jig or positioning dowel.
 - · Design the jig so that no unreasonable mechanical stress is not applied to the semiconductor device.
- f. Heat sink screw holes
 - Be sure that chamfering and shear drop of heat sinks must not be larger than the diameter of screw head used.
 - When using nuts, do not make the heat sink hole diameters larger than the diameter of the head of the screws used. A hole diameter about 15% larger than the diameter of the screw is desirable.
 - \cdot When tap screws are used, be sure that the diameter of the holes in the heat sink are not too small. A diameter about 15% smaller than the diameter of the screw is desirable.
- g. There is a method to mount the semiconductor device to the heat sink by using a spring band. But this method is not recommended because of possible displacement due to fluctuation of the spring force with time or vibration.





ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV5692P-E	HZIP15J (Pb-Free)	20 / Fan-Fold

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