Ordering number : ENA1876C

LV5692P

Bi-CMOS IC

System Power Supply IC for Automotive Infotainment Multiple Output Linear Voltage Regulator

ON Semiconductor®

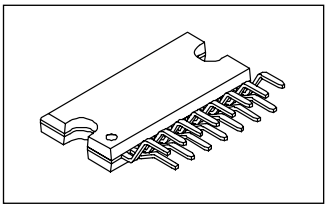
http://onsemi.com

Overview

The LV5692P is a multiple output linear regulator IC, which allows reduction of quiescent current. The LV5692P is specifically designed to address automotive infotainment systems power supply requirements. The LV5692P integrates 5 linear regulator outputs, a liner regulator controller which gives USB supply with external P-channel FET, a high side power switch, over current protection, overvoltage protection and thermal shutdown circuitry.

Function

- Five channel regulator and one channel P-FET pre-driver (for USB-power)
  For V_{DD}: V_{OUT} is 3.3V, $I_O$max is 300mA
  For DSP: V_{OUT} is 3.3V, $I_O$max is 300mA
  For CD: V_{OUT} is 8.0V, $I_O$max is 1300mA
  For illumination: V_{OUT} is 8.4V, $I_O$max is 500mA
  For audio systems: V_{OUT} is 8.4V, $I_O$max is 500mA
  For USB (controller) : V_{OUT} is flexible
  (configurable with external resistor),
  $I_O$max is 1000mA
- High side switch: Voltage difference between input and output is 0.5V, $I_O$max is 500mA
- Over current protector
- Overvoltage protector (Without V_{DD}-OUT) Clamp voltage is 21V (typical)
- Thermal Shut down 175ºC (typical)
- Quiescent current 50μA (Typ. when only VDD is in operation)



HZIP15J

(Warning) The protector functions only improve the IC's tolerance and they do not guarantee the safety of the IC if used under the conditions out of safety range or ratings. Use of the IC such as use under over current protection range or thermal shutdown state may degrade the IC's reliability and eventually damage the IC.

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

March, 2014

32414NK/O2611SY 20111018-S00001/D2210SY/N2410SY No.A1876-1/15

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V_{CC} max			36	V
Power dissipation	Pd max	IC unit	Ta ≤ 25°C	1.5	W
		At using Al heat sink		5.6	W
		At infinity heat sink		32.5	W
Peak voltage	V_{CC} peak	Regarding Bias wave, refer to below the		50	V
Junction temperature	Tj max			150	°C
Operating temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at Ta = 25°C

Parameter	Conditions	Ratings	Unit
Power supply voltage rating 1	V_{DD} output ON, DSP output ON	7 to 16	V
Power supply voltage rating 2	ILM output ON	10.8 to 16	V
Power supply voltage rating 3	Audio output ON, CD output ON	10 to 16	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = 25°C, $V_{CC} = V_{CC}1 = 14.4V$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}	V_{DD} no load, CTRL1/2/3 =「L/L/L」		50	100	μA
CTRL1 Input						
Low input voltage	$V_{IL}1$		0		0.3	V
Middle input voltage	$V_{IM}1$		1.1	1.65	2.1	V
High input voltage	$V_{IH}1$		2.5		5.5	V
Input impedance	$R_{IH}1$		280	400	520	kΩ
CTRL2 Input						
Low input voltage	$V_{IL}2$		0		0.3	V
Middle1 input voltage	$V_{IM1}2$		0.8	1.06	1.4	V
Middle2 input voltage	$V_{IM2}2$		1.9	2.13	2.4	V
High input voltage	$V_{IH}2$		2.9	3.2	5.5	V
Input impedance	$R_{IH}2$		280	400	520	kΩ
CTRL3 input.						
Low input voltage	$V_{IL}3$		0		0.3	V
High input voltage	$V_{IH}3$		2.5		5.5	V
Input impedance	$R_{IH}3$		280	400	520	kΩ
V_{DD}3.3V output						
Output voltage	V_O1	I_O1 = 200mA	3.16	3.3	3.45	V
Output current	I_O1	$V_O1 \geq 3.1V$	300			mA
Line regulation	$\Delta V_{OLN}1$	$7.5V < V_{CC}1 < 16V$, I_O1 = 200mA		30	100	mV
Load regulation	$\Delta V_{OLD}1$	$1mA < I_O1 < 200mA$		70	150	mV
Ripple rejection	$R_{REJ}1$	f = 120Hz, I_O1 = 200mA	30	40		dB
USB output: CTRL3 =「H」(When external power FET 2SJ650, it external resists 27kΩ, and 9.1kΩ is set)						
USB output voltage	V_O2	I_O2 = 1000mA	4.75	5	5.25	V
USB output current	I_O2	$V_O2 \geq 4.75V$	1000			mA
Line regulation	$\Delta V_{OLN}2$	$10V < V_{CC} < 16V$, I_O2 = 1000mA		50	90	mV
Load regulation	$\Delta V_{OLD}2$	$10mA < I_O2 < 1000mA$		100	150	mV
Dropout voltage	$V_{DROP}2$	I_O2 = 1000mA		1.0	1.5	V
Ripple rejection	$R_{REJ}1$	f = 120Hz, I_O2 = 1000mA	40	50		dB

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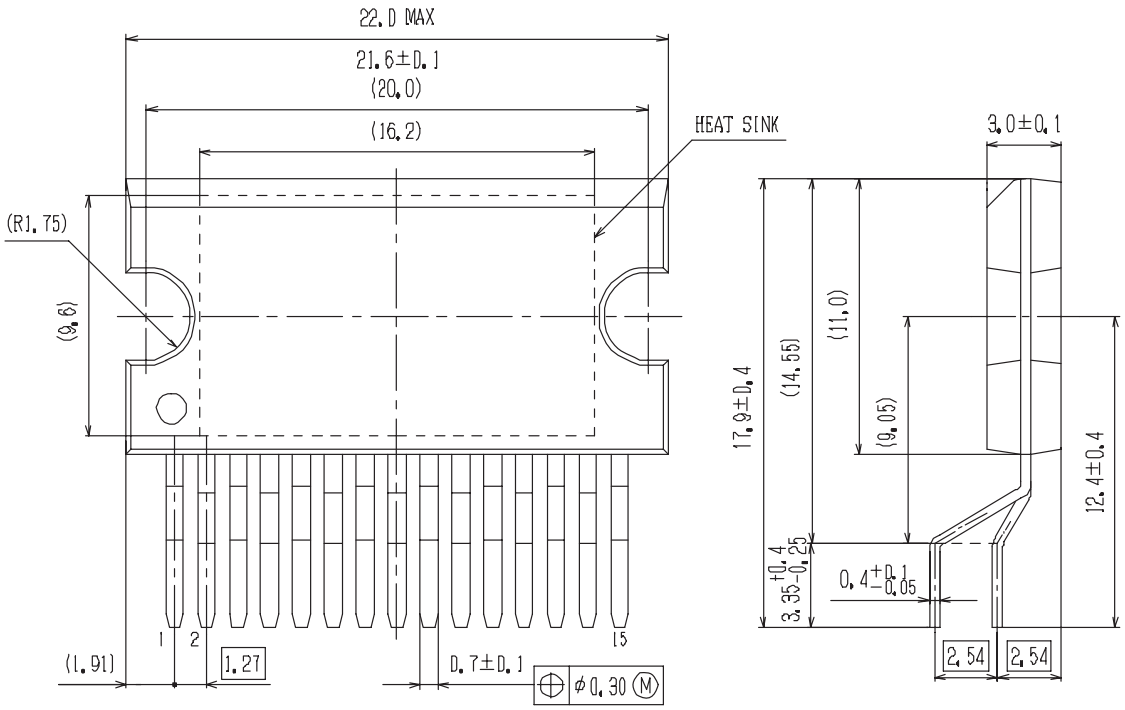
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
AUDIO (8.4V) Output ; CTRL1 =「M or H」						
AUDIO output voltage 1	V_O3	I_O3 = 400mA	8.0	8.4	8.8	V
AUDIO output current	I_O3	$V_O3 \geq 8.0V$	500			mA
Line regulation	$\Delta V_{OLN}3$	10V < V_{CC} < 16V, I_O3 = 400mA		30	90	mV
Load regulation	$\Delta V_{OLD}3$	1mA < I_O3 < 400mA		70	150	mV
Dropout voltage 1	$V_{DROP}3$	I_O3 = 400mA		0.4	0.8	V
Dropout voltage 2	$V_{DROP}3'$	I_O3 = 200mA		0.2	0.4	V
Ripple rejection	$R_{REJ}3$	f = 120Hz, I_O3 = 400mA	40	50		dB
ILM (8.4V) Output ; CTRL2 =「M1 or H」						
ILM output voltage	V_O4	I_O4 = 400mA	8.0	8.4	8.8	V
ILM output current	I_O4		500			mA
Line regulation	$\Delta V_{OLN}4$	10.8V < V_{CC} < 16V, I_O4 = 400mA		30	90	mV
Load regulation	$\Delta V_{OLD}4$	1mA < I_O4 < 400mA		70	150	mV
Dropout voltage 1	$V_{DROP}4$	I_O4 = 400mA		1.0	1.5	V
Dropout voltage 2	$V_{DROP}4'$	I_O4 = 200mA		0.7	1.05	V
Ripple rejection	$R_{REJ}4$	f = 120Hz, I_O4 = 400mA	40	50		dB
AMP_HS-SW; CTRL2 =「M2 or H」						
Output voltage	V_O5	I_O5 = 500mA	V_{CC}-1.0	V_{CC}-0.5		V
Output current	I_O5	$V_O5 \leq V_{CC}$-1.0	350			mA
DSP(3.3V output); CTRL1 =「M or H」						
DSP output voltage	V_O7	I_O7 = 200mA	3.1	3.3	3.5	V
DSP output current	I_O7		300			mA
Line regulation	$\Delta V_{OLN}7$	10V < V_{CC} < 16V, I_O7 = 200mA		30	90	mV
Load regulation	$\Delta V_{OLD}7$	1mA < I_O7 < 200mA		70	150	mV
Ripple rejection	$R_{REJ}7$	f = 120Hz, I_O7 = 200mA	40	50		dB
CD(8.0V output); CTRL1 =「H」						
CD output voltage	V_O8	I_O8 = 1000mA	7.6	8.0	8.4	V
CD output current	I_O8		1300			mA
Line regulation	$\Delta V_{OLN}8$	10.5V < V_{CC} < 16V, I_O8 = 1000mA		50	100	mV
Load regulation	$\Delta V_{OLD}8$	10mA < I_O8 < 1000mA		100	200	mV
Dropout voltage	$V_{DROP}8$	I_O8 = 1000mA		1.0	1.5	V
Ripple rejection	$R_{REJ}8$	f = 120Hz, I_O8 = 1000mA	40	50		dB

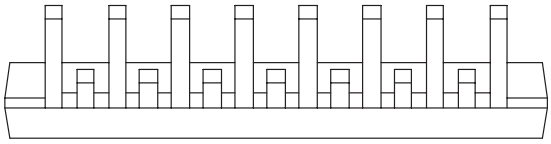
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Package Dimensions

unit : mm

HZIP15J
CASE 945AC
ISSUE A

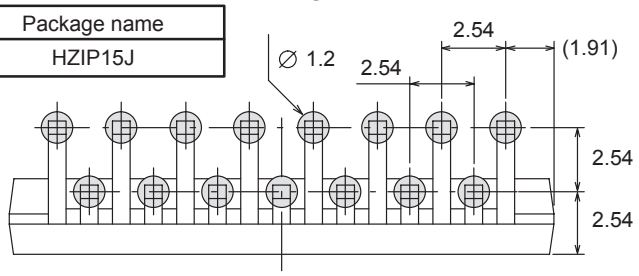




SOLDERING FOOTPRINT*

(Unit: mm) Through Hole Area

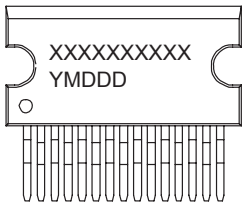
Package name
HZIP15J



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

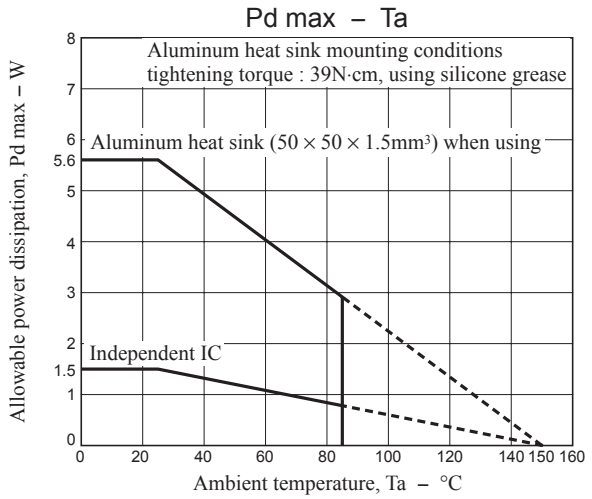
GENERIC MARKING DIAGRAM*



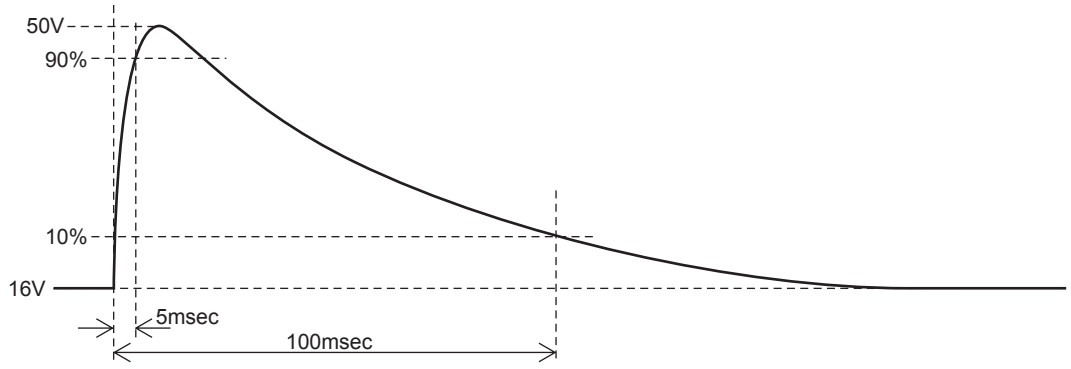
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

• Allowable power dissipation derating curve



• Waveform applied during surge test



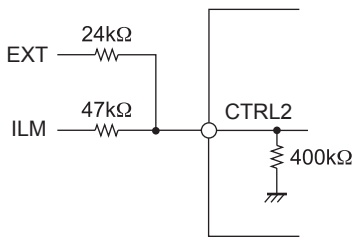
CTRL Pin Output Truth Table

CTRL1	CD	DSP	AUDIO
L	OFF	OFF	OFF
M	OFF	ON	ON
H	ON	ON	ON

CTRL3	USB
L	OFF
H	ON

CTRL2	EXT	ILM
L	OFF	OFF
M1	OFF	ON
M2	ON	OFF
H	ON	ON

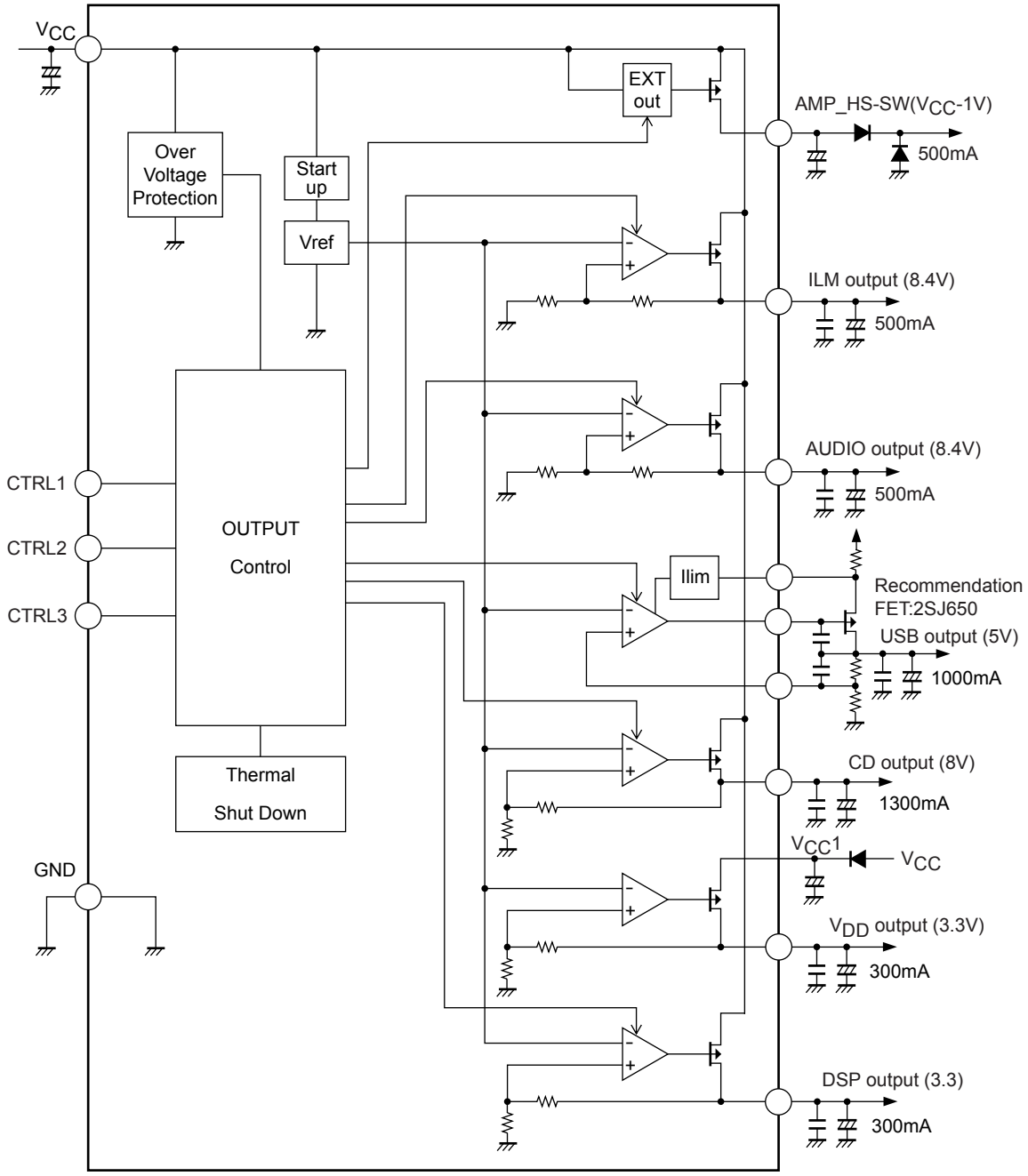
Example of CTRL2 application circuit



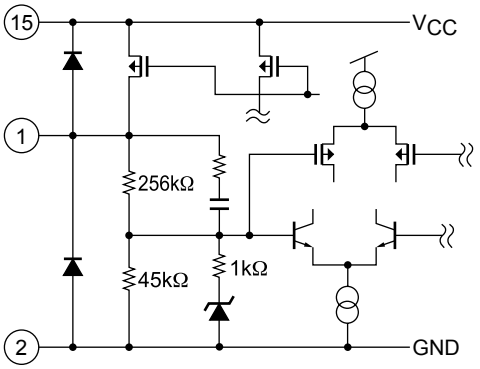
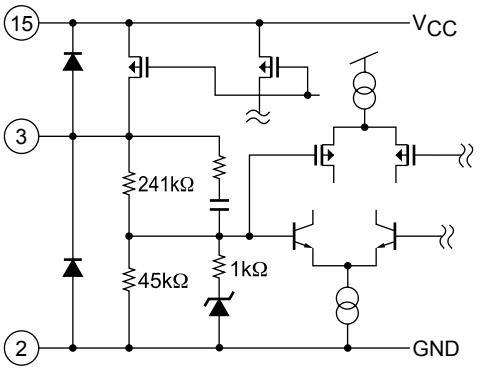
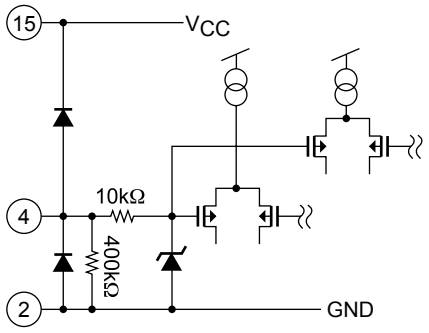
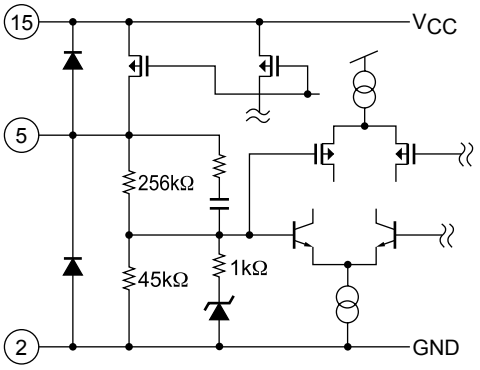
EXT	ILM	CTRL2
0V	0V	0V
0V	3.3V	1.06V
3.3V	0V	2.13V
3.3V	3.3V	3.20V

note) The control terminal is input 3.3V correspondence. Please set it by the input resistance at 5V input.

Block Diagram



Pin Function

Pin No.	Pin name	Description	Equivalent Circuit
1	ILM	ILM output pin ON when CTRL2 = M1, H 8.4V/0.5A	
2	GND	GND pin	
3	CD	CD output pin ON when CTRL1 = H 8.0V/1.3A	
4	CTRL1	CTRL1 input pin Three value input	
5	AUDIO	AUDIO output pin ON when CTRL1 = M, H 8.4V/0.5A	

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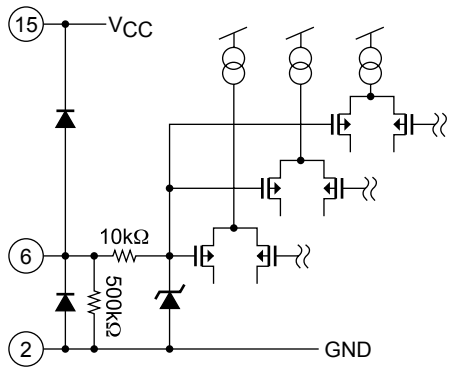
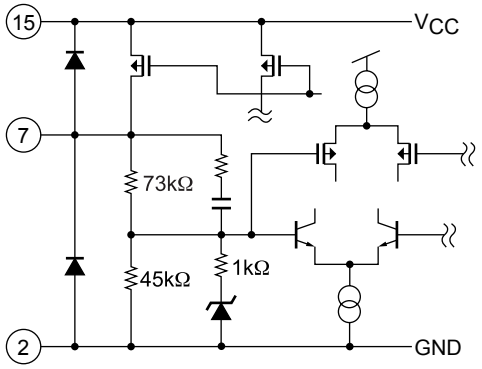
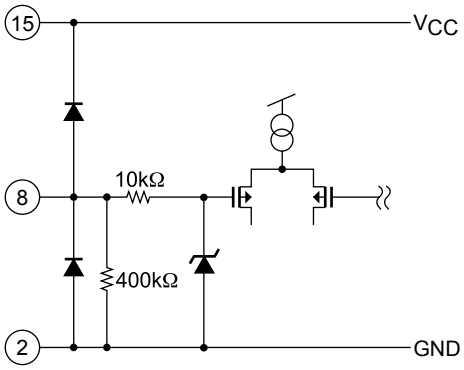
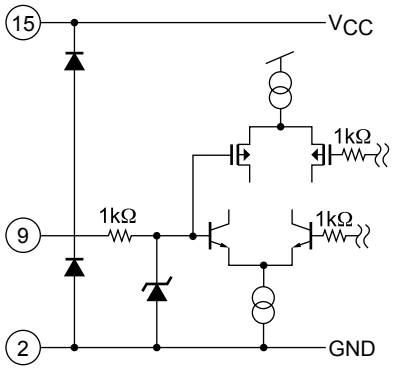
Pin No.	Pin name	Description	Equivalent Circuit
6	CTRL2	CTRL2 input pin Four-value input	
7	DSP	DSP output pin ON when CTRL1 = M, H 3.3V/0.3A	
8	CTRL3	CTRL3 input pin Two-value input	
9	FB	USB-FB pin 1.26V	

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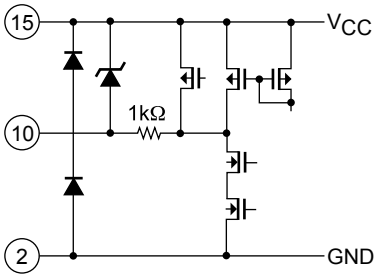
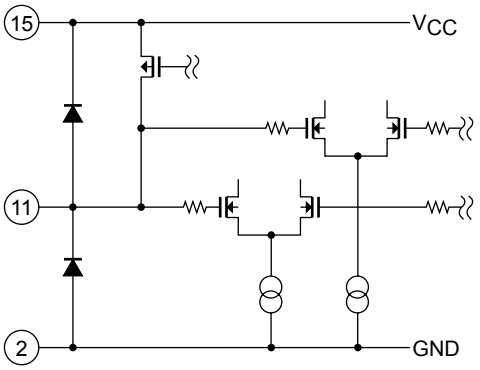
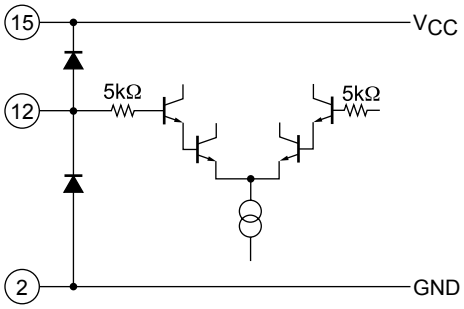
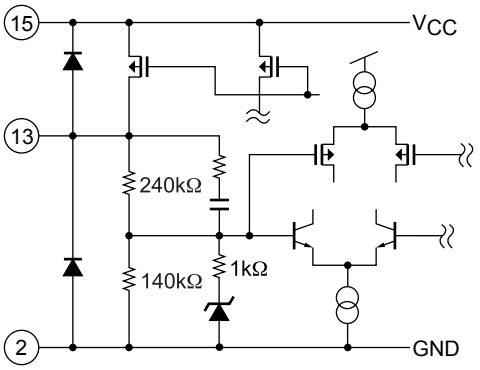
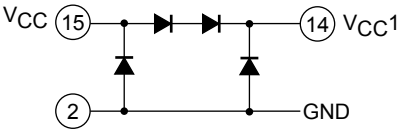
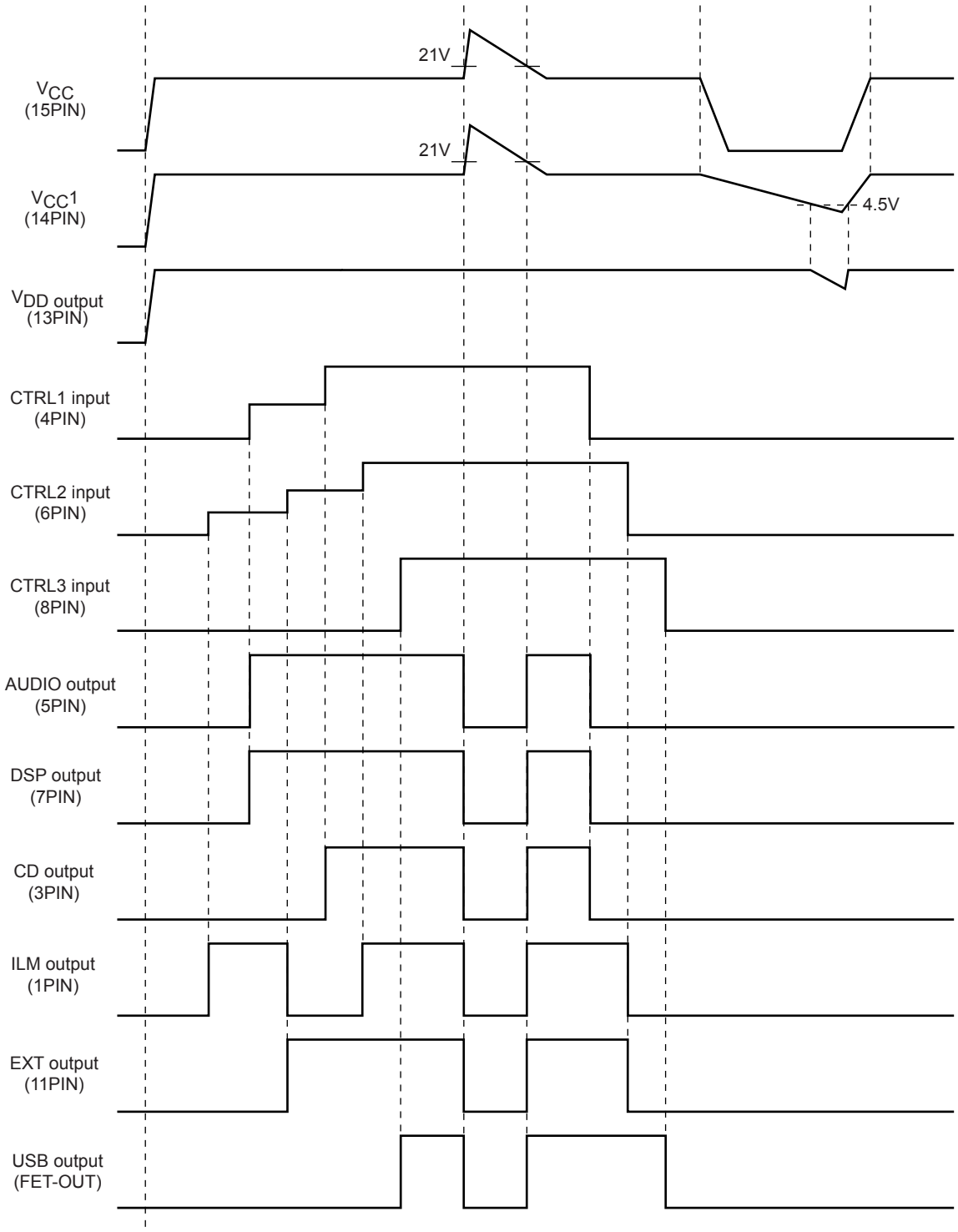
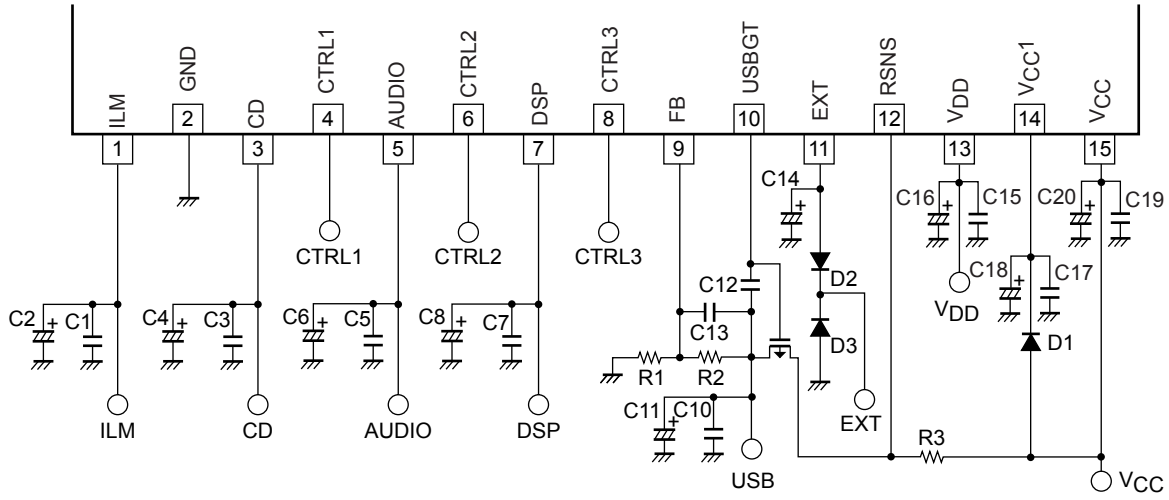
Pin No.	Pin name	Description	Equivalent Circuit
10	USBGT	Pch-FET gate connect pin 12.0V	
11	EXT	EXT output pin ON when CTRL2 = M2, H V_{CC}-0.5V/500mA	
12	RSNS	USB current detection resistance connection pin 14.3V	
13	V_{DD}	V_{DD} output pin 3.3V/0.3A	
14	$V_{CC}1$	V_{DD} power supply pin	
15	V_{CC}	Power supply pin	

Timing Chart



Recommended Operation Circuit



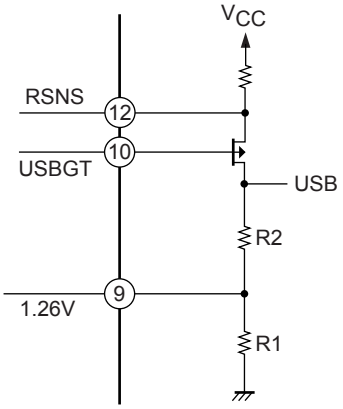
Peripheral parts list

Name of part	Description	Recommended value	Remarks
C2, C4, C6, C8, C11, C16	Output stabilization capacitor	10μF or more*	Electrolytic capacitor
C1, C3, C5, C7, C10, C15	Output stabilization capacitor	0.22μF or more*	Ceramic capacitor
C12, C13	Capacity for phase amends	C12=1000pF (C13=0pF: TBD)	Ceramic capacitor
C18, C20	Power supply bypass capacitor	100μF or more	These capacitors must be placed near the V_{CC} and GND pins.
C17, C19	Oscillation prevention capacitor	0.22μF or more	
C14	EXT output stabilization capacitor	2.2μF or more	
R1, R2	Resistor for ILM voltage adjustment	R1/R2=9.1kΩ/27kΩ for 5.0V	A resistor with resistance accuracy as low as less than ±1% must be used.
R3	Resistor for AUDIO voltage setting	0.1Ω for Ipeak=3A	Panasonic ERJB1CFR10U(Reference)
M1	USB output Pch-FET	2SJ650	
D1	Diode for prevention of backflow		
D2, D3	Diode for internal element protection	SB1003M3	

note)The circuit diagram and the values are only tentative which are subject to change.

* : Make sure that the capacitors of the output pins are 10μF or higher and ESR is 10Ω or lower in total and temperature characteristics and accuracy are taken into consideration. Also the E-cap should have good high frequency characteristics.

• USB output voltage setting method



The FB voltage is determined by the internal band gap voltage of the IC (typ = 1.26V)

Formula for USB voltage calculation

$$USB = \frac{1.26[V]}{R_1} \times R_2 + 1.26[V]$$

$$\frac{R_2}{R_1} = \frac{(USB\text{-}1.26)}{1.26}$$

Please design so that the ratio of R1 and R2 may fill the above-mentioned expression for the set USB voltage.

$$\frac{R_2}{R_1} = \frac{(5.0\text{-}1.26)}{1.26} \cong 2.968$$

$$\frac{R_2}{R_1} = \frac{27k\Omega}{9.1k\Omega} \cong 2.967$$

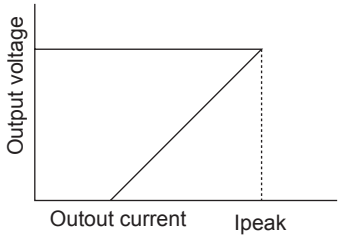
$$USB = 1.26V \times 2.967 + 1.26V \cong \boxed{4.998V}$$

• How to set USB overcurrent limit value (OCP)

OCP of the USB works when the voltage of RSNS is under V_{CC}-0.3V. The peak current value of OCP is calculated as follws: Ipeak(A) =0.3/R3. (ex.) R3=0.1Ω → Ipeak=3A

• Since this IC does not detect the heat generation of the external FET, keep the temperature of the FET as low as possible so as not to exceed the eatings.
• Recommended FET: 2SJ650.

(note)The above values were obtained under typcal conditions. The values may fluctuate in manufacturing processes due to external resistor and IC variation.



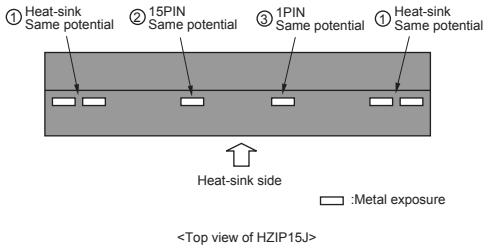
• Warning

The internal circuit of USBGT and RSNS consist of components that support 5V. Do not bias 7V or above between V_{CC} and these pins to prevent the IC from destruction.

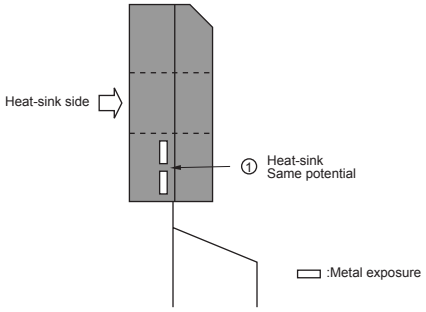
Caution for implementing LV5692P to a system board

The package of LV5692P is HZIP15J which has some metal exposures other than connection pins and heatsink as shown in the diagram below. The electrical potentials of (2) and (3) are the same as those of pin 15 and pin 1, respectively. (2) (=pin 15) is the V_{CC} pin and (3) (=pin 1) is the ILM (regulator) output pin. When you implement the IC to the set board, make sure that the bolts and the heatsink are out of touch from (2) and (3). If the metal exposures touch the bolts which has the same electrical potential with GND, GND short occurs in ILM output and V_{CC}. The exposures of (1) are connected to heatsink which has the same electrical potential with substrate of the IC chip (GND). Therefore, (1) and GND electrical potential of the set board can connect each other.

・ HZIP15J outline

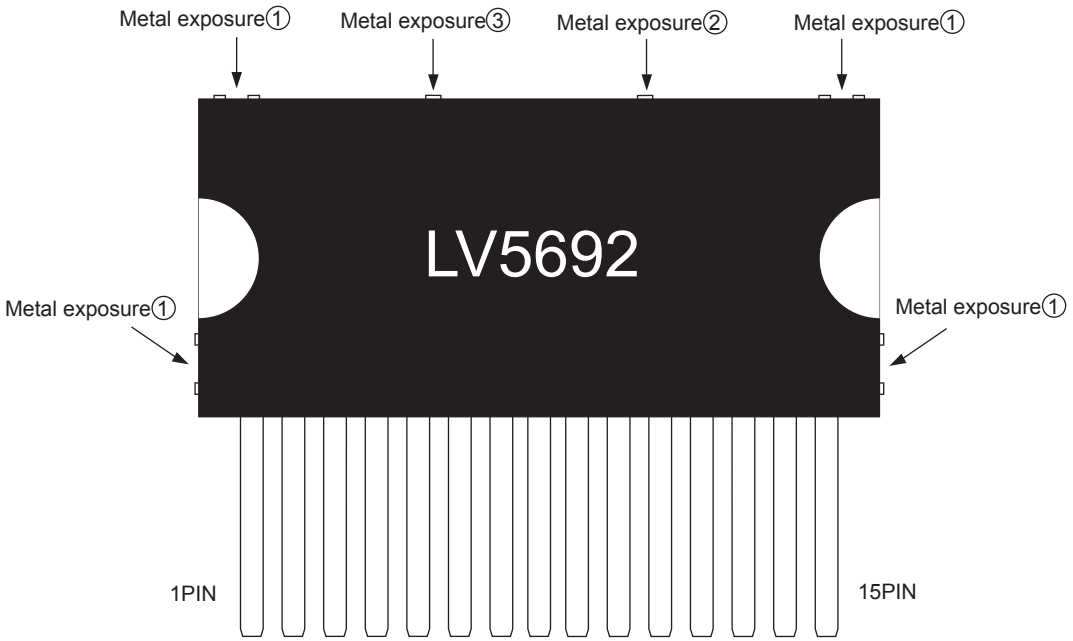


<Top view of HZIP15J>



<Side view of HZIP15J>

• Frame diagram (LV5692P) *In the system power supply other than LV5692P, pin assignment may differ.

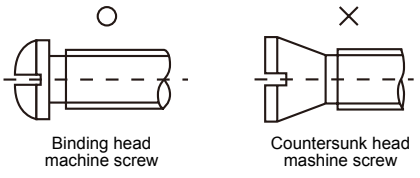


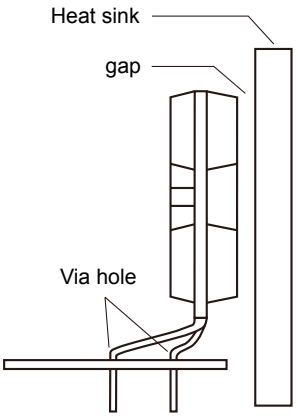
HZIP15J Heat sink attachment

Heat sinks are used to lower the semiconductor device junction temperature by leading the head generated by the device to the outer environment and dissipating that heat.

a. Unless otherwise specified, for power ICs with tabs and power ICs with attached heat sinks, solder must not be applied to the heat sink or tabs.

b. Heat sink attachment
- · Use flat-head screws to attach heat sinks.
- · Use also washer to protect the package.
- · Use tightening torques in the ranges 39-59Ncm(4-6kgcm) .
- · If tapping screws are used, do not use screws with a diameter larger than the holes in the semiconductor device itself.
- · Do not make gap, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- · Take care a position of via hole .
- · Do not allow dirt, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- · Verify that there are no press burrs or screw-hole burrs on the heat sink.
- · Warping in heat sinks and printed circuit boards must be no more than 0.05 mm between screw holes, for either concave or convex warping.
- · Twisting must be limited to under 0.05 mm.
- · Heat sink and semiconductor device are mounted in parallel. Take care of electric or compressed air drivers
- · The speed of these torque wrenches should never exceed 700 rpm, and should typically be about 400 rpm.





c. Silicone grease
- · Spread the silicone grease evenly when mounting heat sinks.
- · Our company recommends YG-6260 (Momentive Performance Materials Japan LLC)

d. Mount
- · First mount the heat sink on the semiconductor device, and then mount that assembly on the printed circuit board.
- · When attaching a heat sink after mounting a semiconductor device into the printed circuit board, when tightening up a heat sink with the screw, the mechanical stress which is impossible to the semiconductor device and the pin doesn't hang.

e. When mounting the semiconductor device to the heat sink using jigs, etc.,
- · Take care not to allow the device to ride onto the jig or positioning dowel.
- · Design the jig so that no unreasonable mechanical stress is not applied to the semiconductor device.

f. Heat sink screw holes
- · Be sure that chamfering and shear drop of heat sinks must not be larger than the diameter of screw head used.
- · When using nuts, do not make the heat sink hole diameters larger than the diameter of the head of the screws used. A hole diameter about 15% larger than the diameter of the screw is desirable.
- · When tap screws are used, be sure that the diameter of the holes in the heat sink are not too small. A diameter about 15% smaller than the diameter of the screw is desirable.

g. There is a method to mount the semiconductor device to the heat sink by using a spring band. But this method is not recommended because of possible displacement due to fluctuation of the spring force with time or vibration.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV5692P-E	HZIP15J (Pb-Free)	20 / Fan-Fold

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