

# BLDC Motor Driver with Speed Control, Single-Phase, 12 V

## LV8316H

### Overview

The LV8316H is the driver for a single-phase BLDC motor, which controls motor rotational speed with the built-in closed loop speed controller. Its target speed can be set by input PWM duty cycle. The speed curve setting can be stored to the internal nonvolatile memory (NVM). In addition, Lead-angle can also be adjusted by the configuration saved in the internal NVM. Thus, it can drive various kinds of motors at high efficiency and low noise.

### Features

- Single-phase Full Wave Fan Motor Driver,  $I_{omax}$ : 2.0 A
- PWM Duty Cycle Input (25 Hz to 100 kHz)
- PI Closed Loop Speed Control Function
- Soft Start-up Function
- PWM Soft Switching Phase Transitions
- Soft PWM Duty Cycle Transitions (Changing the Target Speed Gradually)
- Built-in Current Limit Circuit Function and Over Current Protection Function
- Built-in Thermal Protection Function
- Built-in Locked Rotor Protection and Automatic Recovery Function
- FG or RD Signal Output Selectable
- Dynamic Lead Angle Adjustment with Respect to Rotation Speed
- Parameter Setting by Serial Communication
- Embedded EEPROM as NVM
- Parameter Setting to the NVM
- Pb-Free and Halogen Free

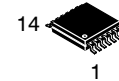
### Typical Applications

- Telecom Server and Base Station Cooling Fan
- Desktop PC Cooling Fan
- Server Cooling Fan
- Refrigerator Circulation Fan
- Appliance Cooling Fan
- Power Supply Unit Cooling Fan



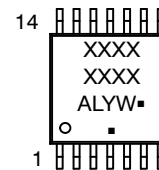
ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)



TSSOP-14  
EXPOSED PAD  
CASE 948AW

### MARKING DIAGRAM



XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
LV8316HGR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# LV8316H

## APPLICATION DIAGRAM

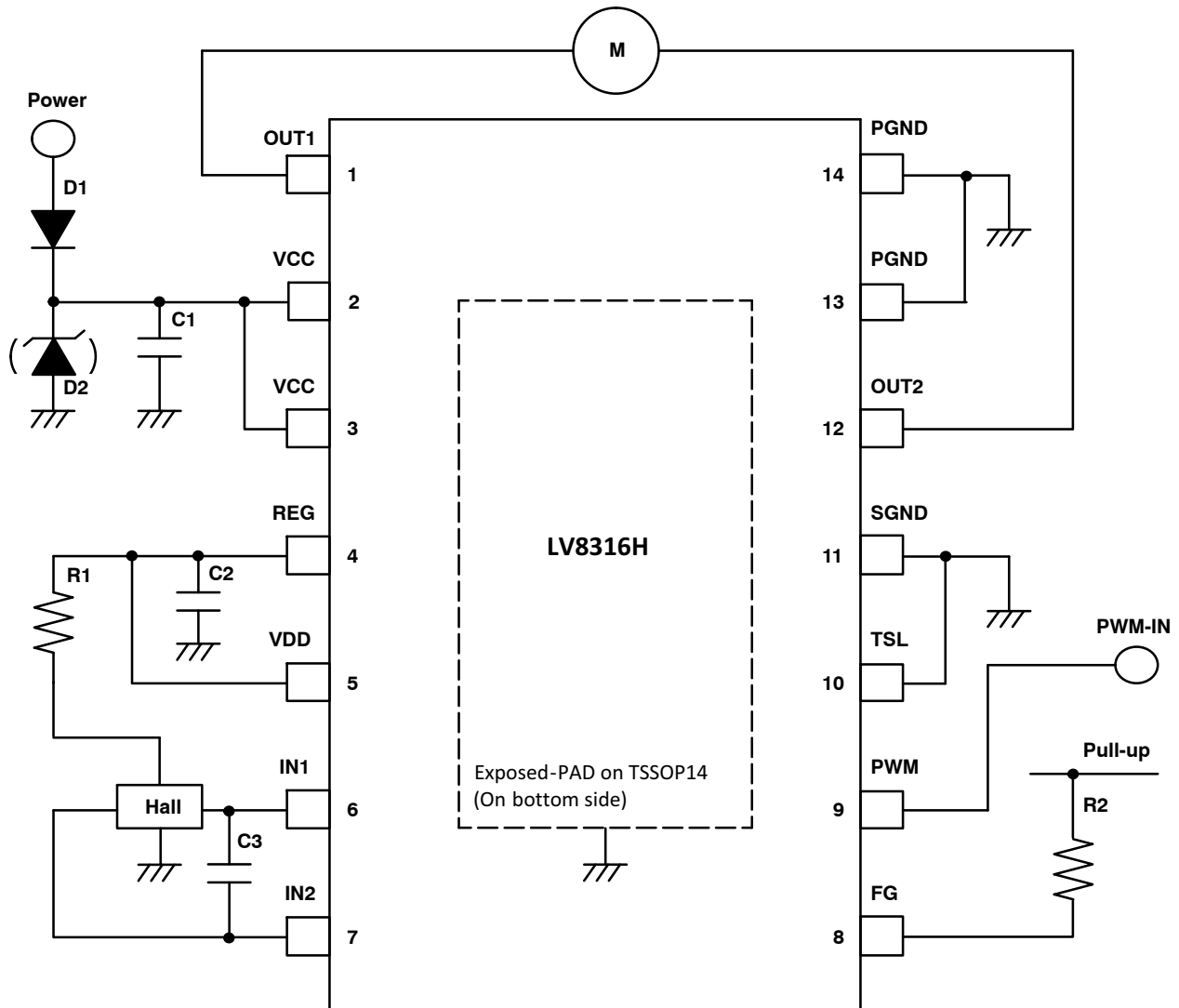


Figure 1. Application Diagram

Table 1. EXAMPLE COMPONENT VALUE

Device	Qty	Description	Value	Tol	Footprint	Manufacture	Manufacture Part Number
D1	1	Anti-reverse connection diode	-	-	TSSOP14EP	ONSEMI	LV8316H
D2	1	Anti-abnormal boost Zener diode	-	-			
C1	1	VCC bypass condenser	10 $\mu$ F 50 V	10%			
C2	1	REG bypass condenser	1 $\mu$ F 25 V	10%			
C3	1	Filter of system noise	0.1 $\mu$ F 50 V	10%			
R1	1	Current limiter resistor for Hall	2 k $\Omega$ 1/4 W	5%			
R2	1	FG pull-up resistor	10 k $\Omega$ 1/4 W	5%			
T1	1	Hall element	-	-			

# LV8316H

## VCC and GND (VCC, GND)

The power supplies of the IC need to be decoupled properly. The following three capacitors must be connected.

- between VCC (pin 2 and pin 3) and PGND (pin 13 and pin 14) as C1 in the application diagrams
- between REG (VDD) and SGND as C2

The Zener diode (D2) in Figure 1 is mandatory to prevent the IC break down in case the supply voltage exceeds the absolute maximum ratings due to the flyback voltage.

## Hall-Sensor Input Pins (IN1, IN2)

Differential output signals of the hall sensor are connected at IN1 and IN2. It is recommended that the capacitor (C3) is connected between both pins to filter system noise. The value of C3 should be selected properly depending on the system noise. When a Hall IC is used, the output of the Hall

IC must be connected to the IN1 pin and the IN2 pin must be kept in the middle level of the Hall IC power supply voltage which should be corresponded to recommended operating range.

## Command Input Pin (PWM)

This pin reads the duty cycle of the PWM pulse which controls rotational speed. The PWM input signal level is supported from 2.8 V to 5.5 V. Linear voltage control is not supported. The minimum pulse width is 100 ns.

## Current Limiter Resistor for Hall (R1)

Hall output amplitude can be adjusted by R1.

The amplitude is proportional to Hall bias level VH for particular magnetic flux density. VH is determined by the following equation.

$$V_H = V_{REG} \times \left( \frac{R_h}{R_h + R_1} \right) \quad (\text{eq. 1})$$

Where

VREG: REG pin voltage (5 V)

Rh: Hall resistance

However, it should be considered with Hall sensor specification and Hall bias current. The bias current should be set under 20 mA which is REG pin max current.

**Table 2. TRUTH TABLE**

IN1	IN2	*Inner PWM State	OUT1	OUT2	FG	Operation State
L	H	On	L	H	Hi-Z	Drive mode
		Off	L	L		Regeneration mode
H	L	On	H	L	L	Drive mode
		Off	L	L		Regeneration mode

\*Inner PWM state means the OUTPUT active period decided by inner control logic. Don't match with PWM-pin input signal.

\*Condition: Register "DRVMODE [1:0]" = 01

# LV8316H

**Table 3. ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	VCC <sub>MAX</sub>	VCC1/VCC2 pin	-0.3 to 20	V
Maximum output voltage	V <sub>OUTMAX</sub>	OUT1/OUT2 pin	20	V
Maximum output current (Note 1)	I <sub>OUTMAX</sub>	OUT1/OUT2 pin	2.0	A
REG pin maximum output current	I <sub>REGMAX</sub>	REG pin	20	mA
IN1/IN2 pin input voltage	V <sub>INMAX</sub>	IN1/IN2 pin	-0.3 to 5.5	V
PWM pin input voltage	V <sub>PWMMAX</sub>	PWM pin	-0.3 to 5.5	V
FG pin withstanding voltage	V <sub>FGMAX</sub>	FG pin	-0.3 to 20	V
FG pin Maximum current	I <sub>FGMAX</sub>	FG pin	7.5	mA
Allowable power dissipation (Note 2)	Pd <sub>MAX</sub>	LV8316H	0.93	W
Operating temperature	T <sub>OP</sub>		-40 to +105	°C
Storage temperature	T <sub>STG</sub>		-55 to +150	°C
Maximum junction temperature	T <sub>Jmax</sub>		150	°C
Moisture Sensitivity Level (MSL) (Note 3)	MSL		1	-
Lead Temperature Soldering Pb-Free Versions (30s or less) (Note 4)	T <sub>SLD</sub>		255	°C
ESD Human body Model : HBM (Note 5)	ESD <sub>HBM</sub>		±4000	V
ESD Charged Device Model : CDM (Note 6)	ESD <sub>CDM</sub>		±1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I<sub>OUTMAX</sub> is the peak value of the motor supply current.
2. Specified circuit board: Toroidal shaped. The actual area is 320 mm<sup>2</sup> and thickness is 0.8 mm, glass epoxy 2-layer board which has 1/2 oz copper traces on top and bottom of the board.
3. Moisture Sensitivity Level (MSL): IPC/JEDEC standard: J-STD-020A
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D [http://www.onsemi.com/pub\\_link/Collateral/SOLDERRM-D.PDF](http://www.onsemi.com/pub_link/Collateral/SOLDERRM-D.PDF)
5. ESD Human Body Model is based on JEDEC standard: JESD22-A114
6. ESD Charged Device Model is based on JEDEC standard: JESD22-C101

**Table 4. THERMAL CHARACTERISTICS**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient (Note 2)	R <sub>θJA</sub>	133.2	°C/W
Thermal Resistance, Junction-to-Case (Top) (Note 2)	R <sub>ψJT</sub>	40	°C/W

**Table 5. RECOMMENDED OPERATING RANGES**

Parameter	Symbol	Conditions	Ratings	Unit
VCC supply voltage	VCC <sub>TYP</sub>	VCC1/VCC2 pin	12	V
VCC operating supply voltage range1	VCC <sub>OP1</sub>	VCC1/VCC2 pin	6.0 to 16	V
VCC operating supply voltage range2 (Note 7)	VCC <sub>OP2</sub>	VCC1/VCC2 pin	3.9 to 6.0	V
VCC operating supply voltage range for NVM program / erase operation	VCC <sub>NVM</sub>	VCC1/VCC2 pin	10.8 to 16	V
PWM input frequency range	F <sub>PWM</sub>	PWM pin	25 to 100k	Hz
PWM minimum input low/high pulse width	T <sub>WPWM</sub>	PWM pin	100	ns
IN1 input voltage range	V <sub>IN1</sub>	IN1 pin	0 to VREG	V
IN2 input voltage range	V <sub>IN2</sub>	IN2 pin	0.3 to 0.55*VREG	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. When the VCC voltage is below 6.0 V, a motor keeps rotation until to 3.9 V, normally. However there are possibility to change the electric characteristics due to low VCC.

# LV8316H

**Table 6. ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{CCOP} = 12\text{ V}$  unless otherwise noted.

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Circuit current	ICC		3.9	12	20	mA
OUT1/OUT2 High-side on-resistance	$R_{OH-ON}$	$I_O = 1.0\text{ A}$		0.28	0.45	$\Omega$
OUT1/OUT2 Low-side on-resistance	$R_{OL-ON}$	$I_O = 1.0\text{ A}$		0.28	0.45	$\Omega$
OUT1/OUT2 PWM output frequency	$f_{PWO}$		45.6	48	50.4	kHz
PWM pin low level input voltage	$V_{PWML}$		0		0.7	V
PWM pin high level input voltage	$V_{PWMH}$		2.8		5.5	V
PWM input resolution	$\Delta_{PWM}$			8		Bit
FG pin low level output voltage	$V_{FGL}$	$I_{FG} = 5\text{ mA}$		0.15	0.3	V
FG pin leak current	$I_{FGLK}$	$V_{CC} = 16\text{ V}$ $V_{FG} = 16\text{ V}$			1	$\mu\text{A}$
REG pin output voltage	$V_{REG}$		4.7	5.0	5.3	V
Lock-detection time1 (Note 8)	$T_{LD1}$	Under rotation	0.27	0.3	0.33	S
Lock-detection time2 (Note 9)	$T_{LD2}$	Start-up	0.63	0.7	0.77	S
Lock-Stop release time1 from 1 <sup>st</sup> to 4 <sup>th</sup> off time	$T_{LRoff1}$		3.1	3.5	3.9	S
Lock-Restart on time	$T_{LRon}$		0.63	0.7	0.77	S
Lock-Restart time ratio1	$R_{LR1}$	$T_{LRoff1} / T_{LRon}$		5		-
Lock-Stop release time2 (Note 10) as from 5 <sup>th</sup> off time	$T_{LRoff2}$		12.5	14	15.5	S
Lock-Restart time ratio2 (Note 10) as from 5 <sup>th</sup> off time	$R_{LR2}$	$T_{LRoff2} / T_{LRon}$		20		-
Thermal shutdown protection detection temperature	$T_{TSD}$	(Design Target)	150	180		$^\circ\text{C}$
Thermal shutdown protection detection hysteresis	$\Delta T_{TSD}$	(Design Target)		40		$^\circ\text{C}$
Over current detection current	$I_{OVC}$			2.5		A
Current limiter	$I_{CL}$		1.8	2.0	2.2	A
REG pin output voltage load regulation	$\Delta V_{regld}$	$I_{REG} = -10\text{ mA}$			50	mV
Hall input bias current	$I_{hin}$	$IN1, IN2 = 0\text{ V}$		0	1	$\mu\text{A}$
Hall input sensitivity	$\Delta V_{hin}$		40			mV
PWM input bias current	$I_{pwmin}$	$V_{DD} = 5.5\text{ V}$ , $PWM = 0\text{ V}$	14	28	42	$\mu\text{A}$
UVLO detection voltage	$V_{uvdet}$	VCC voltage	3.1	3.4	3.6	V
UVLO release voltage	$V_{uvrls}$	VCC voltage	3.3	3.6	3.9	V
UVLO hysteresis voltage	$\Delta V_{uv}$		0.1	0.2	0.4	V
NVM program/erase cycling	$CYC_{NVM}$	w.r.t. $V_{CCNVM}$			10	cycle
NVM data retention	$RET_{NVM}$		10			year

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. When a motor rotates with below 50 rpm (phase change period over 0.3 s), lock protection will work.

9. When a motor can't rotate for 0.7 s after start-up, lock protection will work.

10. When the locked rotor state continues for long time, lock stop period changes as from 5<sup>th</sup> off time.

# LV8316H

## BLOCK DIAGRAM

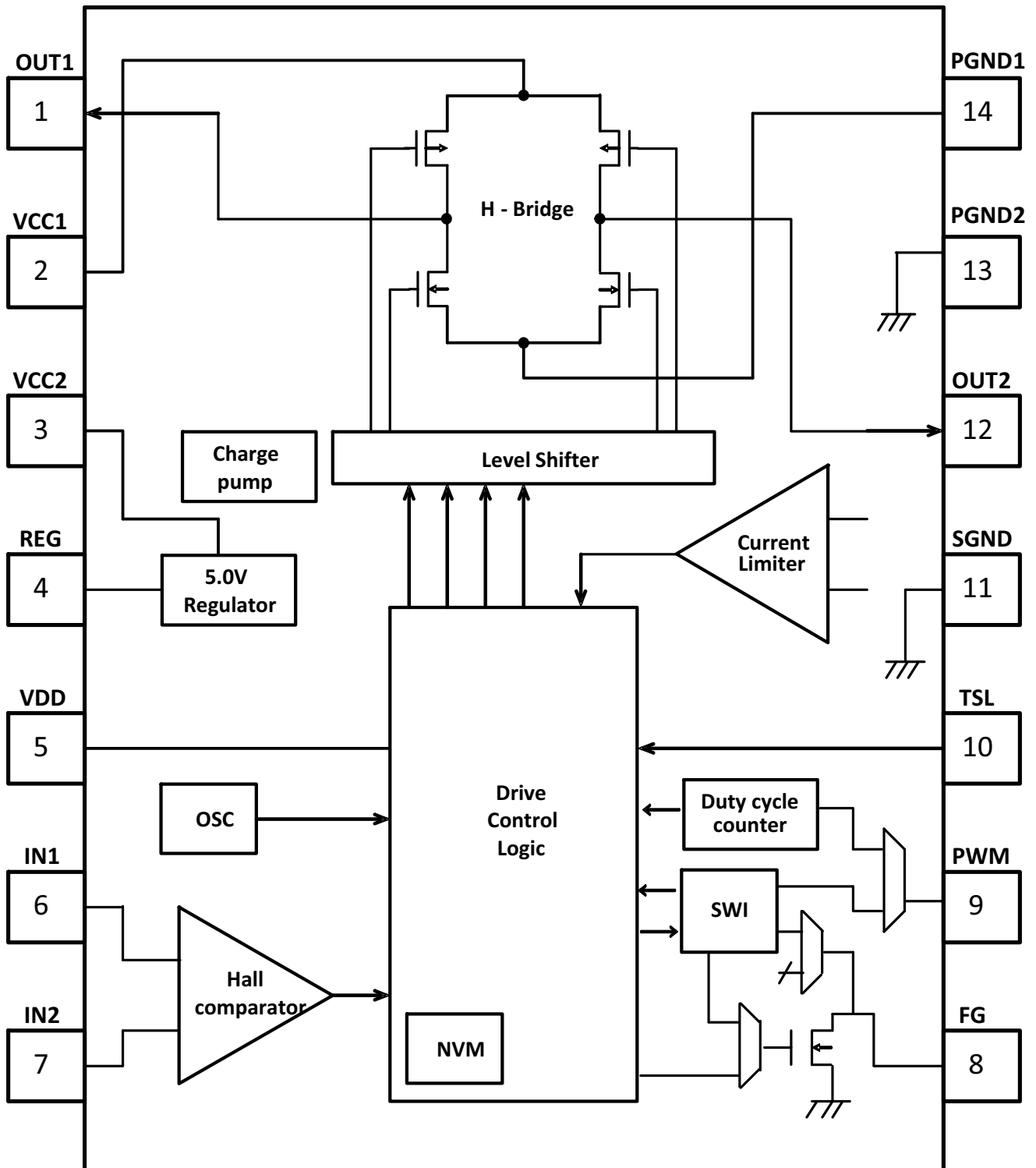
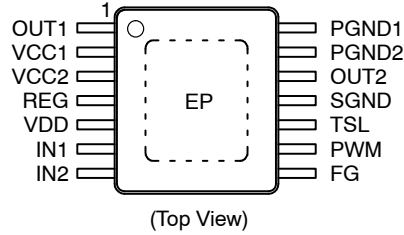


Figure 2. Block Diagram

# LV8316H

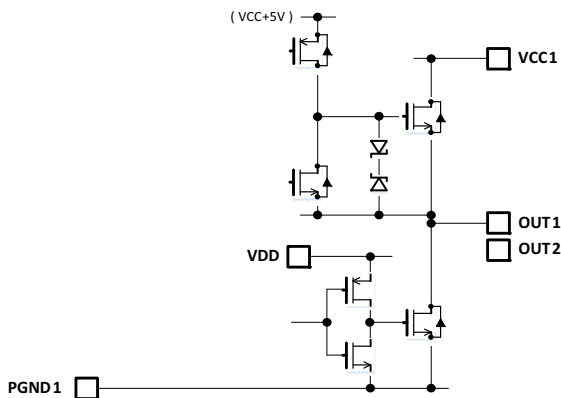
## PIN ASSIGNMENT



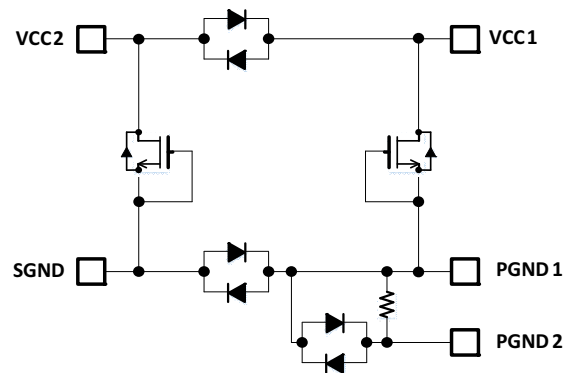
**Table 7. PIN LIST AND FUNCTION**

Pin No.	Pin Name	Description	Equivalent Circuit
1	OUT1	Motor drive output pin. This pin is connected to the built-in power MOSFET.	Figure 3
2	VCC1	Power supply pin for built-in power MOSFET.	Figure 4
3	VCC2	Power supply for internal circuit, ex. pre-driver, charge-pump.	
4	REG	5.0 V regulator output pin. This voltage acts as a power source for oscillator, protection circuits, and so on. The maximum load current of REG is 20 mA. Be sure not to exceed this maximum current.	Figure 5
5	VDD	Power supply pin for logic circuit. This pin should be connected to REG pin normally in use.	Figure 6
6	IN1	Hall sensor input pin. The differential outputs of the hall sensor need to be connected to IN1 and IN2 each.	Figure 7
7	IN2		Figure 8
8	FG	The FG (frequency generator) output controls the motor electrical rotational speed (FG output synchronizes with the Hall sensor signal). This pin can function as RD (rotation detection) by bit setting of Reg. 0x010C "TACHSEL". The FG pin is an open drain output. Recommended pull up resistor is 1 kΩ to 100 kΩ. Leave the pin open when not in use. Parameter setting through the communication, is performed by the pin use.	Figure 9
9	PWM	Rotational control signal input pin. The rotational speed is controlled by duty-cycle of the pulse and is proportional to the duty-cycle ratio. Parameter setting through the communication is performed by this pin.	Figure 10
10	TSL	Communication input selection and internal test mode pin. When short to GND, FG pin is serial in/out. When short to REG, PWM pin is serial in and FG pin is for serial out.	Figure 11
11	SGND	Internal circuit ground pin.	Figure 4
12	OUT2	Motor drive output pin. This pin is connected to the built-in power MOSFET.	Figure 3
13,14	PGND1 PGND2	Power ground pin. This pin has to tolerate surge current.	Figure 4

## EQUIVALENT CIRCUIT



**Figure 3. OUT1 and OUT2 Equivalent Circuit**



**Figure 4. VCC1,2/PGND1,2/SGND Equivalent Circuit**

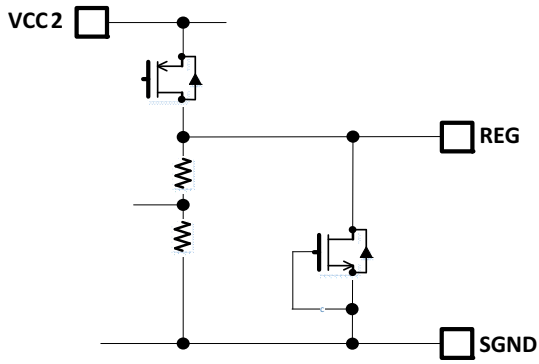


Figure 5. REG Equivalent Circuit

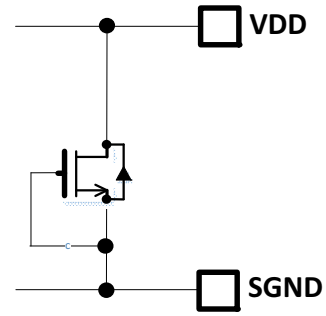


Figure 6. VDD Equivalent Circuit

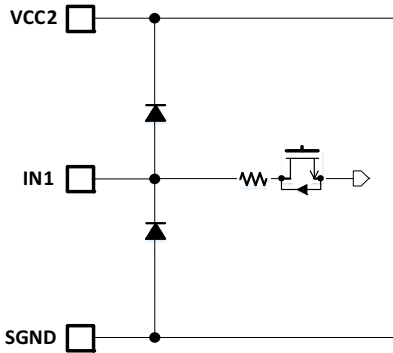


Figure 7. IN1 Equivalent Circuit

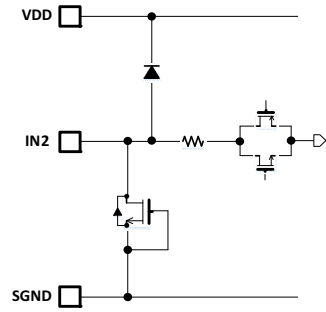


Figure 8. IN2 Equivalent Circuit

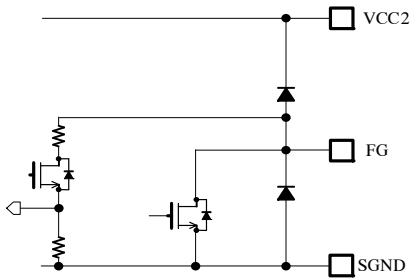


Figure 9. FG Equivalent Circuit

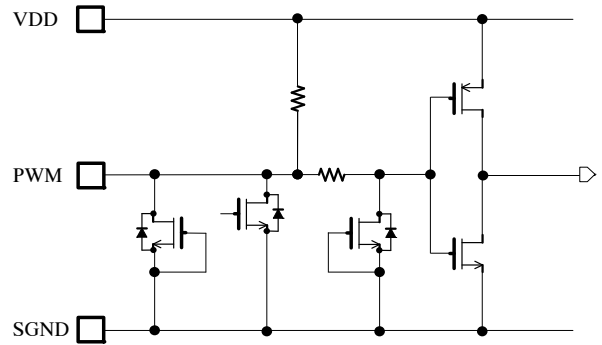


Figure 10. PWM Equivalent Circuit

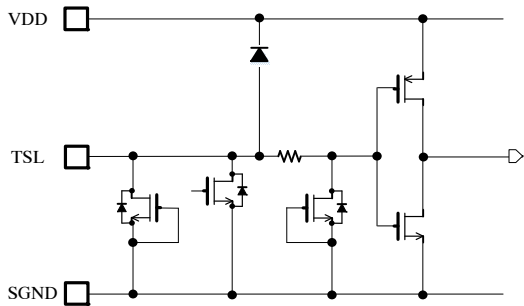


Figure 11. TSL Equivalent Circuit



OPERATION DESCRIPTION

The LV8316H has various functions and parameters which are defined by built-in registers. Refer to the Register map and description page for the detail.

**Spin-up Sequence**

To spin-up a motor, power is applied to VCC pin, and the appropriate input PWM signal (see “DUTY\_L” and “DUTY\_S” setting description in section “Steady rotation”) is applied to PWM pin. The LV8316H starts driving the motor whose current direction is determined by the Hall sensor signal. To avoid the unnecessary rush current, the “soft start” mode is provided, which gradually increases output duty-cycle. After the soft start mode, LV8316H goes to steady rotation mode. The detail of the soft start mode and steady rotation mode are described in the sections below.

If a motor already rotates at the power on in faster speed than 304 rpm, the soft start mode is skipped and goes to steady rotation mode immediately.

**Soft Start**

For soft start mode, the duty-cycle ramp up profile is defined by the initial duty-cycle, slope, and exit condition. The initial duty-cycle is fixed and it starts from 4%. The slope is programmable. It is determined by registers “ENDPWM” and “INCTIM”. The duty-cycle is increased up to the end duty-cycle “ENDPWM” for duration time “INCTIM”. The end duty-cycle is selectable at 24% or 80% (see Table 8). The duration time can be selected from 0.0002 sec to 15.2 sec (see Table 9). The exit condition means it’s in the state of either the duty cycle reaching ”ENDPWM” or that the rotational speed is reaching the exit target speed specified by the register “RELLEV” (see Table 10). Soft start operation requires at least 8 electrical cycles (4 mechanical cycles in case of 4 poles single phase) independent on the exit condition.

**Table 8. SOFT START END DUTY-CYCLE**

ENDPWM	End Duty-cycle
0	24% output duty-cycle
1	80% output duty-cycle

**Table 9. SOFT START DURATION TIME**

INCTIM			Duration Time (s)	
[2]	[1]	[0]	ENDPWM = 1 (End duty-cycle = 80%)	ENDPWM = 0 (End duty-cycle = 24%)
0	0	0	0.15	0.0002
0	0	1	0.76	0.48
0	1	0	1.51	0.96
0	1	1	2.28	1.50
1	0	0	3.04	2.00
1	0	1	4.56	3.00
1	1	0	7.60	5.00
1	1	1	15.2	10.0

**Table 10. SOFT START EXIT TARGET SPEED**

RELLEV	Exit Target Speed
0	97% of target speed determined by input PWM duty-cycle
1	500 rpm

To avoid overshoot at the transition from soft start to the steady rotation mode, the release condition is set to 97% of the target speed in case of RELLEV=0.

Figures 12 and 13 show the image of soft start mode.

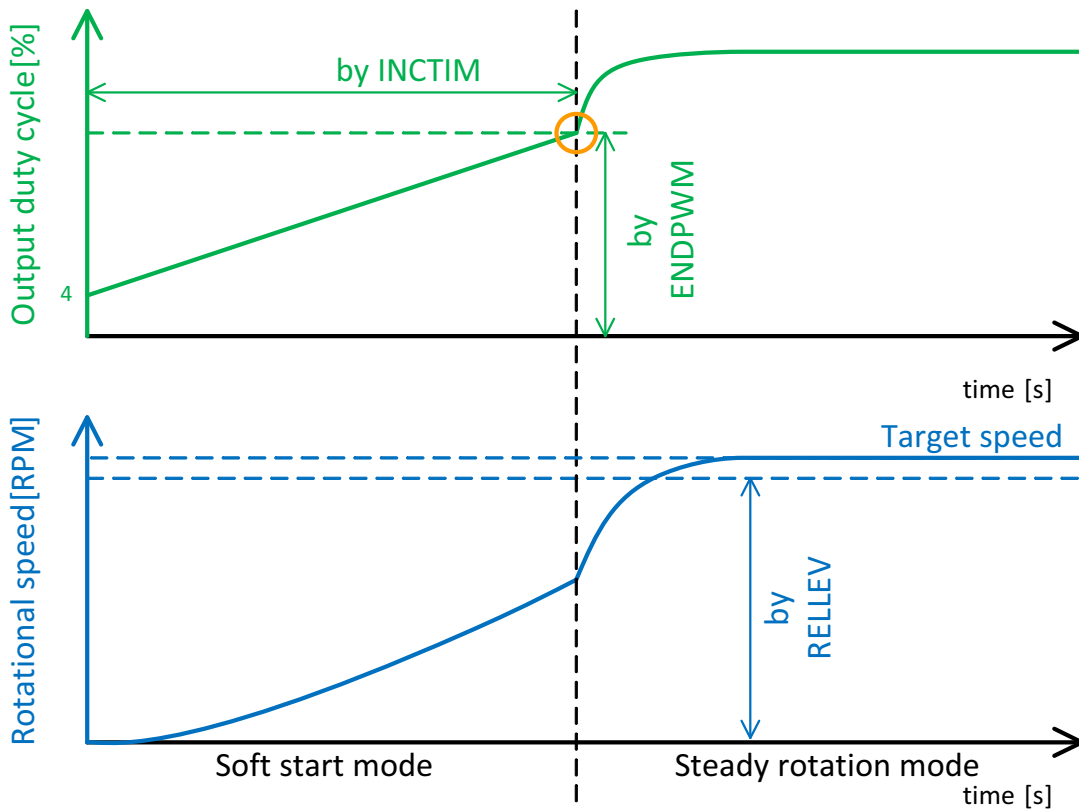


Figure 12. The Image of Soft Start Exit by End Duty-cycle

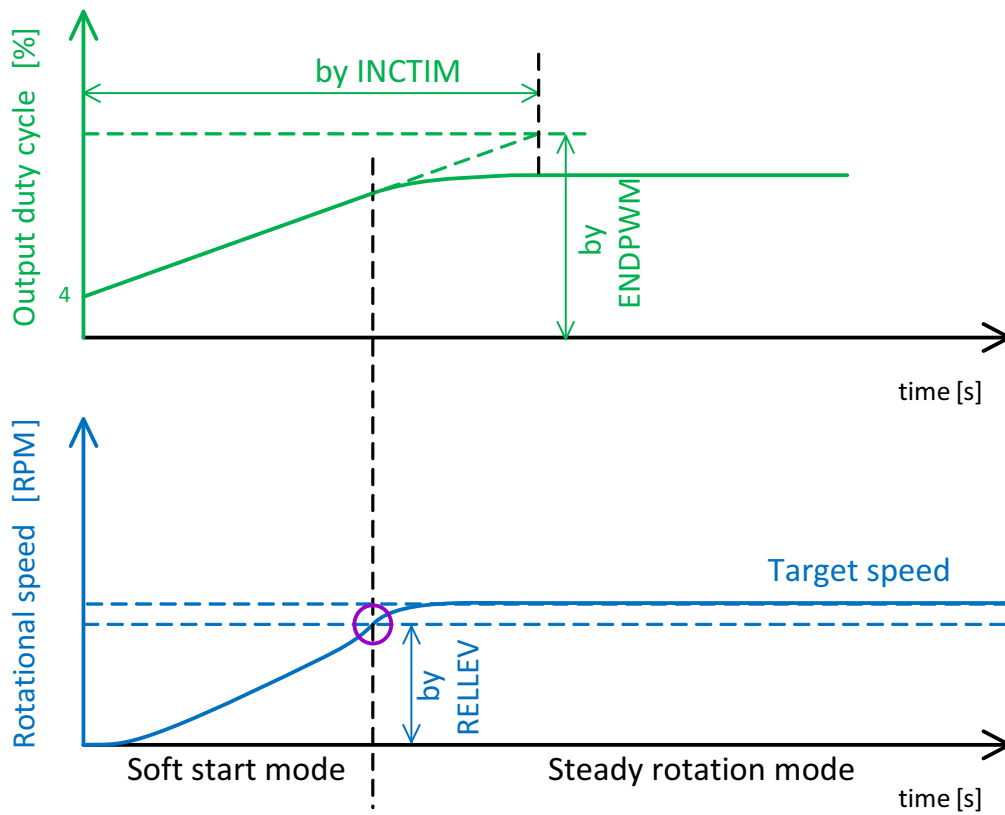


Figure 13. The Image of Soft Start Exit by Target Speed

## LV8316H

As the green curve shown in Figure 12, the output duty-cycle in the soft start mode starts from 4% of the output duty. Then the output duty-cycle is increased to the end duty-cycle linearly, which is shown by yellow circle. After that, LV8316H goes to the steady rotation mode. Figure 13

shows the case which the rotational speed reaches the exit target speed before the output duty-cycle reaches to the exit condition.

Figure 14 is the example of the duration time in case of "ENDPWM = 0".

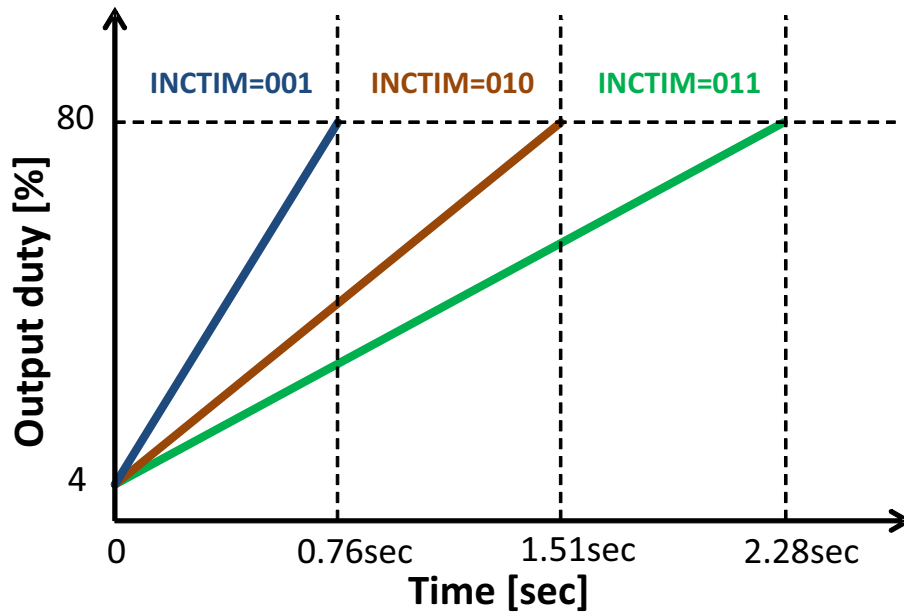


Figure 14. Example: The Image of Soft Start Duration Time

**Steady Rotation**

The rotational speed is controlled by built-in PI closed loop speed control function. The target rotational speed is defined by input PWM pin.

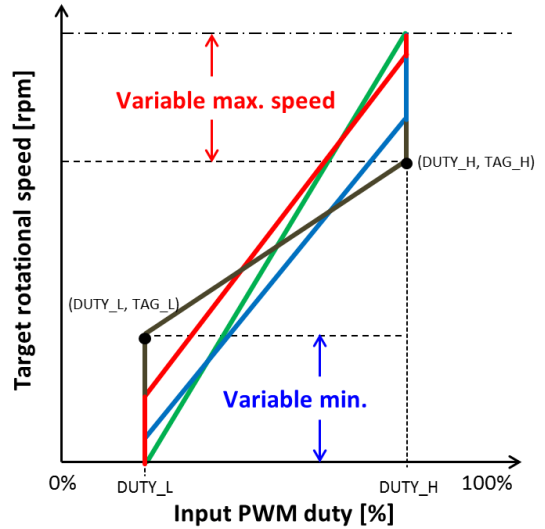
The input PWM frequency range is 25 Hz–100 kHz. The output frequency is fixed to 48 kHz and it is not related to input PWM frequency. Figure 15 shows the speed control profile which is relationship between input PWM duty-cycle and the target rotational speed. Registers to determine this relationship are;

- TAG\_L (Address 0x0100 D [7:0]): Minimum target rotational speed
- TAG\_H (Address 0x0101 D [7:0]): Maximum target rotational speed
- DUTY\_L (Address 0x0102 D [7:0]): Minimum input duty-cycle
- DUTY\_H (Address 0x0103 D [7:0]): Maximum input duty-cycle
- FULL (Address 0x0109 D [2]): Speed selection at input duty-cycle over DUTY\_H
- DUTY\_S (Address 0x0109 D [3:0]): Speed selection at input duty-cycle under DUTY\_L

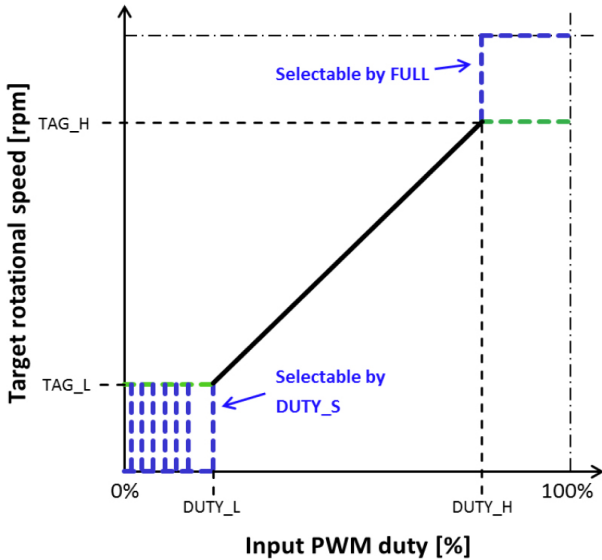
The detail of each register will be explained later.

**TAG\_L/TAG\_H: Minimum/Maximum Target Rotational Speed Setting**

The minimum speed is set by “TAG\_L” and the maximum speed is set by “TAG\_H” within the range of DUTY\_L and DUTY\_H. (See Figure 16.)



**Figure 16. Max/Min Speed Setting**



**Figure 15. Speed Control Profile**

Table 11 and Table 12 shows the list of RPM that can be used for speed setting

Do not set the maximum speed setting (TAG\_H) less than the minimum speed setting (TAG\_L).



**DUTY\_L/DUTY\_H: Minimum/Maximum Input Duty-cycle Setting**

The range of PWM input duty-cycle can be set by the registers “DUTY\_L” and “DUTY\_H” whose range is 0 to 100%. The equation of resolution is

$$D_{min} = \frac{DUTY\_L}{255} \times 100 [\%] \quad (eq. 2)$$

$$D_{max} = \frac{DUTY\_H}{255} \times 100 [\%] \quad (eq. 3)$$

Where  $D_{min}$  is minimum input duty-cycle  
 $D_{max}$  is maximum input duty-cycle  
 Do not set “DUTY\_H” less than “DUTY\_L”.

Figure 17 shows the relationship between input duty-cycle and target rotational speed. TAG\_L/TAG\_H define the start and end points of the speed curve and the value between (DUTY\_L, TAG\_L) and (DUTY\_H, TAG\_H) are interpolated linearly.

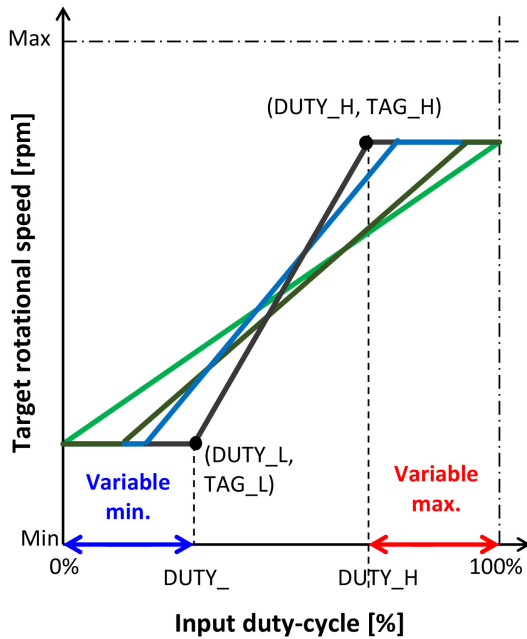


Figure 17. Input Duty-cycle Setting

**FULL: Speed Selection at Input Duty-cycle over DUTY\_H**

For the behavior at input duty-cycle which is over DUTY\_H, the register “FULL” provides two options. FULL = 0 is to keep the speed specified by “TAG\_H” and FULL = 1 is to go to 100% output duty-cycle as shown in Figure 18.

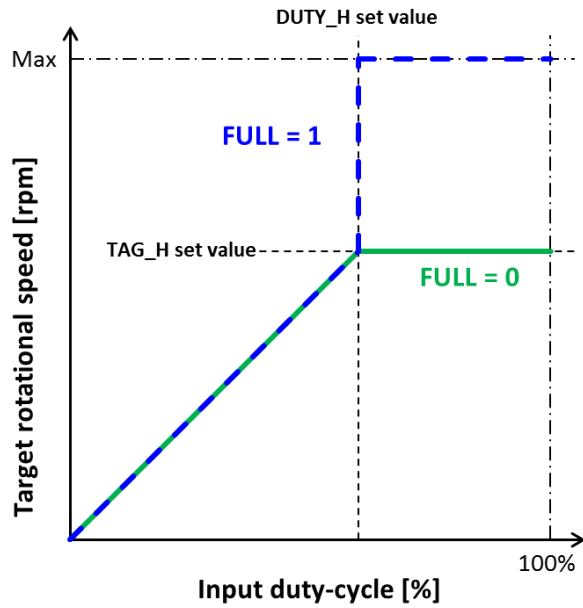


Figure 18. Max Speed Function Setting

**DUTY\_S: Speed Selection at Input Duty-cycle under DUTY\_L**

For the behavior at input duty-cycle less than DUTY\_L, the register “DUTY\_S” provides several options. The “DUTY\_S” sets the input duty cycle of the motor speed to 0 rpm. It is calculated by equation 4, except for the case of “DUTY\_S” = 15.

$$D_0 = \frac{5 \times DUTY\_S}{255} \times 100 [\%] \quad (eq. 4)$$

Where  $D_0$  is input duty-cycle of the motor speed 0 rpm  
 Table 13 shows the option of “DUTY-S”

Table 13. THE SETTING OF DUTY\_S

DUTY_S	Motor Stop Duty Setting (%)
0	0
1	1.9
2	3.9
3	5.8
4	7.8
5	9.8
6	11.7
7	13.7
8	15.6
9	17.6
10	19.6
11	21.5
12	23.5
13	25.4
14	27.4
15	The value of DUTY_L

## LV8316H

When DUTY\_S = 15, the threshold duty-cycle is same as the “DUTY\_L” setting.

When DUTY\_S = 1 to 14, the motor speed keeps “TAG\_L” setting from “DUTY\_L” to “DUTY\_S” and goes to 0 rpm at defined by equation 1.

When DUTY\_S = 0, the motor speed keeps “TAG\_L” setting whenever input duty-cycle is less than “DUTY\_L”.

If “DUTY\_L” setting is smaller than “DUTY\_S” setting, the threshold is same as “DUTY\_L” setting.

To restart the motor rotation, the input duty-cycle must be set higher than “DUTY\_S” + 1.6% (i.e. the hysteresis is 1.6%).

Figure 19 shows the speed curves for various “DUTY\_S”.

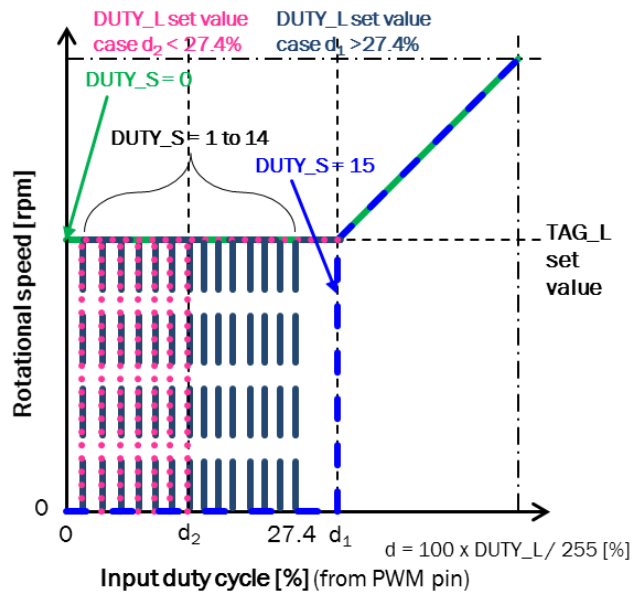


Figure 19. Min Speed Function Setting

**Output Waveform**

The output pulse signal is about 0 V – VCC and its duty is controlled by built-in PI closed loop speed control function. The duty before commutation change decreases

gradually to 0% and the duty after commutation change increases gradually to the duty level controlled by speed control function by built-in function called Soft Switch. This state is shown in Figure 20 as a schematic view.

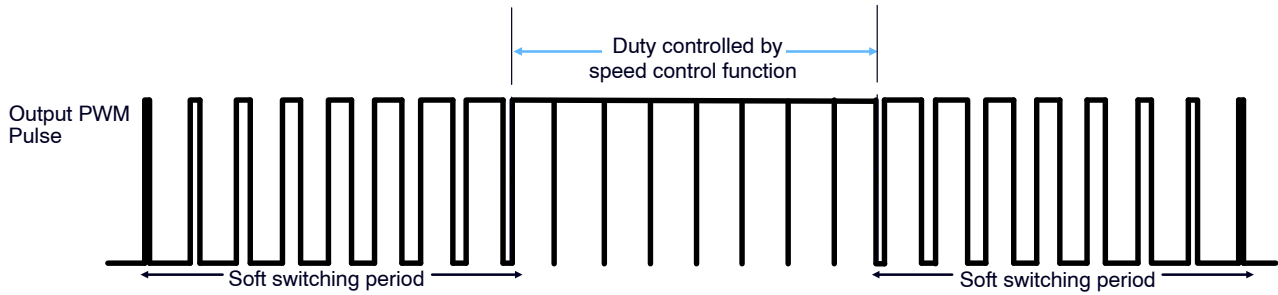


Figure 20. Output Waveform Image

**Soft Switch Setting**

The LV8316H can adjust Soft switch period as the ratio of L and S shown in Figure 21. It is defined by following equation and Register “SSWHIGH” and “SSWLOW” can adjust it.

$$\text{Soft switch width [\%]} = \frac{S}{L} \times 100$$

where:

S is Soft Switch period

L is one commutation period

Figure 21 shows the soft switch image.

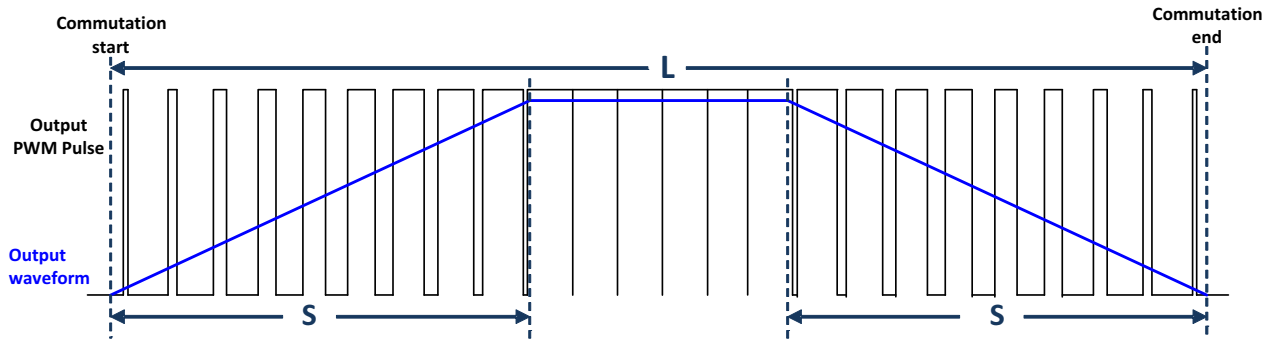


Figure 21. Soft Switch Image

SSWHIGH is for the maximum target rotational speed defined by TAG\_H and SSWLOW is for the minimum target rotational speed defined by TAG\_L. Each register has 4bits and Table 14 shows the adjustable value.

Table 14. SOFT SWITCH WIDTH ADJUSTMENT

Register	S/L ratio	Register	S/L ratio
0000	2.9%	1000	26.4%
0001	5.9%	1001	29.3%
0010	8.8%	1010	32.2%
0011	11.7%	1011	35.2%
0100	14.6%	1100	38.1%
0101	17.6%	1101	41.0%
0110	20.5%	1110	43.9%
0111	23.4%	1111	46.9%

Once “SSWHIGH” and “SSWLOW” is set, the ratio of Soft Start in other speed is interpolated linearly as shown in Figure 22.

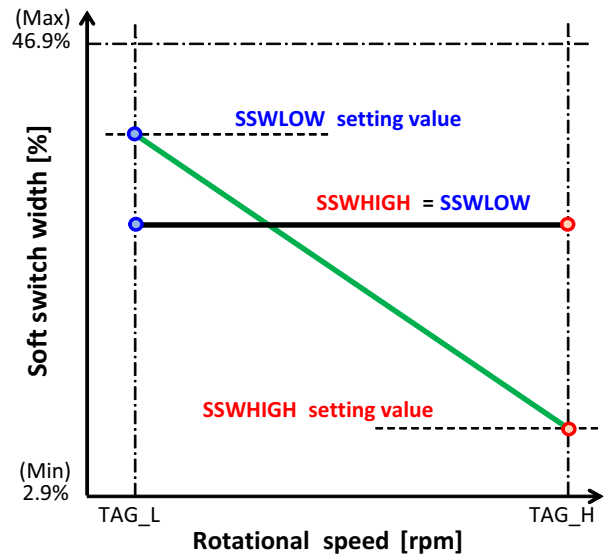


Figure 22. The Relationship Between Soft Switch and speed Target Rotational Speed



# LV8316H

## FG Output

FG signal output is decided by the Hall signal cross point. The relationship between motor speed and FG frequency represents the following equation.

$$f_{FG}[\text{Hz}] = \frac{N}{60} \times \frac{p}{2}$$

Where N: Motor speed [rpm]  
p: Number of Pole

Figure 23 shows the timing chart of the hall sensor output and the FG output.

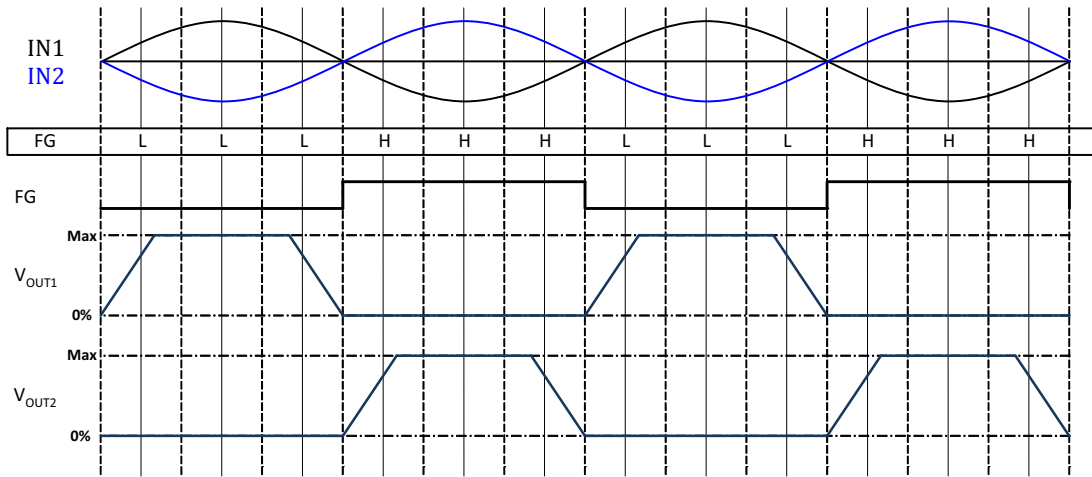


Figure 23. Timing Chart of Output

## Lead Angle Setting

In the output, the output current delays from the output voltage because of the inductance of motor coil. The output current which flows in a motor coil generates torque for the motor and the torque is maximized by the synchronization of output current with the BEMF phase. Therefore, this delay decreases an efficiency of motor rotation. It is generally increased in proportion to the rotational speed.

The LV8316H can cancel the delay by earlier commutation than the Hall sensor signal as shown in Figure 24. This phase adjustment is called “Lead-angle”.

In Figure 24, the output voltage VOUT1 and the output current IOUT1 in black are changed to the waveform in red after the Lead-angle adjustment and it is the most optimum commutation timing.

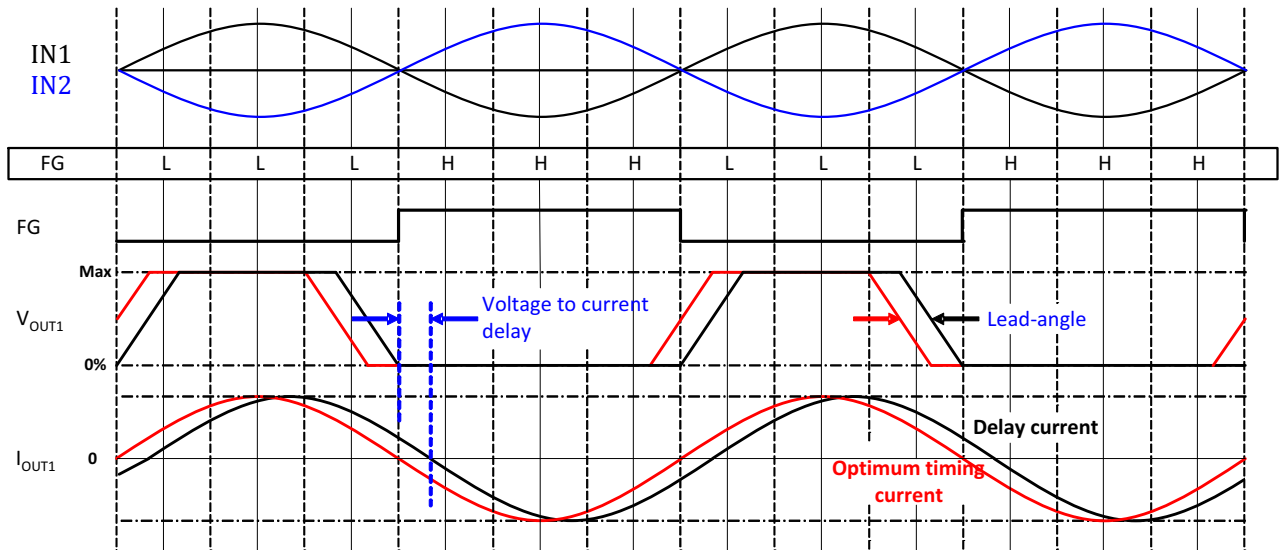


Figure 24. The Relationship between the Lead-angle and the Delay of Output Current

The relationship between rotational speed and Lead-angle is shown in Figure 25. The optimum Lead-angle will vary by the motor characteristics so it is necessary to adjust the Lead-angle based on the motor in use.

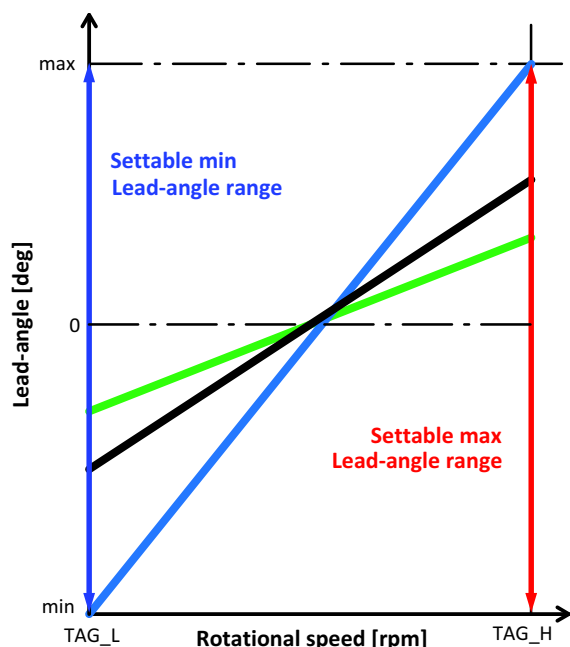


Figure 25. Lead-angle Curve Image

The LV8316H can set the Lead-angle at maximum target rotational speed (TAG\_H) and at minimum target rotational speed (TAG\_L) by “DLDEG\_H” and “DLDEG\_L” individually.

These register have 8 bits D[7:0] in each and both MSBs define the direction of phase delay. When MSB sets to “0”, the Lead-angle is set to minus value which means phase delay, that is, the output voltage commutation is delay than the Hall sensor signal. When MSB sets to 1, the Lead-angle is set to plus value which means phase advance, that is, the output voltage commutation is earlier than the Hall sensor signal. The resolution is approximately 0.175°. Hence, the adjustable range is from -22.225° to 22.225° expressed in the following equation.

$$L_{max} = \frac{22.225}{127} \times DLDEG\_H \text{ [deg]}$$

$$L_{min} = \frac{22.225}{127} \times DLDEG\_L \text{ [deg]}$$

where:

Lmax: Lead-angle at max. target rotational speed (TAG\_H)

Lmin: Lead-angle at min. target rotational speed (TAG\_L)

Once DLDEG\_H and DLDEG\_L are set, the Lead-angle in other speed is set to interpolated and extrapolated value according to the rotational speed, even though the rotational speed is defined by FULL = 1.

## PROTECTIONS

The LV8316H has the following protection functions

- TSD (Thermal Shut Down)
- UVLO (Under Voltage Lock Out)
- Lock protection
- CLM (Current Limiter)
- OCP (Over Current Protection)

When the TSD or Lock protection works, all of the internal FETs are turned off. When UVLO or CLM works, the output PWM is off and the motor goes to re-circulation mode.

### Thermal Shutdown Protection (TSD)

When LV8316H’s junction temperature rises to 180°C, TSD will activate and turns off high-side and low-side Power FET. Therefore, OUT1 and OUT2 pins will become high impedance and the coil current will shut off. When it falls under 140°C, TSD will deactivate and motor will start to rotate.

### Under Voltage Lock Out (UVLO)

When VCC voltage goes to low level (3.4 V), UVLO will activate and stop the motor. It is cleared when VCC voltage recovers over 3.6 V.

The TRUTH TABLE of UVLO is as shown in Table 15.

Table 15. UVLO TRUTH TABLE

Input		Register	Output	
IN1	IN2	DRVMODE	OUT1	OUT2
L	H	00 / 01	L	Hi-Z
H	L	00 / 01	Hi-Z	L
L	H	10 / 11	Hi-Z	H
H	L	10 / 11	H	Hi-Z

### Lock Detection and Lock Protection

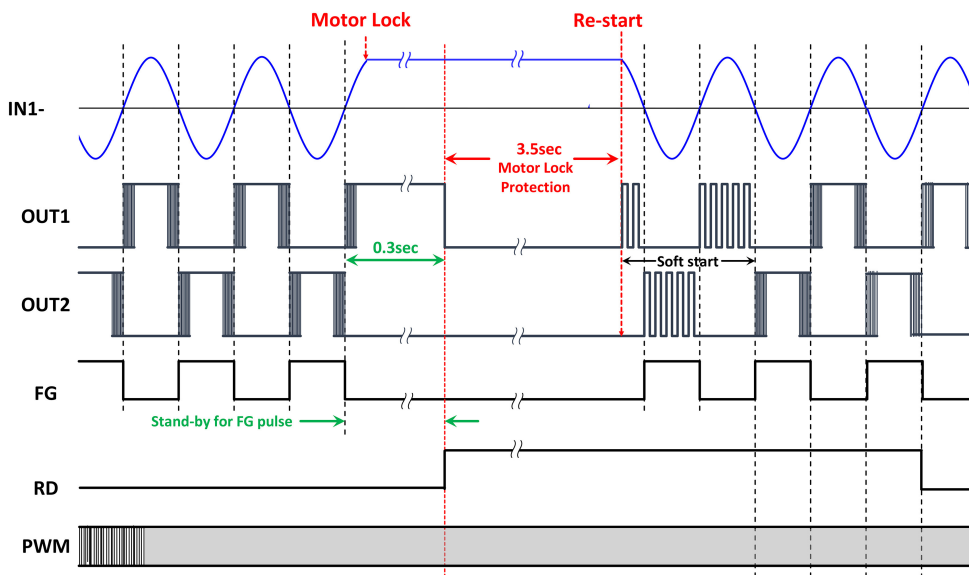
When the motor is locked, the heat is continuously generated because the IC keeps trying to rotate the motor.

The lock protection works to prevent such a heat generation by turning off the motor current. When a motor is locked in the steady rotation mode and IC doesn’t detect the FG edge for more than 0.3 s which is equivalent to 50 rpm, the lock protection works (Figure 26).

The lock protection signal can be output from FG pin by setting the register “TACHSEL”. Please see Table 20. In this mode, the RD signal goes to “High”, though it is “Low” at motor starts.

When the motor restarts and IC detects 4 phase changes at least (depends on rotation speed), the RD signal goes to “Low”.

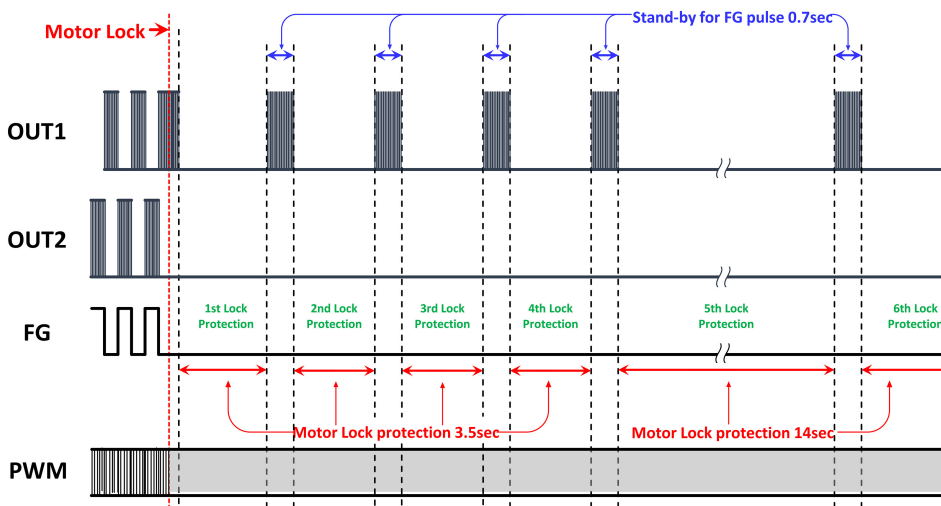
# LV8316H



**Figure 26. Timing Chart of the Lock Protection**

Figure 27 shows the relationship between protection period and the number of protection times. 1<sup>st</sup> to 4<sup>th</sup> protection period take 3.5 s and 5<sup>th</sup> protection period takes 14 s. To reset the lock protection mode, Stop duty cycle must

be applied to the PWM input signal. To retry the motor rotation, Proper duty cycle must be applied to the PWM input signal.

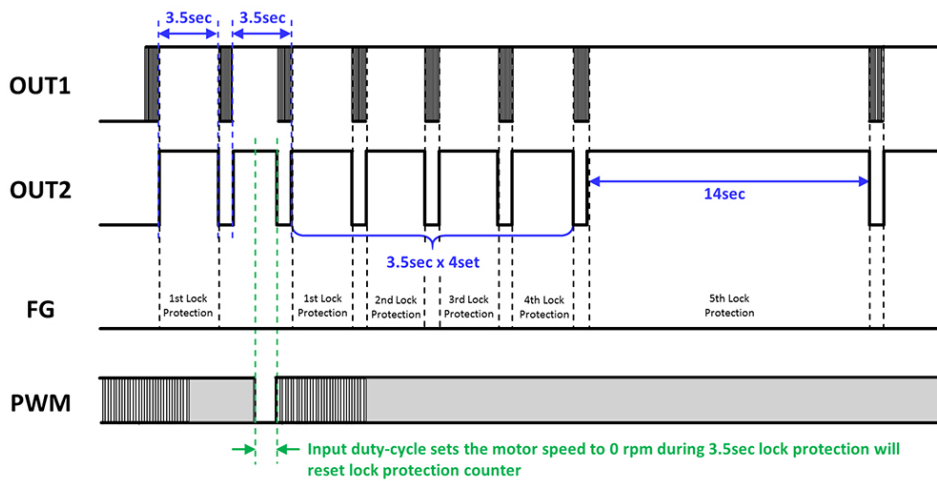


**Figure 27. The Relationship between Protection Time and Number of Times Protection**

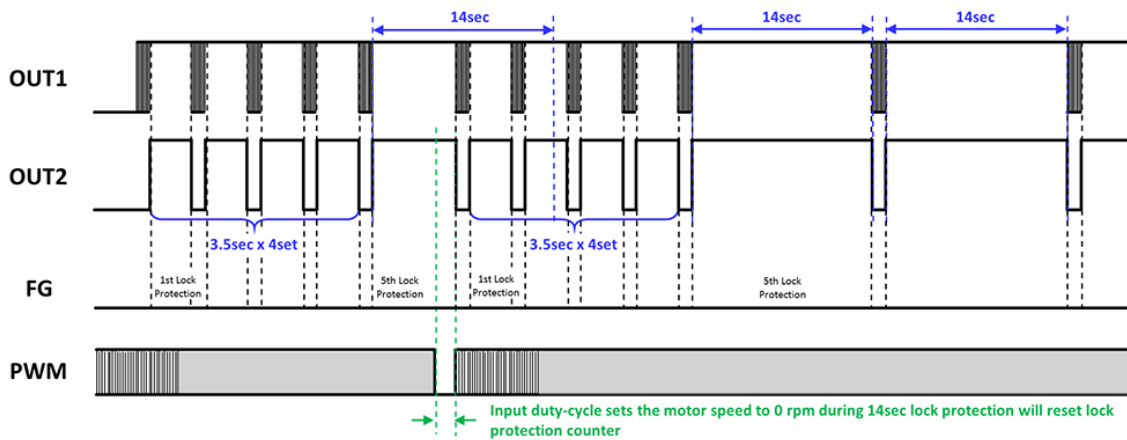
These protection periods and the number of protection times are applied in accordance with the internal counter. It will reset the counter if the duty-cycle which sets the motor speed to 0 rpm determined by “DUTY\_L” and “DUTY\_S” is entered during lock protection period (in either 3.5 sec or

14 sec). In this case, the lock protection counter will activate from the initial state starting from PWM Pos-Edge and protection period will start from 1<sup>st</sup> time as shown in Figure 28 and Figure 29.

# LV8316H



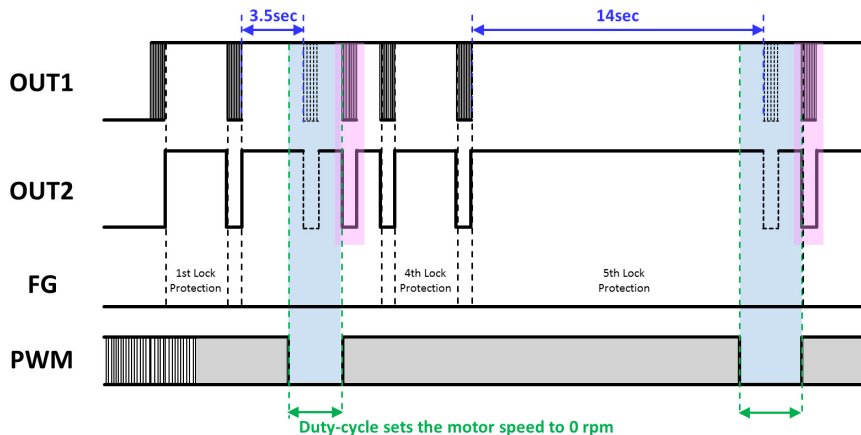
**Figure 28. Lock Protection Counter Reset during 3.5 sec Lock Protection Period**



**Figure 29. Lock Protection Counter Reset during 14 sec Lock Protection Period**

The lock protection period is changed by the condition of output signal. If the duty-cycle which sets motor speed to 0 rpm is input and the output signals are disappeared during the restart period in lock protection period as shown in light blue in Figure 30, the counter is not reset and the remaining

restart period is applied immediately when PWM Pos-Edge will be input as shown in pink in Figure 30. In this case, the protection period is not related to the internal lock protection timer and protection period is not fixed to 3.5 sec or 14 sec.



**Figure 30. In Case of Having Changes in Protection Period**

# LV8316H

## Current Limiter (CLM)

When the coil current becomes large, CLM will activate and then output will be in the re-circulation state. The current is monitored by internal sensing resistance and the threshold is 2.0 A (typ.).

There are three registers related to the current limiter function. The first one is CL\_SKIP which can set the period of protection operation when CL is detected. The second one is CL\_ASYNC. When “1” is set to this register while CL is active, synchronous rectification of the output becomes disabled. The third one is OCP\_MASK which sets the masking time to ignore upper and lower FET’s reverse recovery. See Table 20 for more details.

## Overcurrent Protection (OCP)

OCP monitors the coil current by internal sensing resistance and if it becomes larger than 2.5 A (typ) even if CLM is activated, OCP will activate and motor driver will stop.

Register called OCP\_LAT\_CLR allows to select behavior when OCP is activated. One is to keep the motor stopped until the next power on sequence, and the other one is to activate Lock protection mode. See Table 20 for more details.

## NONVOLATILE MEMORY

The LV8316H has internal nonvolatile memory which can store register values which define various parameters and settings. The stored register values will be reloaded at POR shown as Figure 31. LV8316H has also the communication mode. It allows user to modify register values, and to store them to the nonvolatile memory (Figure 31). It doesn’t need the resistors as like the conventional models to set the various review In addition, PCB design becomes simpler.

Here is a list of the main configurable items.

- Max/Min rotational speed.

- Max/Min input duty-cycle.
- Lead-angle
- Soft start
- Speed control slope

Program/Erase to the memory is performed through a built-in register. Please note that Program/Erase is allowed for 10 times only. For more detail, please see the application note NVM Programming Procedure.

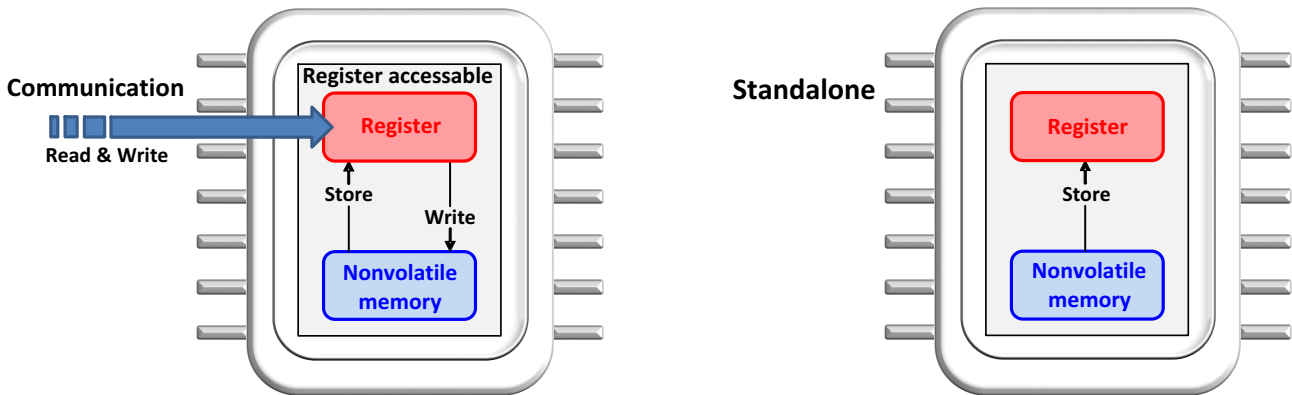


Figure 31. Image of Internal Register and Nonvolatile Memory

## SERIAL INTERFACE

The LV8316H allows communication via UART (Universal Asynchronous Receiver Transmitter). Various parameter registers can be accessed through UART communication.

UART is one to one communication and the LV8316H doesn’t support parallel access to the multiple devices, so be sure to turn on only the target devices.

The LV8316H provides two UART modes, a one-wire mode and a two-wire mode. In one-wire mode, the FG pin is used for both input and output. In two-wire mode, the FG

pin is used as output and the PWM pin is used as input. The state of the TSL pin defines the UART mode as shown in Table 16.

Table 16. I/O PIN CONDITION IN UART MODE

	One-wire Mode	Two-wire Mode
TSL pin	Pull down (GND)	Pull-up (VDD)
Communication Pin	FG pin (For Read and Write)	PWM pin (For Write) FG pin (For Read)

## LV8316H

Figure 32 shows the connection image of one-wire mode. The communication line FG should be open-drain type because it supports duplex mode. Therefore the communication pin of the MPU or CPU must be an

open-drain output. Figure 33 shows the connection image of two-wire mode. Please refer to the Application note [AND9761/D](#) for more detail.

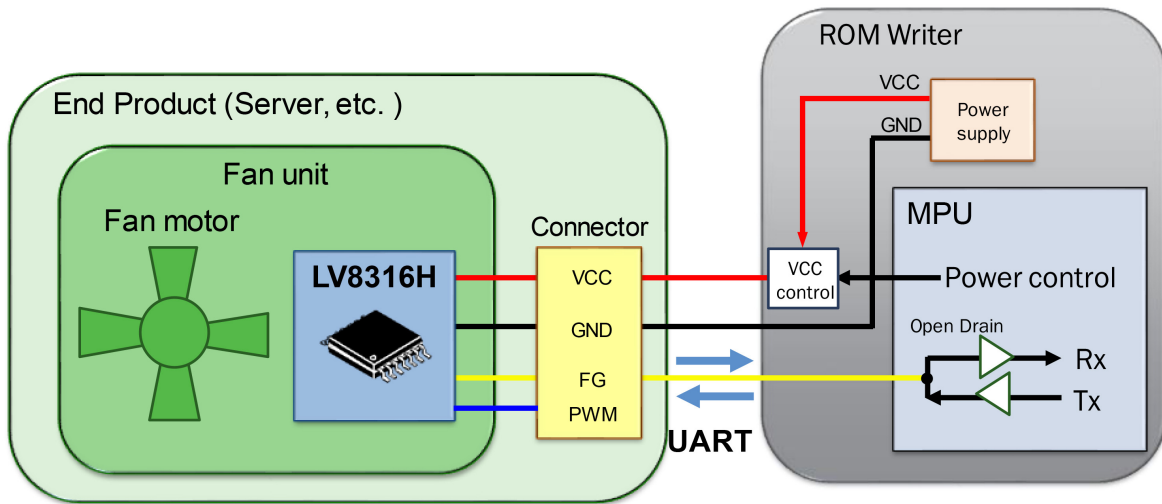


Figure 32. Connection Image of One-wire Mode

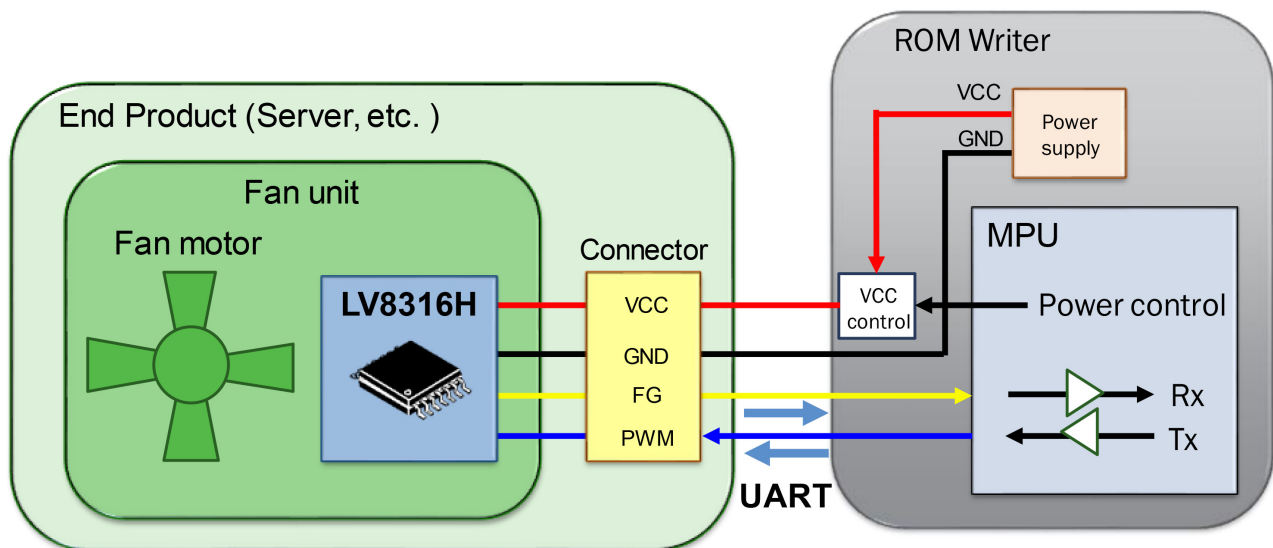


Figure 33. Connection Image of Two-wire Mode

About the detail of communication protocol, please see the Application note, [AND9761/D](#).

# LV8316H

## REGISTER MAP

### Register MAP

Internal register map can be classified into four types as shown in Table 17.

- Read only
- Read/Write, User defined registers to be written to nonvolatile memory.
- Read/Write
- Write only (Auto clear)

**Table 17. REG. MAP 1 (Address 0x000 – 0x0114)**

Address	Key	Initial	Register								
			D7	D6	D5	D4	D3	D2	D1	D0	
0x0000	Free	0xAA	1	0	1	0	1	0	1	0	
0x0001		0x55	0	1	0	1	0	1	0	1	
0x0002		0x00					0	0	RECALC_EN	RELOAD_EN	
0x0003		0x00								RELOAD	
0x0004		0x00								RECALC	
0x0005		0x75	Identification number								
0x0100	Free	0x15	TAG_L[7:0]								
0x0101		0x63	TAG_H[7:0]								
0x0102		0x19	DUTY_L[7]	DUTY_L[6:0]							
0x0103		0x65	DUTY_H[7]	DUTY_H[6:0]							
0x0104		0x00	DLDEG_L[7:0]								
0x0105		0x8B	DLDEG_H[7:0]								
0x0106		0x6F	SSWHIGH[3:0]				SSWLOW[3:0]				
0x0107		0x01					0	PWMIN_INV	DRVMODE[1:0]		
0x0108		0x0A	DWNSET	FULL	SS_SW_SEL	RELLEV	ENDPWM	INCTIM[2:0]			
0x0109		0x0F					DUTY_S[3:0]				
0x010A		0x00							0	DTIME[0]	
0x010B		0x0E				0	CL_SKIP	CL_ASYNC	OCP_LAT_CLR	STEPSEL	
0x010C		0x00							0	TACHSEL[0]	
0x010D		0x02							PWMAV[1:0]		
0x010E		0x00					0	0	OCP_MASK[1:0]		
0x010F		0x00			0	0	0	0	ON INTERNAL	0	
0x0110		0x00					LOCK FAULT	0	0	0	
0x0111		0x20	MSKDEG_TP[3:0]				0	0	0	0	
0x0112		NA	RESERVED								
0x0113		0xB0	IX[3:0]				0	IG[2:0]			
0x0114	0x20	0	PX[2:0]			0	PG[2:0]				

**Table 18. REG. MAP 2 (Address 0x0219)**

Address	Key	Initial	Register							
			D7	D6	D5	D4	D3	D2	D1	D0
0x0219	Free	0x00		SWI_ERR[6:0]						

Registers in the black cells do not exist. Therefore, these registers cannot be written and the read values are always zero. The bits with numeric values (0 or 1) must remain as-is.

There are some register addresses which contain both the bits stored in NVM and the bits not stored in NVM. Confirm the bit types to save the data to NVM.

# LV8316H

## REGISTER DESCRIPTION

**Table 19. REGISTER ADDRESS 0x0000–0x0005 Register Description 1**

Function	Address	Bits	Register Name	Description
Fixed register 1	0x0000	[7:0]	–	Data of 0xAA are stored. (Read only)
Fixed register 2	0x0001	[7:0]	–	Data of 0x55 are stored. (Read only)
Enable re-calculation	0x0002	[1]	RECALC_EN	This register enable re-calculation of Speed/Lead Angle/Soft SW setting. 0 : Disable 1 : Enable
Register re-loading (memory to register)	0x0002	[0]	RELOAD_EN	This register enables data reloading from NVM. 0 : Disable 1 : Enable
	0x0003	[0]	RELOAD	When this bit is set to 1, data reloading from NVM is executed while RELOAD_EN is set to 1. This register is auto clear type.
Trigger of re-calculation	0x0004	[0]	RECALC	When this bit set 1, re-calculation of Speed/Lead Angle/Soft SW setting is executed while RECALC_EN is set to 1. This register is auto clear type.
Device ID	0x0005	[7:0]	ID_NUMBER	Data of device ID are stored. (Read only)

**Table 20. REGISTER ADDRESS 0x0100–0x0114 Register Description 2**

Function	Address	Bits	Register Name	Description
Minimum speed setting	0x0100	[7:0]	TAG_L	This register sets minimum/maximum rotational speed. 0000 0000: 0/300rpm (Min / Max) 1111 1111: 10400/36000rpm (Min / Max)  *Refer to the section “Steady Rotation” for details.
Maximum speed setting	0x0101	[7:0]	TAG_H	
Minimum input duty cycle setting	0x0102	[7:0]	DUTY_L	This register sets minimum input duty-cycle. 0000 0000: Duty 0% 0111 1111: Duty 49.8%
Maximum input duty cycle setting	0x0103	[7:0]	DUTY_H	This register sets maximum input duty-cycle. 1000 0000: Duty 50.2% 1111 1111: Duty 100%
Lead-angle setting at minimum speed	0x0104	[7:0]	DLDEG_L	This register adjusts lead-angle in rotational speed by TAG_L setting. 000 0000: 0 degree, 111 1111 : -22.225deg (DLDEG_L[7] = 0) 000 0000: 0 degree, 111 1111 : +22.225deg (DLDEG_L[7] = 1)
Lead-angle setting at maximum speed	0x0105	[7:0]	DLDEG_H	This register adjusts lead-angle in rotational speed by TAG_H setting 000 0000: 0 degree, 111 1111 : -22.225deg (DLDEG_H[7] = 0) 000 0000: 0 degree, 111 1111 : +22.225deg (DLDEG_H[7] = 1)
Soft switch width setting at maximum speed	0x0106	[7:4]	SSWHIGH	Soft switch width is set at rotational speed of TAG_H setting. 0000: 2.9% equivalency of a commutation period. 1111: 46.9% equivalency of a commutation period.
Soft switch width setting at minimum speed	0x0106	[3:0]	SSWLOW	Soft switch width is set at rotational speed of TAG_L setting. 0000: 2.9% equivalency of a commutation period. 1111: 46.9% equivalency of a commutation period.
Speed control slope invert	0x0107	[2]	PWMIN_INV	Control slope polarity for input duty-cycle is changed. 0: Normal mode (Low duty-cycle is low speed rotation) 1: Invert mode (Low duty-cycle is high speed rotation)
Sync/Async drive select	0x0107	[1:0]	DRVMODE	This register selects synchronous / asynchronous drive. 00: High-side switching is PWM. Low-side switching is asynchronous 01: High-side switching is PWM. Low-side switching is synchronous 10: High-side switching is asynchronous. Low-side switching is PWM. 11: High-side switching is synchronous. Low-side switching is PWM.



# LV8316H

**Table 20. REGISTER ADDRESS 0x0100–0x0114 Register Description 2**

Function	Address	Bits	Register Name	Description
Sync-drive stop mode (deceleration)	0x0108	[7]	DWNSET	This register selects drive mode when the target speed is less than 80% of the actual motor speed. *When receives control less than 80% of existing speed. 0: Normal (Synchronization drives are always maintained) 1: It is changed to asynchronous drive in speed decrease
Maximum speed setting 2	0x0108	[6]	FULL	This register defines the output behavior when input PWM is greater than the duty cycle set by DUTY_H. 0: Fixed speed set by TAG_H 1: Fixed duty-cycle of 100% with soft switch.
Soft switch mask time select	0x0108	[5]	SS_SW_SEL	This register sets soft switch period in soft start mode. 0: Rise 2.5ms, Fall 5ms 1: Rise 1.25ms, Fall 2.5ms
Soft start release condition	0x0108	[4]	RELLEV	This register selects rotational speed of soft start release condition. 0: When rotational speed arrives at 97% of the target speed. 1: When rotational speed arrives at 500rpm.
Soft start release condition	0x0108	[3]	ENDPWM	This register selects max output duty-cycle of soft start release condition. 0: Max output duty-cycle is 24% 1: Max output duty-cycle is 80%
Soft start release time	0x0108	[2:0]	INCTIM	This register sets the soft start duration time.
Minimum speed setting 2	0x0109	[3:0]	DUTY_S	This register sets the various speed when input duty-cycle is less than DUTY_L.
Dead Time setting	0x010A	[0]	DTIME	This register sets dead time in synchronous rectification drive. 0: 125ns 1: 250ns
Disable period of motor current in CL	0x010B	[3]	CL_SKIP	This register sets disable period of motor current when CLM is active. 0 : Only for corresponding PWM pulse 1 : For corresponding and next PWM pulse
Disable motor synchronous rectification in CL	0x010B	[2]	CL_ASYNC	This register disables motor synchronous rectification when CLM is active. 0 : Synchronous rectification is not disable when CLM is active 1 : Synchronous rectification is disable until detecting Hall signal or motor stop signal when CLM is active. After detecting Hall signal or motor stop, synchronous rectification is enabled.
Condition to enter Lock Protection mode in OCP active	0x010B	[1]	OCP_LAT_CLR	This register sets the condition to enter Lock Protection mode when OCP is happened. 0 : The motor stops until next power on sequence 1 : The IC goes to "Lock Protection mode"
Speed control slope setting	0x010B	[0]	STEPSEL	To prevent drastic changes of a target speed in the closed loop control, this register selects slopes of the target speed change against the input duty cycle change. (The amount is prescribed in the time per 1FG pulse) 0: 1/4 of the existing speed, or +-2047rpm (Small one is chosen) 1: 1/8 of the existing speed, or +-1023rpm (Small one is chosen)
FG/RD select	0x010C	[0]	TACHSEL	This register selects FG pin function. 0: FG output 1: RD output (Rotation is Low, Locked motor is High)
Input PWM average setting	0x010D	[1:0]	PWMAV	The number of times to perform averaging for input PWM duty cycle. 00: Not averaged 01: Averaged 4 times 10: Averaged 8 times 11: Averaged 16 times

# LV8316H

**Table 20. REGISTER ADDRESS 0x0100–0x0114 Register Description 2**

Function	Address	Bits	Register Name	Description
Mask time for reverse recovery time setting	0x010E	[1:0]	OCP_MASK	This register sets the masking time to ignore the reverse recovery for both high-side and low-side Power FET. 00: 0.5us 01: 1.0us 10: 2.0us 11: 4.0us
Lock protection enable	0x0110	[3]	LOCK_FAULT	This register selects enable or disable of the lock protection function. 0: Lock protection enable 1: Lock protection disable
OFF time setting (TOP)	0x0111	[7:4]	MSKDEG_TP	This register sets off period at commutation initiation. It is selected as follows. [7] and [3] 0: In angle                    1: In time [6:4] and [2:0] 000: 0deg            or    0s 001: 0.35deg        or    2.0us 010: 0.70deg        or    4.0us 011: 1.05deg        or    10.0us 100: 2.10deg        or    14.0us 101: 3.50deg        or    20.0us 110: 4.90deg        or    28.0us 111: 7.00deg        or    40.0us
Feedback Gain Adjustment 1	0x0113	[7:4]	IX	Integral gain coarse 0000: 1x 0001: 2x 0010: 4x 0011: 8x 0100: 16x 0101: 32x 0110: 64x 0111: CUT 1000: 1x 1001: 1/2x 1010: 1/4x 1011: 1/8x 1100: 1/16x 1101: 1/32x 1110: 1/64x 1111: CUT
Feedback Gain Adjustment 2	0x0113	[2:0]	IG	Integral gain fine 000: 1x 001: 7/8x 010: 6/8x 011: 5/8x 100: 4/8x 101: 3/8x 110: 2/8x 111: 1/8x

# LV8316H

**Table 20. REGISTER ADDRESS 0x0100–0x0114 Register Description 2**

Function	Address	Bits	Register Name	Description
Feedback Gain Adjustment 3	0x0114	[6:4]	PX	Proportional gain coarse 000: 1x 001: 2x 010: 4x 011: 8x 100: 16x 101: 32x 110: 64x 111: CUT
Feedback Gain Adjustment 4	0x0114	[2:0]	PG	Proportional gain fine 000: 1x 001: 7/8x 010: 6/8x 011: 5/8x 100: 4/8x 101: 3/8x 110: 2/8x 111: 1/8x

**Table 21. REGISTER ADDRESS 0x0219 Register Description**

Function	Address	Bits	Register Name	Description
Communication error status	0x0219	[6:0]	SWI_ERR	Communication error status store to these registers. (Read only)  Refer to a section " <a href="#">COMMUNICATION ERROR</a> " for more information.

# LV8316H

## COMMUNICATION ERROR

The Communication error is reported in the Register (Address 0x0219). Table 22 shows the error report functions.

**Table 22. ERROR REPORT DESCRIPTION**

Address	Bit	DRVMODE	Error Description	State after Error		
				Mode	Communication	Transferred Data
0x0219	D[6]	R/W Field Data Error	Non-zero value is written in the D[5:1] in R/W Field	Wait for the data from the master	Enable	In write mode; Nullified In read mode; No action
	D[5]	Time out Error	The delay between the fields in "Communication mode" is longer than 3 fields	"Standby"	Terminated	---
	D[4]	Checksum Error	Checksum value is wrong in write mode	"Error"	Terminated	Nullified
	D[3]	Data Length Field parity Error	The parity in "Data Length Field" is wrong	"Error"	Terminated	Nullified
	D[2]	R/W Field parity Error	The parity in "R/W Field" is wrong	"Error"	Terminated	Nullified
	D[1]	Header Error	Header input is not correct	"Error"	Terminated	Nullified
	D[0]	Framing Error	The signal pin is "Low" state in Stop bits	"Error"	Terminated	Nullified

When "Time out error" posts "1" in D[5] of register 0x0219, the LV8316H goes into standby mode.

If the data length is long and the "Time out Error" is happened during the Register write, the data with the correct "Checksum" transferred before the "Time out Error" is stored in register, then the LV8316H goes to "Standby mode".

When "Checksum error" posts "1" in D[4] of Register 0x0219 while in the Write mode, the LV8316H goes into Error mode and the communication is terminated. In this case, the transferred data is discarded but the data with correct "Checksum" transferred before the "Checksum error" is stored in the register.

Other errors, except for "R/W Field Data Error" also write "1" in the specified register and the LV8316H goes to "Error

mode" as well. To recover from "Error mode", the communication pin should be kept "High" for longer than the time corresponding to 4 "Fields", then the LV8316H goes to "Standby mode" automatically despite of the status of error register.

Each error register keeps the error bit until the master reads the error register.

Reading Reg.0x0219 as 1byte will clear the error bits. Multiple read will not clear the error bits.

It is recommended to read the error register after every transaction to confirm that the communication is completed successfully.

Figure 34 shows the state diagram. Refer to the Application note [AND9761/D](#) as well for more information regarding the communication.

# LV8316H

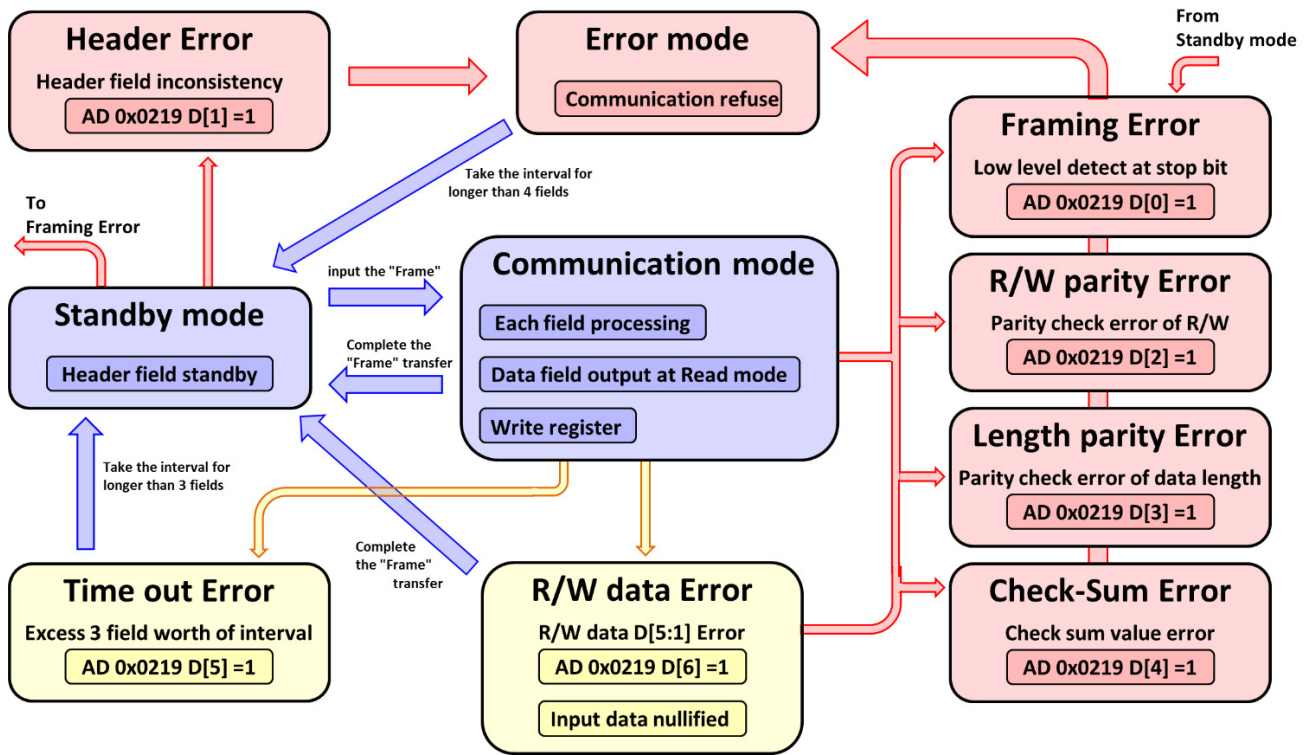
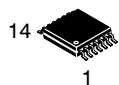


Figure 34. State Transition Diagram of Each Error

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

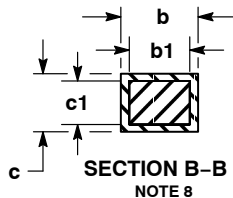
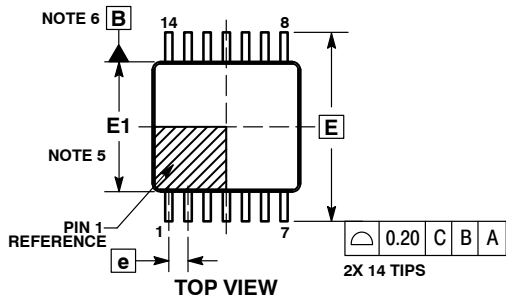
ON Semiconductor®



SCALE 1:1

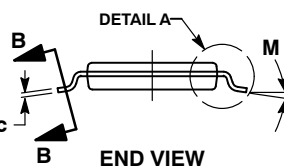
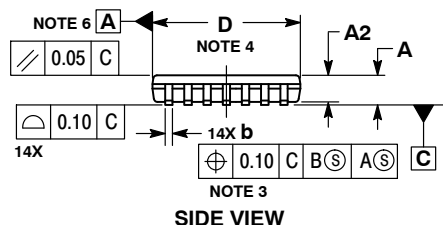
## TSSOP-14 EP CASE 948AW ISSUE C

DATE 09 OCT 2012

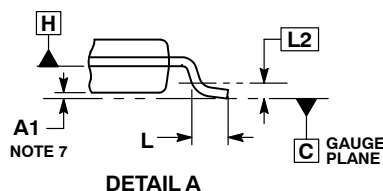
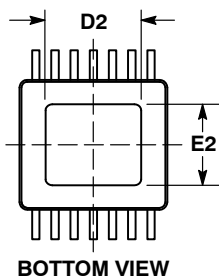


NOTES:

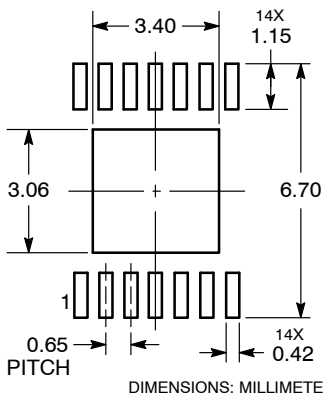
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.07 mm MAX. AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADII OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION D IS DETERMINED AT DATUM H.
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM H.
- DATUMS A AND B ARE DETERMINED AT DATUM H.
- A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
- SECTION B-B TO BE DETERMINED AT 0.10 TO 0.25 mm FROM THE LEAD TIP.



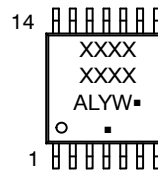
MILLIMETERS		
DIM	MIN	MAX
A	---	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	4.90	5.10
D2	3.09	3.62
E	6.40 BSC	
E1	4.30	4.50
E2	2.69	3.22
e	0.65 BSC	
L	0.45	0.75
L2	0.25 BSC	
M	0°	8°



### RECOMMENDED SOLDERING FOOTPRINT\*



### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON66474E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP-14 EP, 5.0X4.4	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative

## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [Motor/Motion/Ignition Controllers & Drivers](#) category:*

*Click to view products by [ON Semiconductor](#) manufacturer:*

Other Similar products are found below :

[FSB50550TB2](#) [FSBF15CH60BTH](#) [MSVCPM2-63-12](#) [MSVGW45-14-2](#) [MSVGW54-14-3](#) [MSVGW54-14-5](#) [NTE7043](#) [LA6565VR-TLM-E](#)  
[LB11650-E](#) [LB1837M-TLM-E](#) [LB1845DAZ-XE](#) [LC898300XA-MH](#) [SS30-TE-L-E](#) [26700](#) [LV8281VR-TLM-H](#) [BA5839FP-E2](#) [IRAM236-1067A](#) [LA6584JA-AH](#) [LB11847L-E](#) [NCV70501DW002R2G](#) [AH293-PL-B](#) [STK672-630CN-E](#) [TND315S-TL-2H](#) [FNA23060](#) [FSB50250AB](#)  
[FNA41060](#) [MSVB54](#) [MSVBTC50E](#) [MSVCPM3-54-12](#) [MSVCPM3-63-12](#) [MSVCPM4-63-12](#) [MSVTA120](#) [FSB50550AB](#)  
[NCV70501DW002G](#) [LC898301XA-MH](#) [LV8413GP-TE-L-E](#) [MSVGW45-14-3](#) [MSVGW45-14-4](#) [MSVGW45-14-5](#) [MSVGW54-14-4](#)  
[STK984-091A-E](#) [MP6519GQ-Z](#) [LB11651-E](#) [IRSM515-025DA4](#) [LV8127T-TLM-H](#) [MC33812EKR2](#) [NCP81382MNTXG](#) [TDA21801](#)  
[LB11851FA-BH](#) [NCV70627DQ001R2G](#)