Ordering number : ENA2039C

LV8549MC

Monolithic Linear IC

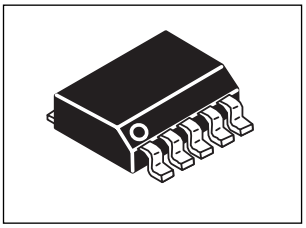
12V Low Saturation Voltage Drive Stepper Motor Driver

ON Semiconductor®

http://onsemi.com

Overview

The LV8549MC is a low saturation voltage stepper motor driver IC.
It is optimal for Full step motor drive in 12V system products.



SOIC10

Function

- DMOS output transistor adoption (Upper and lower total RON=1Ω typ)
- The compact package (SOIC10) is adopted
- V_{CC} max=20v, I_O max=1A
- For one power supply (The control system power supply is unnecessary.)
- Current consumption 0 when standing by

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	V_{CC} max	VCC	-0.3 to +20	V
Output impression voltage	VOUT	OUT1 , OUT2 , OUT3 , OUT4	-0.3 to +20	V
Input impression voltage	V_{IN}	ENA , IN1 , IN2	-0.3 to +6	V
GND pin outflow current	IGND	Per ch	1.0	A
Allowable Power dissipation	Pd max	*	1.0	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-40 to +150	°C

*: When mounted on the specified printed circuit board (57.0mm ×57.0mm × 1.6mm), glass epoxy, both sides

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommendation Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{CC}	VCC	4.0 to 16	V
Input “H” level voltage	$V_{IN}H$	ENA , IN1 , IN2	+1.8 to +5.5	V
Input “L” level voltage	$V_{IN}L$		-0.3 to +0.7	V

ORDERING INFORMATION

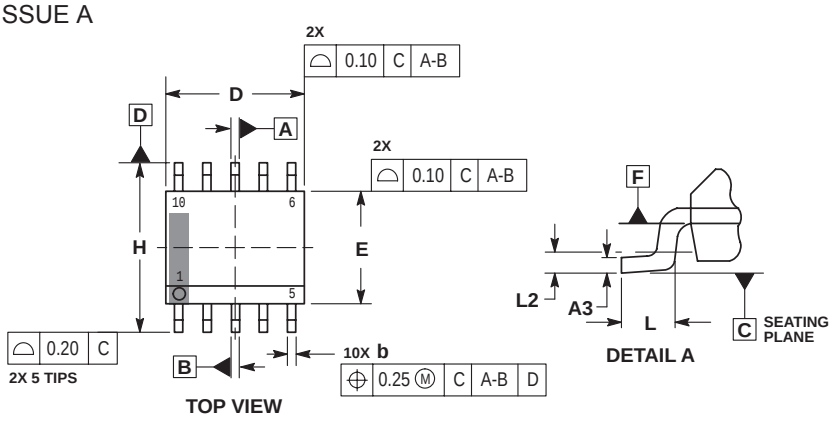
See detailed ordering and shipping information on page 10 of this data sheet.

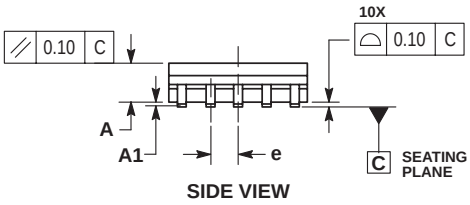
Electrical Characteristics at Ta = 25°C, V_{CC} = 12V

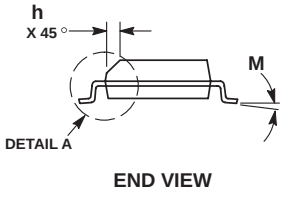
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply voltage	$I_{CC}0$	Standby mode ENA=L			1	μA
	$I_{CC}1$	ENA=H , no-load		1.7	2.3	mA
Input current	I_{IN}	V_{IN}=5V	30	50	65	μA
Thermal shutdown operating temperature	Ttsd	Design certification	150	180	210	°C
Temperature hysteresis width	ΔTtsd	Design certification		40		°C
Low voltage protection function operation voltage	VthV_{CC}		3.3	3.5	3.65	V
Release voltage	Vthret		3.55	3.8	3.95	V
Output ON resistance (Upper and lower total)	R_{ON}	I_{OUT}=1.0A	0.7	1	1.25	Ω
Output leak current	$I_O$leak	V_O=16V			10	μA
Diode forward voltage	VD	ID=1.0A		1.0	1.2	V

Package Dimensions

SOIC-10NB
CASE 751BQ-01
ISSUE A



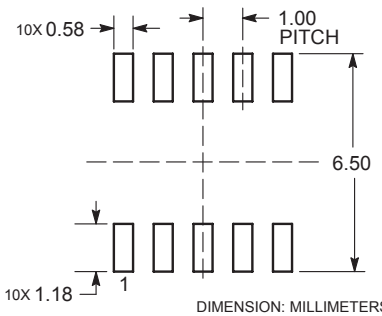




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.75
A1	0.10	0.25
A3	0.17	0.25
b	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.00 BSC	
H	5.80	6.20
h	0.37 REF	
L	0.40	1.27
L2	0.25 BSC	
M	0°	8°

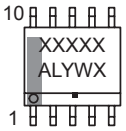
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

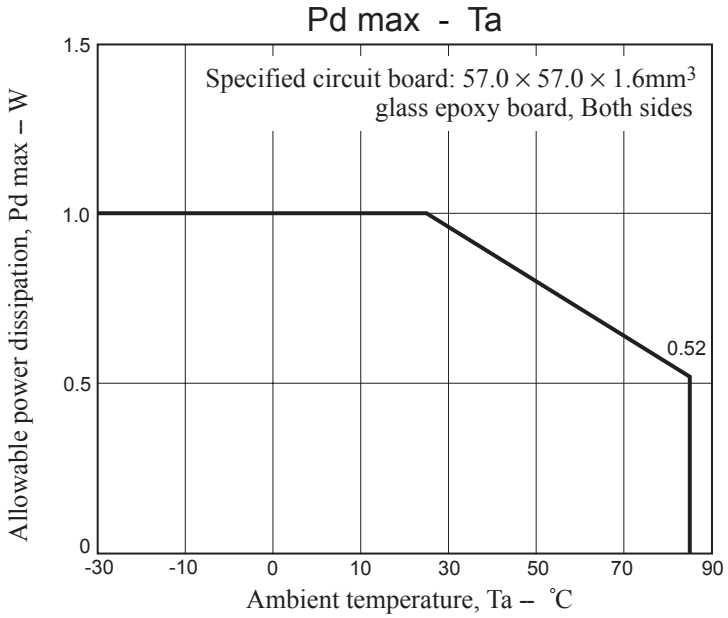
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

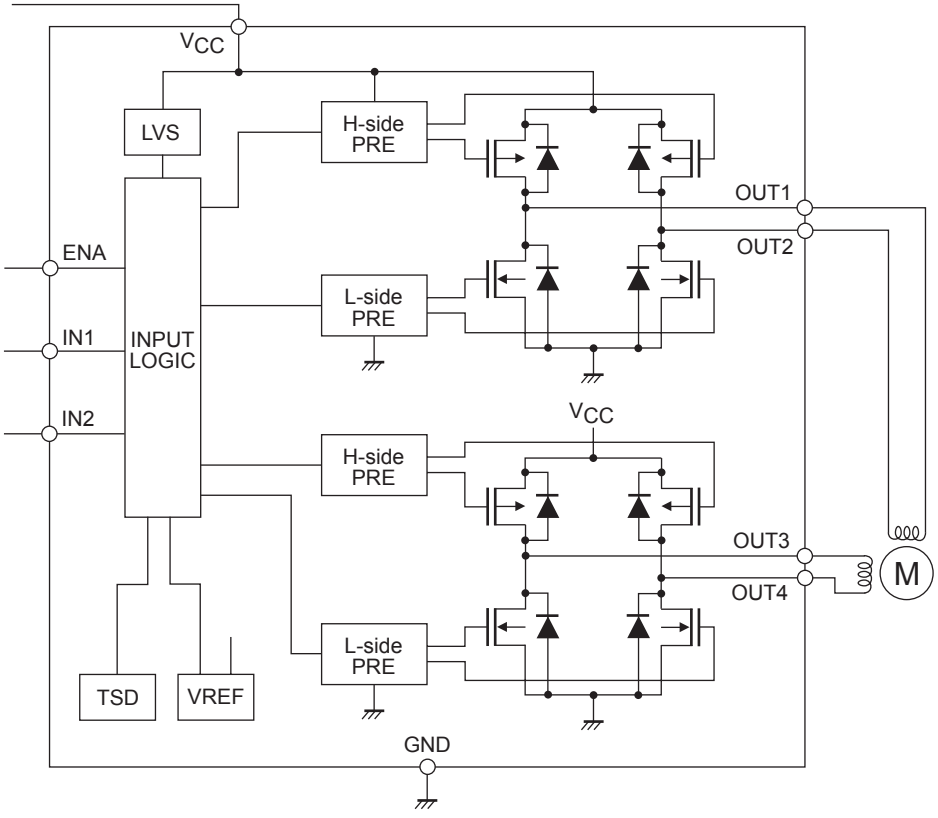


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

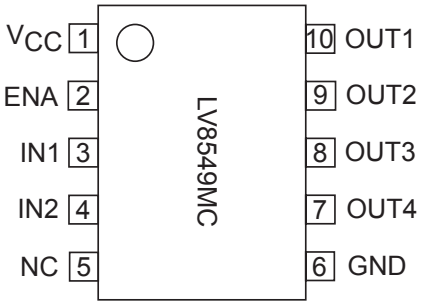
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G", may or not be present.



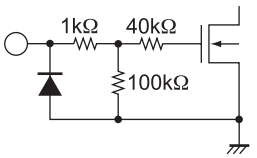
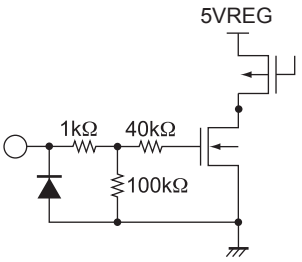
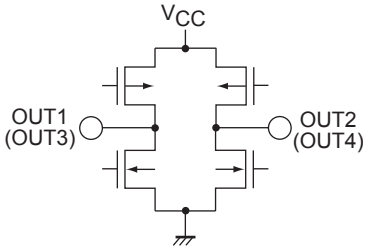
Block Diagram



Pin Assignment



Pin function

Pin No.	Pin name	Pin function	Equivalent Circuit
1	V_{CC}	Power-supply voltage pin. V_{CC} voltage is impressed. The permissible operation voltage is from 4.0 to 16.0(V). The capacitor is connected for stabilization for GND pin (6pin).	
2	ENA	Motor drive control input pin. ENA pin becomes the stand-by mode in "L" and can 0 circuitry current. When ENA pin are "H", from the stand-by mode, the output state becomes an output corresponding to the input logic. It is a digital input, and the range of "L" level input is 0 to 0.7(V). The range of "H" level input is 1.8 to 5.5(V). With built-in pull-down resistance 100(kΩ).	
3	IN1	Motor drive control input pin. Driving control input pin of OUT1 (10pin) and OUT2 (9pin). With built-in pull-down resistance.	
4	IN2	Motor drive control input pin. Driving control input pin of OUT3 (8pin) and OUT4 (7pin). With built-in pull-down resistance.	
5	NC		
6	GND	Ground pin.	
7	OUT4	Driving output pin. The motor coil is connected between terminal OUT3 (8pin).	
8	OUT3	Driving output pin. The motor coil is connected between terminal OUT4 (7pin).	
9	OUT2	Driving output pin. The motor coil is connected between terminal OUT1 (10pin).	
10	OUT1	Driving output pin. The motor coil is connected between terminal OUT2 (9pin).	

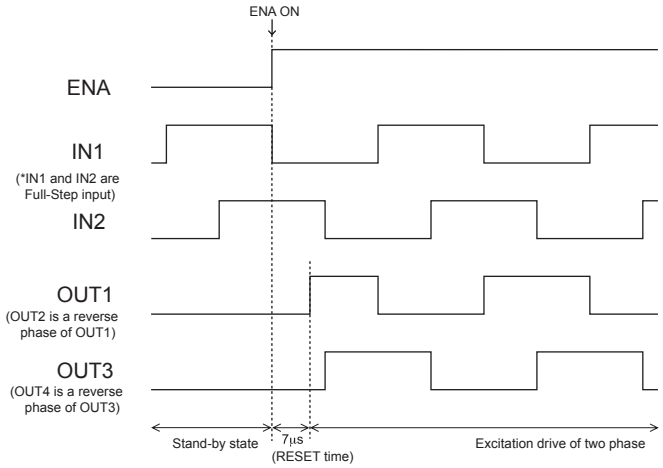
Operation explanation

1. STM output control logic

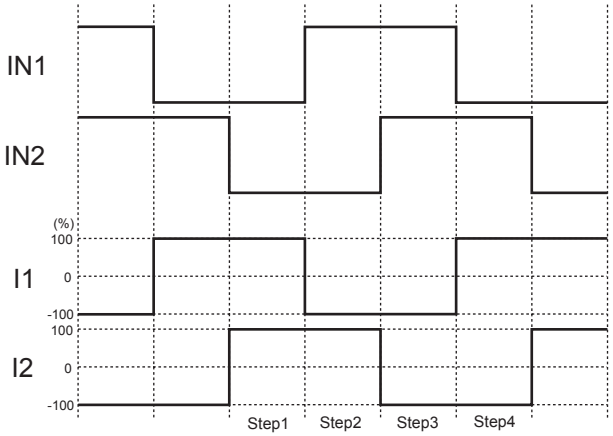
Input			Output				State
ENA	IN1	IN2	OUT1	OUT2	OUT3	OUT4	
L	-	-	OFF	OFF	OFF	OFF	Stand-by
H	L	L	H	L	H	L	Step 1
	H	L	L	H	H	L	Step2
	H	H	L	H	L	H	Step3
	L	H	H	L	L	H	Step4

2. About the switch time from the stand-by state to the state of operation

This IC has completely stopped operating when ENA pin is "L". After the reset time of about 7μs internal settings it shifts to a prescribed output status corresponding to the state of the input when ENA pin is "H".
During reset time, all output TR OFF is maintained.



3. Example of current waveform at full-step mode.

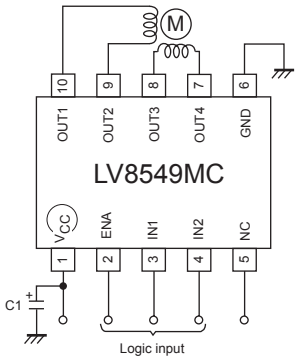


4. Thermal shutdown function

The thermal shutdown circuit is incorporated and the output is turned off when junction temperature Tj exceeds 180°C . As the temperature falls by hysteresis, the output turned on again (automatic restoration).
The thermal shutdown circuit does not guarantee the protection of the final product because it operates when the temperature exceed the junction temperature of Tjmax=150°C.

TSD = 180°C (typ)
ΔTSD = 40°C (typ)

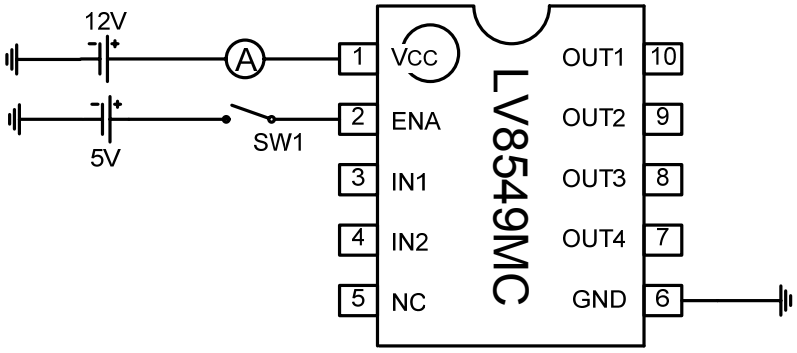
Applied circuit example



* Bypass capacitor (C1) connected between V_{CC}-GND of all examples of applied circuit recommends the electric field capacitor of 0.1μF to 10μF.
Confirm there is no problem in operation in the state of the motor load including the temperature property about the value of the capacitor.
Mount the position where the capacitor is mounted on nearest IC.

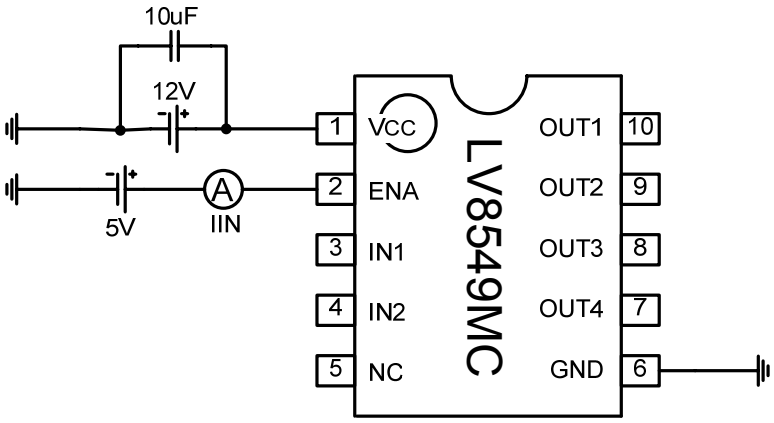
Measurement connection diagram

(1) Current consumption when standing by $I_{CC}0$
Current consumption $I_{CC}1$



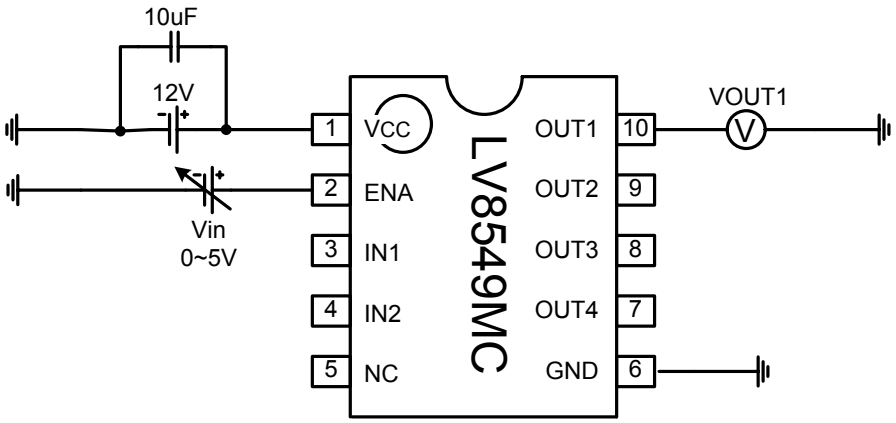
Measure $I_{CC}0$ with all SW OFF. Measure $I_{CC}1$ with any of the SW1 ON.

(2) Input current I_{IN}



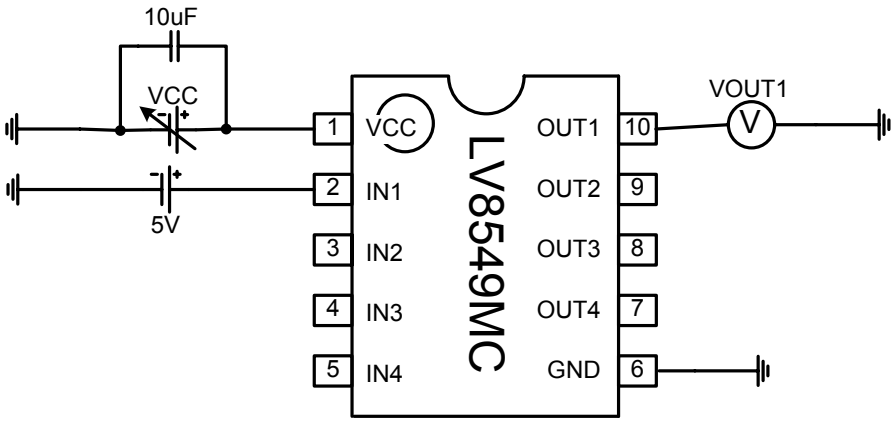
This is about the measurement of ENA pin. Measure the other IN1 and IN2 pins as is this case.

(3) Input "H" level voltage VINH



Measure the Vin value at the time VOUT1 changes to "H" while varying Vin 0 to 5V.
This is about the measurement of ENA pin. Measure the other IN1 and IN2 pins as is this case.
When I measure IN1 and IN2 pins, ENA pin, please perform it in a state of "H".

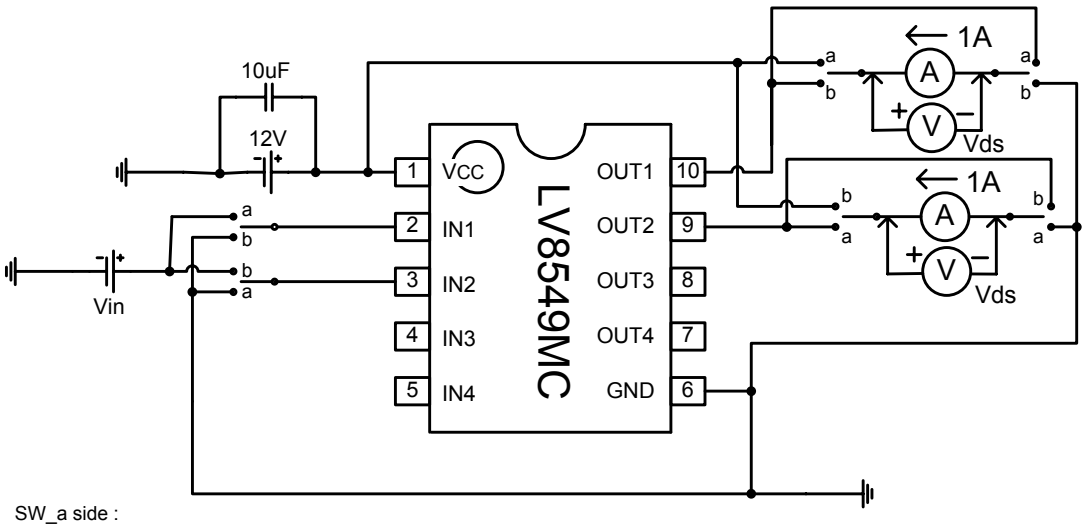
(4) Low voltage protection function operation voltage VthV$_{CC}$ / Release voltage Vthret



Low voltage protection function
Operation voltage : VCC=12V to 0V
Release voltage : VCC=0V to 12V

To measure the operating voltage of the reduced voltage protection, measure the VCC value at the time VOUT1 becomes "L" while varying VCC from 12V to 0V.
To measure the release voltage of the reduced voltage protection, measure the VCC value at the time VOUT1 becomes "H" while varying VCC from 0V to 12V.

(5) Output ON resistance Ron

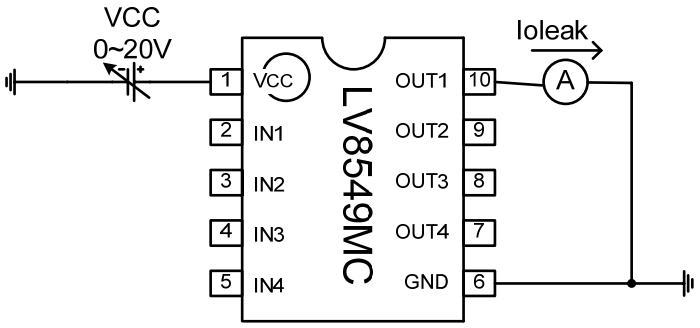


SW_a side :
OUT1 Upper-side/OUT2 Lower-side
OUT3 Upper-side/OUT4 Lower-side
SW_b side :
OUT1 Lower-side/OUT2 Upper-side
OUT3 Lower-side/OUT4 Upper-side

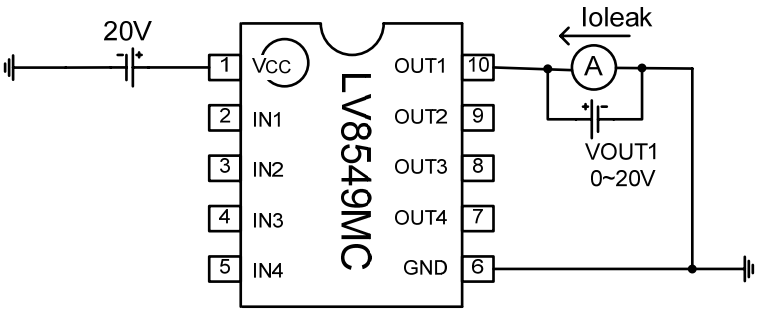
Measure OUT1 upper side and OUT2 lower side FET with the SW set to "a".
Measure OUT1 lower side and OUT2 upper side FET with the SW set to "b".
Measure OUT3 and OUT4 as are the cases of OUT1 and OUT2.

(6) Output leak current Ioleak

<Each OUT Upper-side>

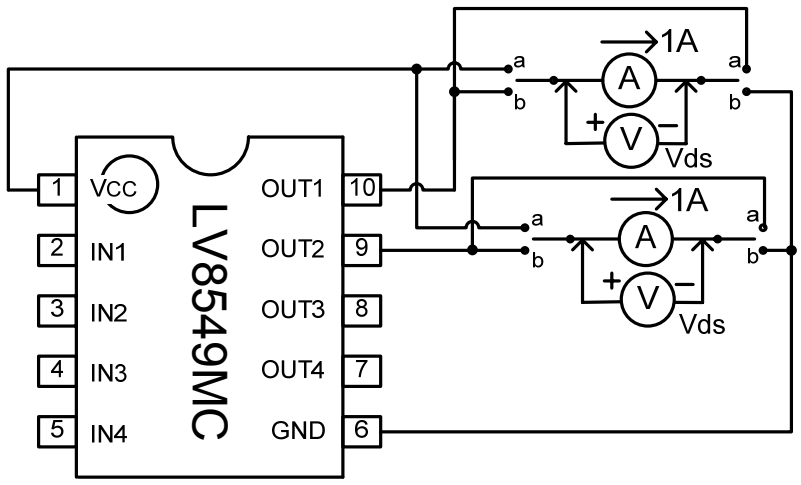


<Each OUT Lower-side>



To measure the upper FET output leak current, set the OUT to 0V and measure the OUT current while varying VCC from 0 to 20V.
To measure the lower FET output leak current, set the VCC to 20V and measure the OUT current while varying OUT from 0 to 20V.
This is about the measurement of OUT1 pin. Measure the other OUT2-4 pins as is this case.

(7) Diode forward voltage VD



SW_a side : Each OUT Upper-side
SW_b side : Each OUT Lower-side

Measure OUT1 and OUT2 upper FET with the SW set to "a".
Measure OUT1 and OUT2 lower FET with the SW set to "b".
Measure OUT3 and OUT4 as are the cases/connections of OUT1 and OUT2.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV8549MC-AH	SOIC10 (Pb-Free / Halogen Free)	2500 / Tape & Reel
LV8549MC-BH	SOIC10 (Pb-Free / Halogen Free)	2500 / Tape & Reel

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