LV8740V

ON Semiconductor®

http://onsemi.com

Monolithic Linear IC

PWM Current Control Stepper Motor Driver

Overview

The LV8740V is a 2-channel H-bridge driver IC that can switch a stepper motor driver, which is capable of micro-step drive and supports Quarter-step excitation, and two channels of a brushed DC motor driver, which supports forward, reverse, brake, and standby of a motor. It is ideally suited for driving brushed DC motors and stepper motors used in office equipment and amusement applications.

Function

- Single-channel PWM current control stepper motor driver (selectable with DC motor driver channel 2) incorporated.
- On resistance (upper side : 0.3Ω ; lower side : 0.2Ω ; total of upper and lower : 0.5Ω ; Ta = 25°C, I_O = 2.5A)
- Excitation mode can be set to Full-step, Half-step full torque, Half-step , or Quarter-step
- Excitation step proceeds only by step signal input
- Motor current selectable in four steps
- BiCDMOS process IC
- Output short-circuit protection circuit (selectable from latch-type or auto reset-type) incorporated
- Unusual condition warning output pins
- No control supply required

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_M max	VM , VM1 , VM2	38	V
Output peak current	I_O peak	tw ≤ 10ms, duty 20%, Each 1ch	3.0	A
Output current	I_O max	Each 1ch	2.5	A
Logic input voltage	V_{IN}	ST , OE , DM , MD1/DC11 , MD2/DC12 , FR/DC21 , STP/DC22 , RST , EMM , ATT1 , ATT2	-0.3 to +6.0	V
MONI/EMO input voltage	V_{MONI}/V_{EMO}		-0.3 to +6.0	V
Allowable power dissipation	Pd max	*	3.45	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified circuit board : 90×90×1.6mm³ : 2-Layer glass epoxy printed circuit board with back mounting.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ORDERING INFORMATION

See detailed ordering and shipping information on page 25 of this data sheet.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_M	VM , VM1 , VM2	9 to 35	V
Logic input voltage	V_{IN}	ST , OE , DM , MD1/DC11 , MD2/DC12 , FR/DC21 , STP/DC22 , RST , EMM , ATT1 , ATT2	0 to 5.5	V
VREF input voltage range	VREF		0 to 3.0	V

Electrical Characteristics at Ta = 25°C, V_M = 24V, VREF = 1.5V

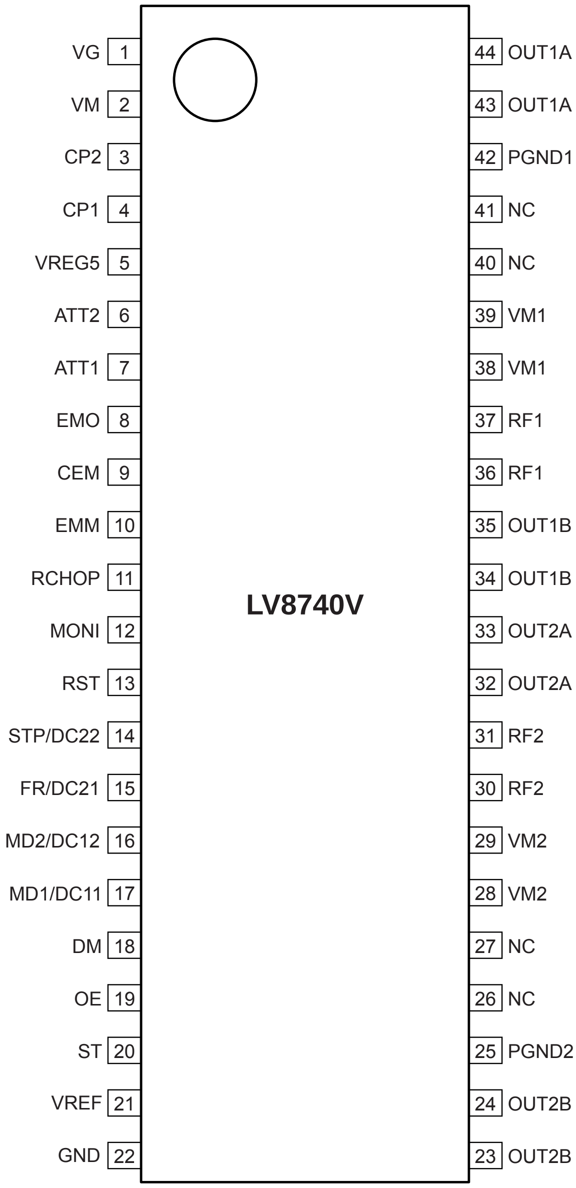
Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Standby mode current drain		IMstn	ST = "L" , I(VM)+I(VM1)+I(VM2)		180	250	μA
Current drain		IM	ST = "H", OE = "L", no load I(VM)+I(VM1)+I(VM2)		3	5	mA
VREG5 output voltage		Vreg5	I_O=-1mA	4.7	5.0	5.3	V
Thermal shutdown temperature		TSD	Design guarantee	150	180	210	°C
Thermal hysteresis width		ΔTSD	Design guarantee		40		°C
Motor Driver							
Output on-resistance		Ronu	I_O = 2.5A, Upper-side on resistance		0.3	0.4	Ω
		Rond	I_O = 2.5A, Lower-side on resistance		0.2	0.25	Ω
Output leakage current		$I_O$leak	VM=35V			50	μA
Diode forward voltage		VD	ID = -2.5A		1.1	1.3	V
ST pin input current		I_{ST}L	V_{IN} = 0.8V	3	8	15	μA
		I_{ST}H	V_{IN} = 5V	48	80	112	μA
Logic pin input current (other ST pin)		I_{IN}L	OE , DM , MD1/DC11 , MD2/DC12 , FR/DC21 , STP/DC22 , RST , EMM , ATT1 , ATT2 , V_{IN} = 0.8V	3	8	15	μA
		I_{IN}H	V_{IN} = 5V	30	50	70	μA
Logic input voltage	High	V_{IN}h	ST , OE , DM , MD1/DC11 , MD2/DC12 , FR/DC21 , STP/DC22 , RST , EMM , ATT1 , ATT2	2.0		5.5	V
	Low	V_{IN}l		0		0.8	V
Current setting comparator threshold voltage (Current step switch)	Quarter step resolution	Vtdac0_W	Step 0(When initialized : channel 1 comparator level)	0.290	0.300	0.310	V
		Vtdac1_W	Step 1 (Initial state+1)	0.260	0.270	0.280	V
		Vtdac2_W	Step 2 (Initial state+2)	0.200	0.210	0.220	V
		Vtdac3_W	Step 3 (Initial state+3)	0.095	0.105	0.115	V
	Half step resolution	Vtdac0_H	Step 0 (When initialized: channel 1 comparator level)	0.290	0.300	0.310	V
		Vtdac2_H	Step 2 (Initial state+1)	0.200	0.210	0.220	V
	Half step resolution (full torque)	Vtdac0_HF	Step 0 (Initial state, channel 1 comparator level)	0.290	0.300	0.310	V
		Vtdac2_HF	Step 2 (Initial state+1)	0.290	0.300	0.310	V
	Full step resolution	Vtdac2_F	Step 2	0.290	0.300	0.310	V
Current setting comparator threshold voltage (Current attenuation rate switch)		Vtatt00	ATT1=L, ATT2=L	0.290	0.300	0.310	V
		Vtatt01	ATT1=H, ATT2=L	0.190	0.200	0.210	V
		Vtatt10	ATT1=L, ATT2=H	0.140	0.150	0.160	V
		Vtatt11	ATT1=H, ATT2=H	0.090	0.100	0.110	V
Chopping frequency		Fchop	RCHOP = 20kΩ	45	62.5	75	kHz
VREF pin input current		Iref	VREF = 1.5V	-0.5			μA
MONI pin saturation voltage		Vsatmon	I_{MONI}=1mA		50	100	mV
Charge pump							
VG output voltage		VG		28	28.7	29.8	V
Rise time		tONG	VG = 0.1μF , Between CP1-CP2 0.1uF ST="H" → VG=VM+4V			0.5	ms
Oscillator frequency		Fosc	RCHOP = 20kΩ	90	125	150	kHz

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output short-circuit protection						
EMO pin saturation voltage	Vsatemo	Iemo = 1mA		50	100	mV
CEM pin charge current	Icem	Vcem=0V	7	10	13	μA
CEM pin threshold voltage	Vtcem		0.8	1.0	1.2	V

Pin Assignment

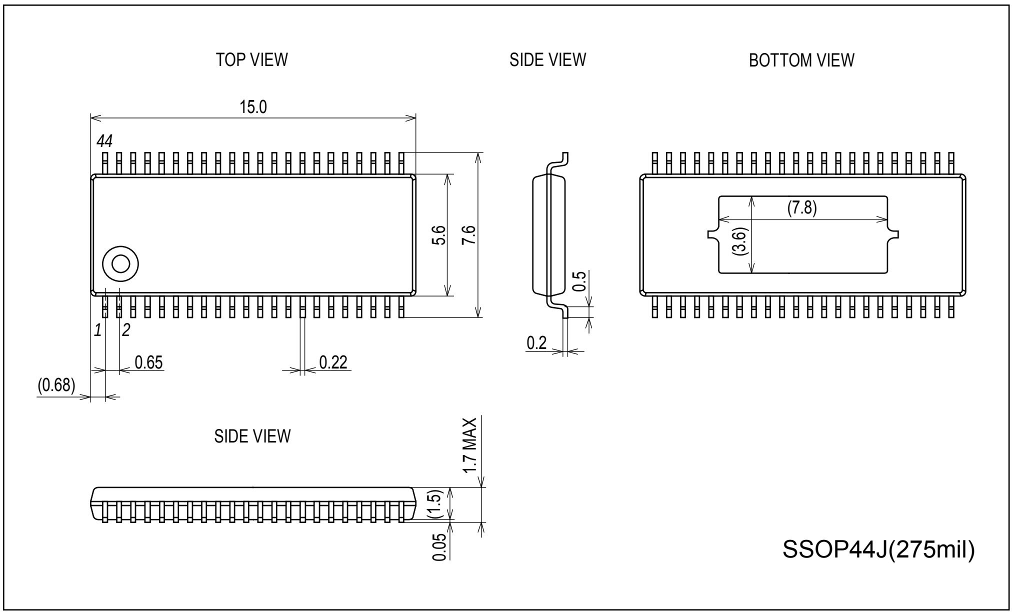


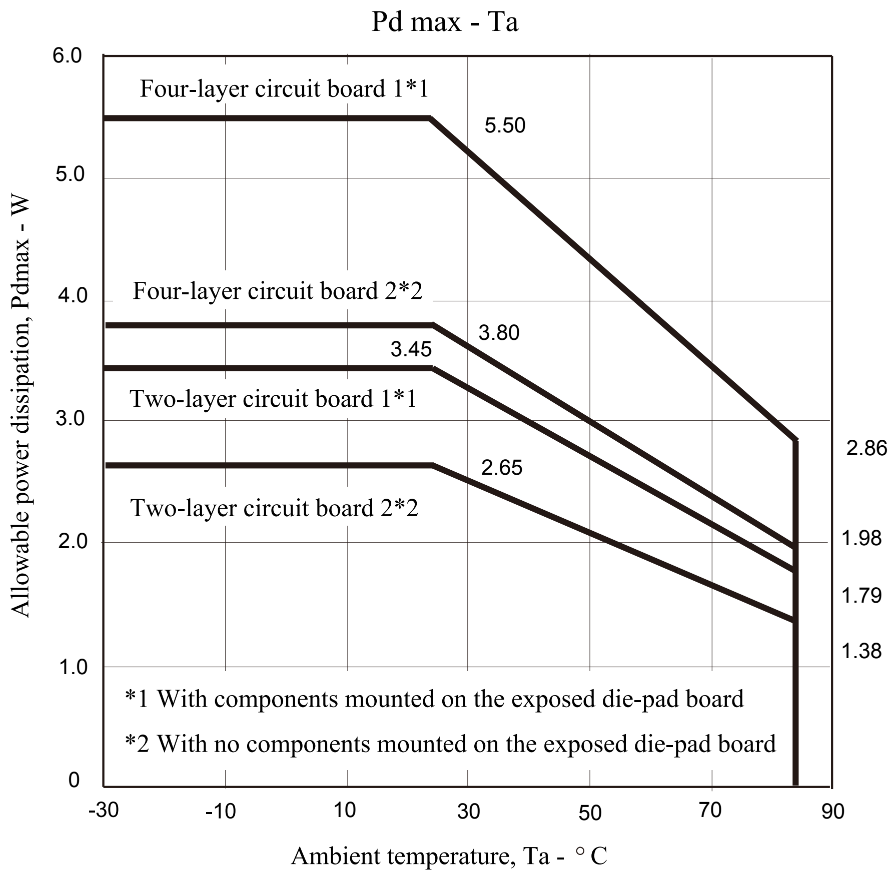
Top view

Package Dimensions

unit : mm (typ)

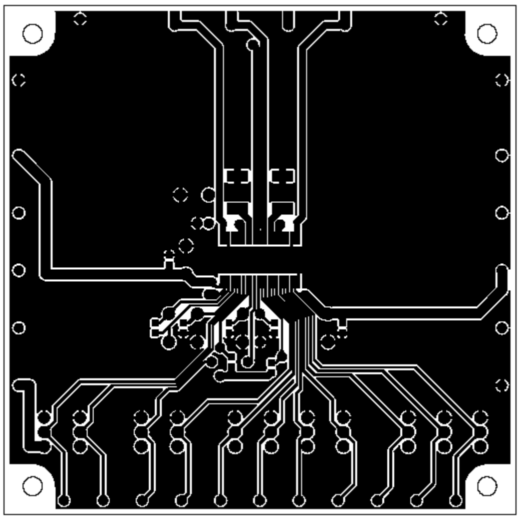
3285B



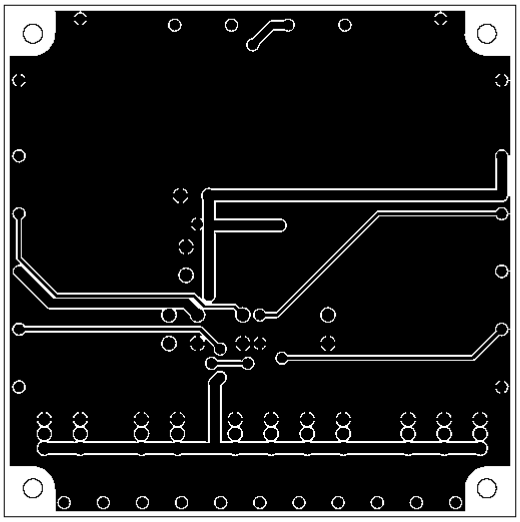


Substrate Specifications (Substrate recommended for operation of LV8740V)

Size : 90mm × 90mm × 1.6mm
Material : Glass epoxy
Copper wiring density : L1 = 85% / L2 = 90%



L1 : Copper wiring pattern diagram



L2 : Copper wiring pattern diagram

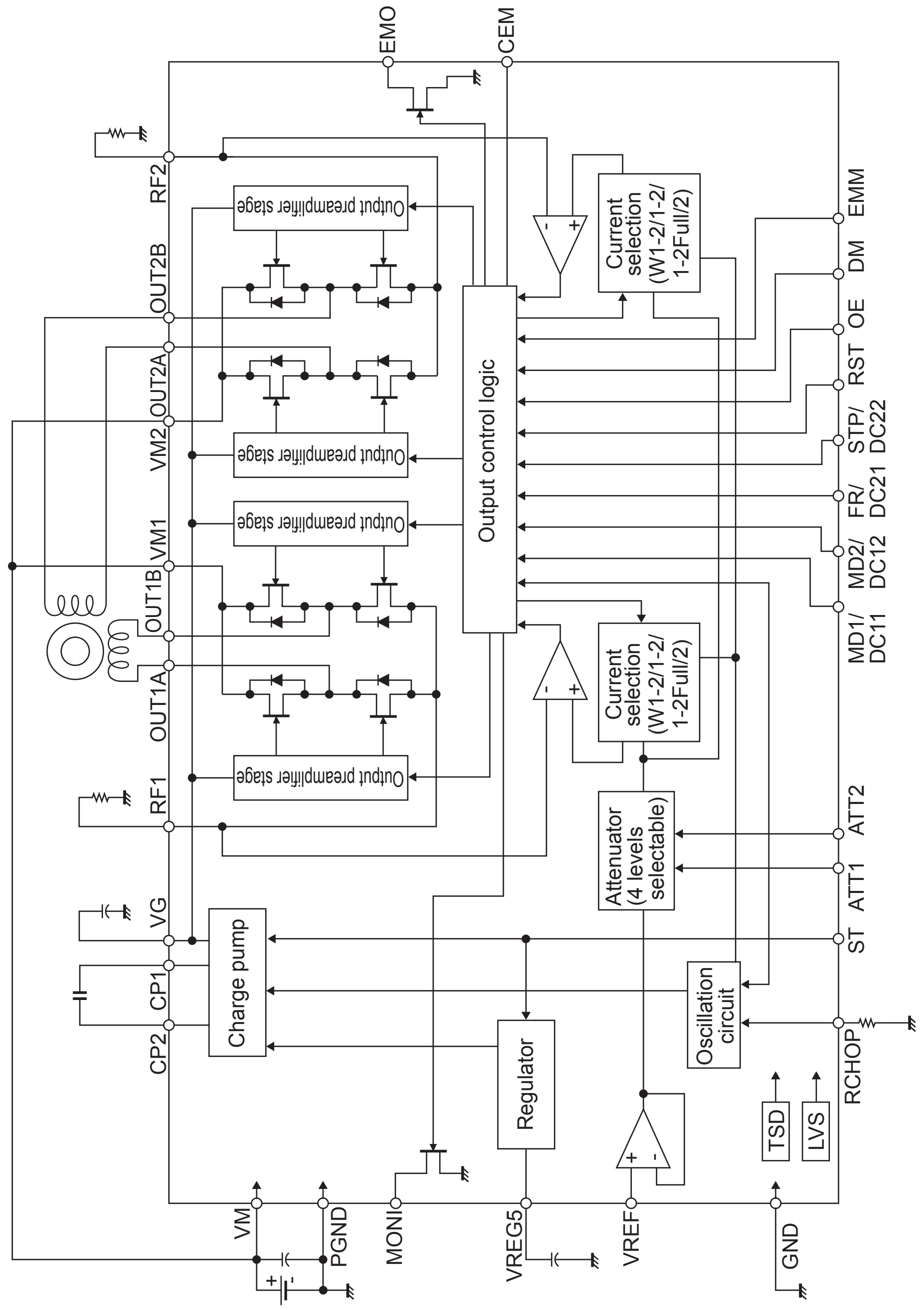
Cautions

1) The data for the case with the Exposed Die-Pad substrate mounted shows the values when 90% or more of the Exposed Die-Pad is wet.

2) For the set design, employ the derating design with sufficient margin.
Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stresses such as vibration, impact, and tension.
Accordingly, the design must ensure these stresses to be as low or small as possible.
The guideline for ordinary derating is shown below :
(1)Maximum value 80% or less for the voltage rating
(2)Maximum value 80% or less for the current rating
(3)Maximum value 80% or less for the temperature rating

3) After the set design, be sure to verify the design with the actual product.
Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc.
Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal conduction, possibly resulting in thermal destruction of IC.

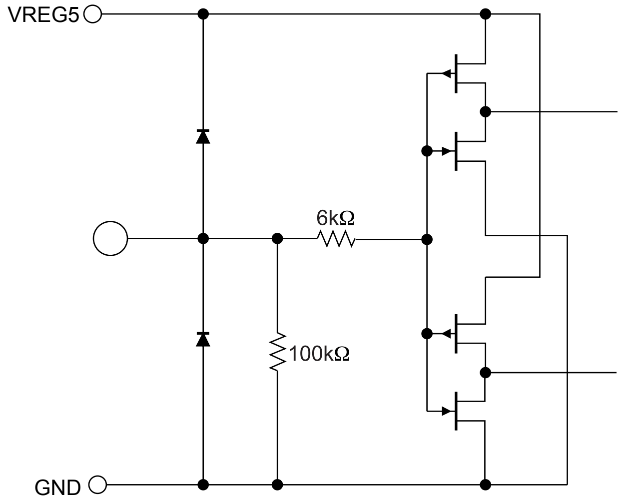
Block Diagram

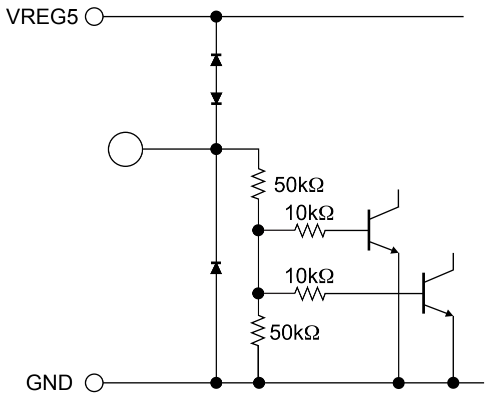


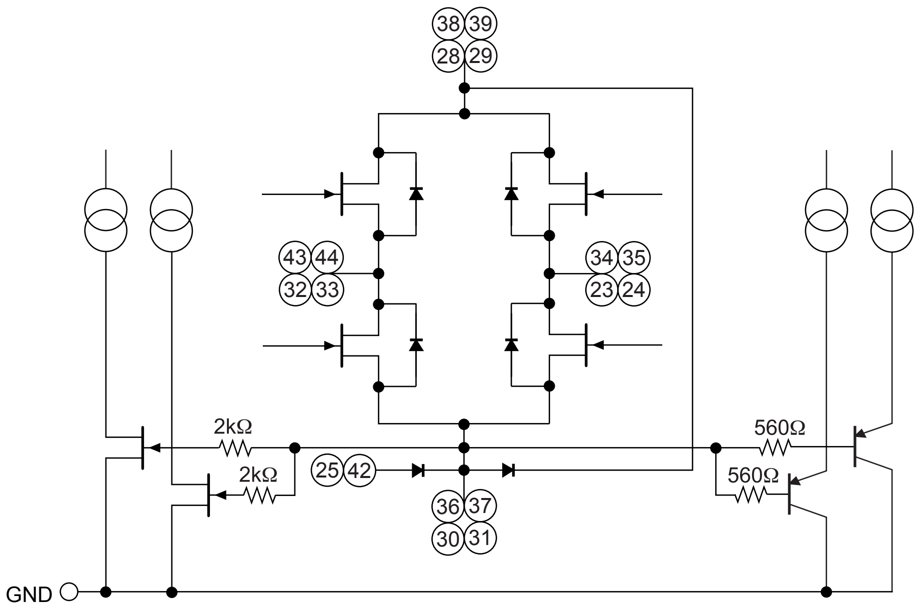
Pin Functions

Pin No.	Pin name	Description
1	VG	Charge pump capacitor connection pin
2	VM	Motor power supply connection pin
3	CP2	Charge pump capacitor connection pin
4	CP1	Charge pump capacitor connection pin
5	VREG5	Internal power supply capacitor connection pin
6	ATT2	Motor holding current switching pin
7	ATT1	Motor holding current switching pin
8	EMO	Output short-circuit state warning output pin
9	CEM	Pin to connect the output short-circuit state detection time setting capacitor
10	EMM	Over current mode switching pin
11	RCHOP	Chopping frequency setting resistor connection pin
12	MONI	Position detection monitor pin
13	RST	Reset signal input pin
14	STP/DC22	STM STEP signal input pin/DCM2 output control input pin
15	FR/DC21	STM forward/reverse rotation signal input pin/DCM2 output control input pin
16	MD2/DC12	STM excitation mode switching pin/DCM1 output control input pin
17	MD1/DC11	STM excitation mode switching pin/DCM1 output control input pin
18	DM	Drive mode (STM/DCM) switching pin
19	OE	Output enable signal input pin
20	ST	Chip enable pin
21	VREF	Constant current control reference voltage input pin
22	GND	Signal system ground
23, 24	OUT2B	Channel 2 OUTB output pin
25	PGND2	Channel 2 Power system ground
28, 29	VM2	Channel 2 motor power supply connection pin
30, 31	RF2	Channel 2 current-sense resistor connection pin
32, 33	OUT2A	Channel 2 OUTA output pin
34, 35	OUT1B	Channel 1 OUTB output pin
36, 37	RF1	Channel 1 current-sense resistor connection pin
38, 39	VM1	Channel 1 motor power supply pin
42	PGND1	Channel 1 Power system ground
43, 44	OUT1A	Channel 1 OUTA output pin
26, 27 40, 41	NC	No Connection (No internal connection to the IC)

Equivalent Circuits

<table>
<tr><th>Pin No.</th><th>Pin</th><th>Equivalent Circuit</th></tr>
<tr><td>6
7
10
13
14
15
16
17
18
19</td><td>ATT2
ATT1
EMM
RST
STP/DC22
FR/DC21
MD2/DC12
MD1/DC11
DM
OE</td><td>


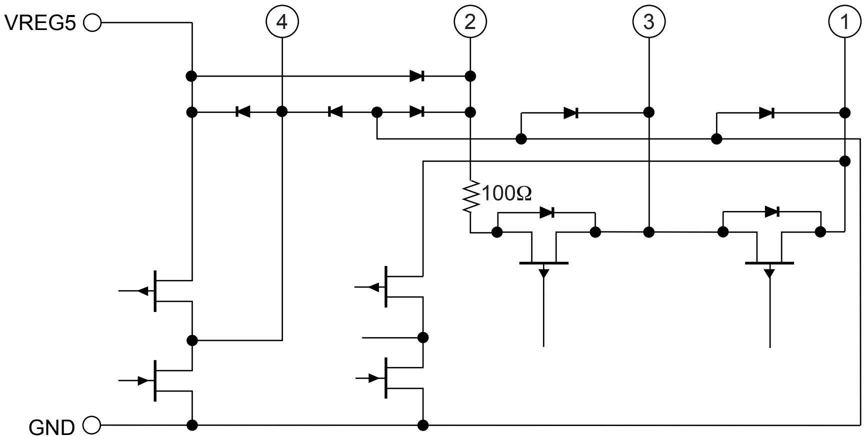
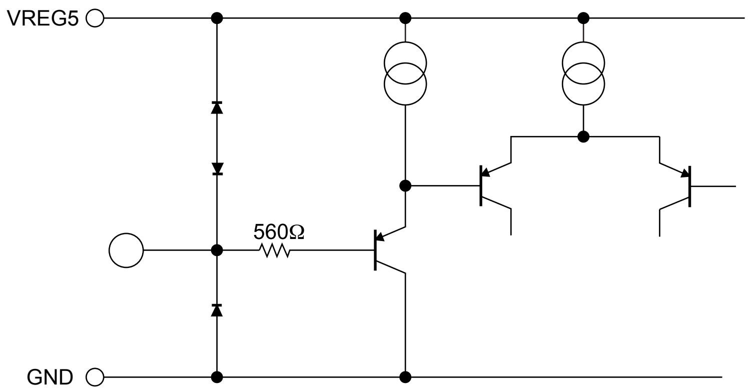
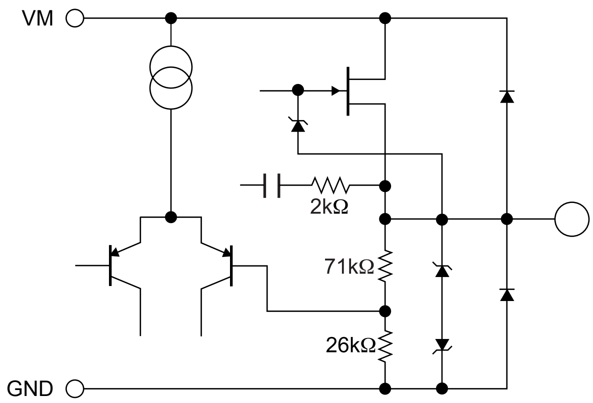
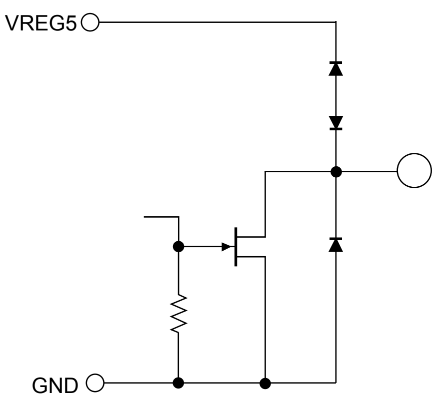
</td></tr>
<tr><td>20</td><td>ST</td><td>


</td></tr>
<tr><td>23, 24
25
28, 29
30, 31
32, 33
34, 35
36, 37
38, 39
42
43, 44</td><td>OUT2B
PGND2
VM2
RF2
OUT2A
OUT1B
RF1
VM1
PGND1
OUT1A</td><td>


</td></tr>
</table>

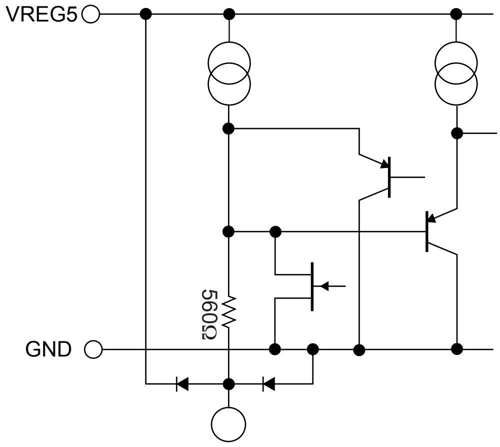
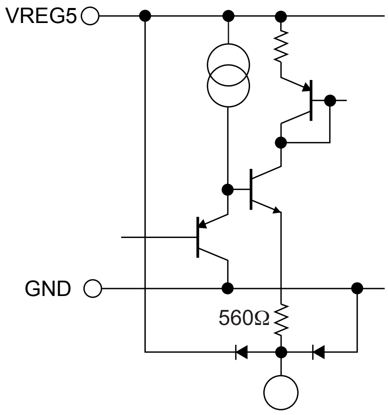
Continued on next page.

Continued from preceding page.

Pin No.	Pin	Equivalent Circuit
1 2 3 4	VG VM CP2 CP1	
21	VREF	
5	VREG5	
8 12	EMO MONI	

Continued on next page.

Continued from preceding page.

Pin No.	Pin	Equivalent Circuit
9	CEM	
11	RCHOP	

Description of operation

1. Input Pin Function

1-1) Chip enable function

This IC is switched between standby and operating mode by setting the ST pin. In standby mode, the IC is set to power-save mode and all logic is reset. In addition, the internal regulator circuit and charge pump circuit do not operate in standby mode.

ST	Mode	Internal regulator	Charge pump
Low or Open	Standby mode	Standby	Standby
High	Operating mode	Operating	Operating

1-2) Drive mode switching pin function

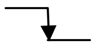
The IC drive mode is switched by setting the DM pin. In STM mode, stepper motor channel 1 can be controlled by the CLK-IN input. In DCM mode, DC motor channel 2 or stepper motor channel 1 can be controlled by parallel input. Stepper motor control using parallel input is Full-step or Half-step full torque.

DM	Drive mode	Application
Low or Open	STM mode	Stepper motor channel 1 (CLK-IN)
High	DCM mode	DC motor channel 2 or stepper motor channel 1 (parallel)

2. STM mode (DM = Low or Open)

2-1) STEP pin function

The excitation step progresses by inputting the step signal to the STP pin.

Input		Operating mode
ST	STP	
Low	*	Standby mode
High		Excitation step proceeds
High		Excitation step is kept

2-2) Excitation mode setting function

The excitation mode of the stepper motor can be set as follows by setting the MD1 pin and the MD2 pin.

MD1	MD2	Micro-step resolution (Excitation mode)	Initial position	
			Channel 1	Channel 2
Low	Low	Full step (2 phase excitation)	100%	-100%
High	Low	Half step (1-2 phase excitation) full torque	100%	0%
Low	High	Half step (1-2 phase excitation)	100%	0%
High	High	Quarter step (W1-2 phase excitation)	100%	0%

This is the initial position of each excitation mode in the initial state after power-on and when the counter is reset.

2-3) Positional detection monitor function

The MONI position detection monitoring pin is of an open drain type.
When the excitation position is in the initial position, the MONI output is placed in the ON state.
(Refer to "2-12.Examples of current waveforms in each micro-step mode.")

2-4)Constant-current control reference voltage setting function

This IC does the PWM fixed current chopping control of the current of the motor by the automatic operation in setting the output current. The output current in which a fixed current is controlled by the following calculation type is set by the resistance connected between the voltage and RF-GND being input to the VREF pin.

I_{OUT}=(VREF/5)/RF resistance

*The above-mentioned, set value is an output current of each excitation mode at 100% time.

VREF input voltage attenuation function

ATT1	ATT2	Current setting reference voltage attenuation ratio
Low	Low	100%
High	Low	66.7%
Low	High	50%
High	High	33.3%

The output ammeter calculation type when the attenuation function of the VREF input voltage is used is as follows.

IOUT=(VREF/5)×(Attenuation ratio)/RF resistance

(Example) When VREF = 1.5V, setting current ratio = 100% [(ATT1, ATT2) = (Low, Low)] and RF resistor = 0.22Ω, the following output current flows :

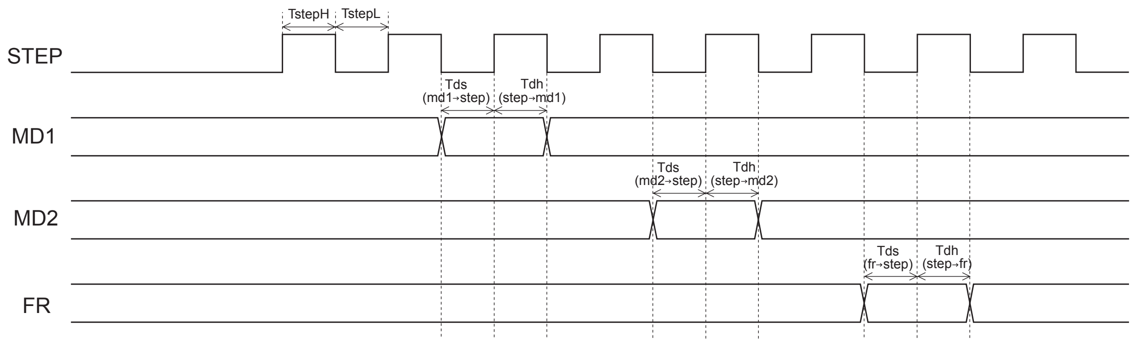
I_{OUT} = 1.5V/5×100%/0.22Ω=1.36A

Under such a condition, when assuming (ATT1, ATT2) = (High, High).

I_{OUT} = 1.36A×33.3%=453mA

The power saving can be done, and attenuating the output current when the motor energizes maintenance.

2-5) Input Timing



TstepH/TstepL : Clock H/L pulse width (min 500ns)
Tds : Data set-up time (min 500ns)
Tdh : Data hold time (min 500ns)

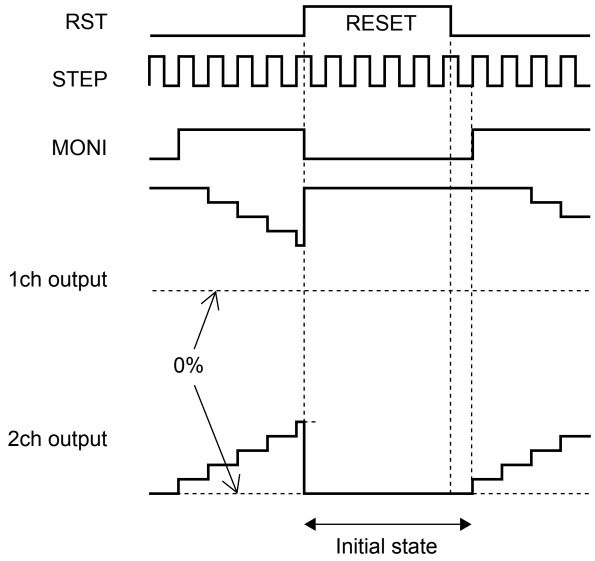
2-6) Blanking period

If, when exercising PWM constant-current chopping control over the motor current, the mode is switched from decay to charge, the recovery current of the parasitic diode may flow to the current sensing resistance, causing noise to be carried on the current sensing resistance pin, and this may result in erroneous detection. To prevent this erroneous detection, a blanking period is provided to prevent the noise occurring during mode switching from being received. During this period, the mode is not switched from charge to decay even if noise is carried on the current sensing resistance pin.

This IC's blanking period is fixed at about 1 μs in STM mode (2 μs in DCM mode).

2-7) Reset function

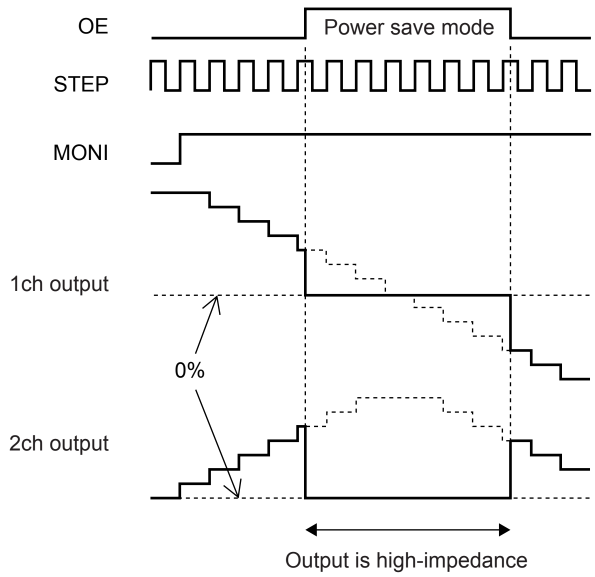
RST	Operating mode
Low	Normal operation
High	Reset state



When the RST pin is set High, the output excitation position is forced to the initial state, and the MONI output enters ON a state. When RST is set Low after that, the excitation position proceeds to the next STEP input.

2-8) Output enable function

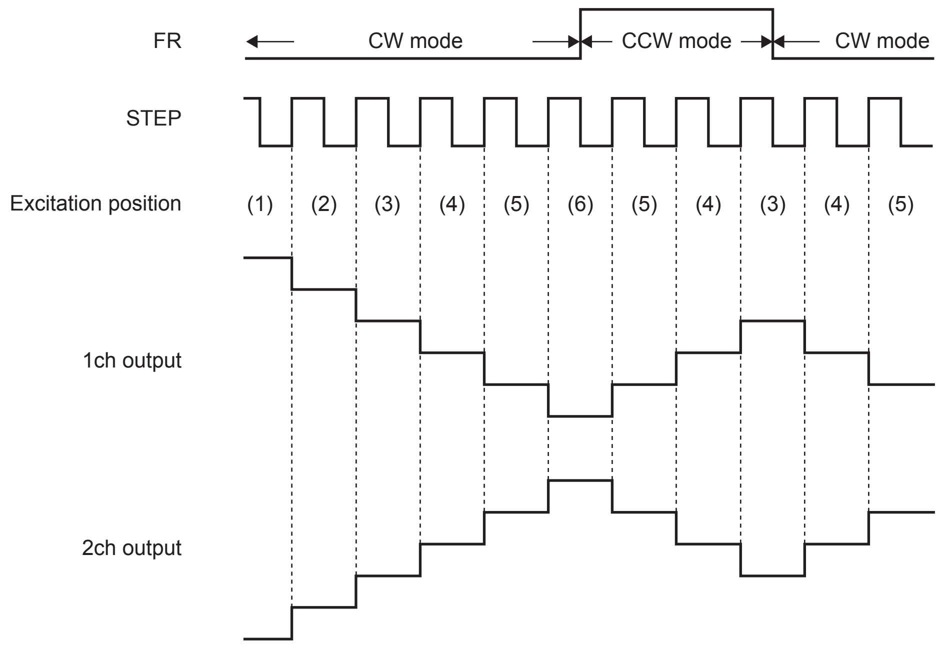
OE	Operating mode
High	Output OFF
Low	Output ON



When the OE pin is set High, the output is forced OFF and goes to high impedance.
However, the internal logic circuits are operating, so the excitation position proceeds when the STEP signal is input to the STP pin. Therefore, when OE is returned to Low, the output level conforms to the excitation position proceeded by the STEP input.

2-9) Forward/reverse switching function

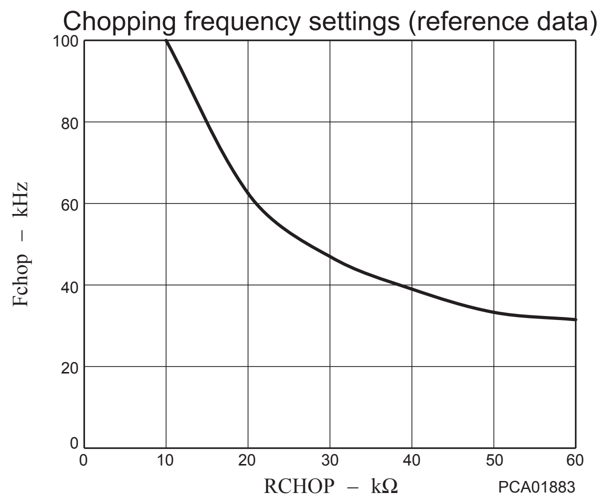
FR	Operating mode
Low	Clockwise (CW)
High	Counter-clockwise (CCW)



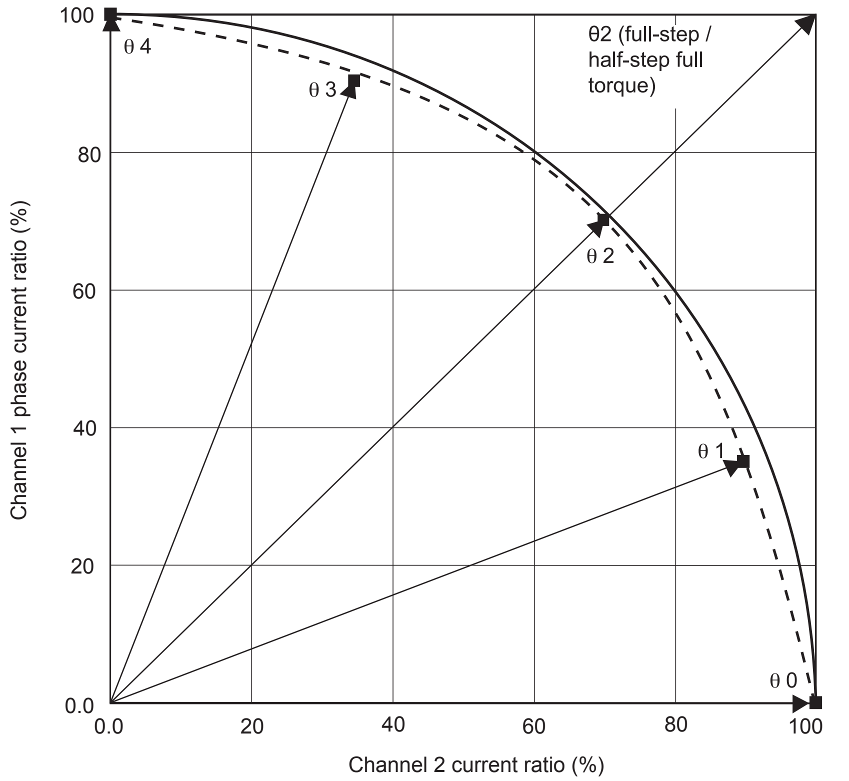
The internal D/A converter proceeds by one bit at the rising edge of the input STEP pulse.
In addition, CW and CCW mode are switched by setting the FR pin.
In CW mode, the channel 2 current phase is delayed by 90° relative to the channel 1 current.
In CCW mode, the channel 2 current phase is advanced by 90° relative to the channel 1 current.

2-10) Setting the chopping frequency

For constant-current control, chopping operation is made with the frequency determined by the external resistor (connected to the RCHOP pin).
The chopping frequency to be set with the resistance connected to the RCHOP pin (pin 11) is as shown below.



2-11) Output current vector locus (one step is normalized to 90 degrees)

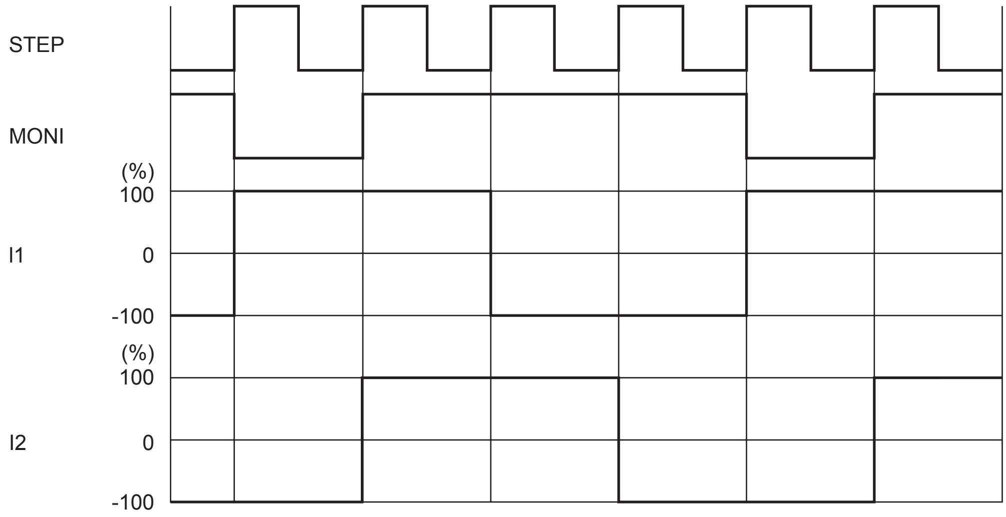


Setting current ration in each micro-step mode

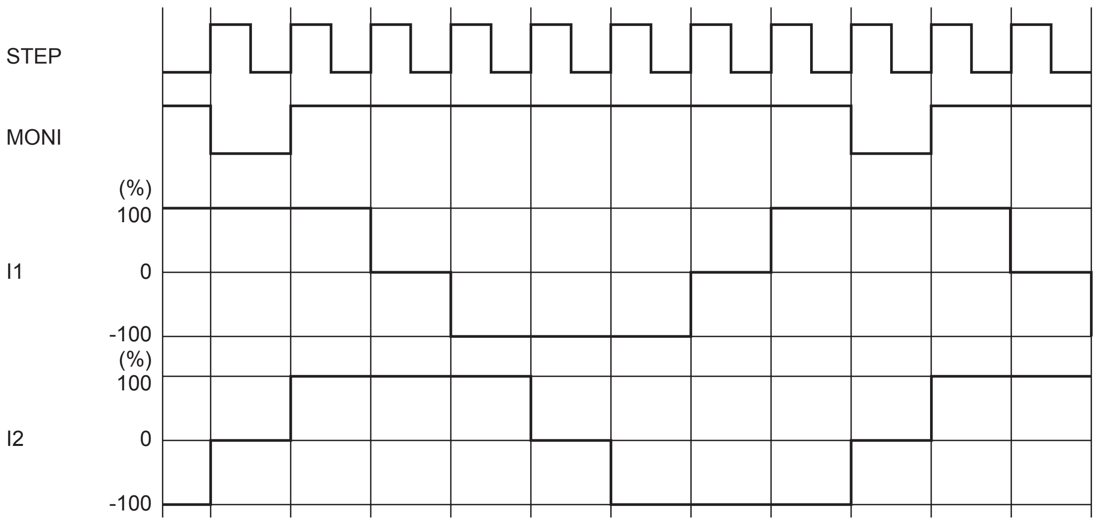
STEP	Quarter-step (%)		Half-step (%)		Half-step full torque (%)		Full-step (%)	
	Channel 1	Channel 2	Channel 1	Channel 2	Channel 1	Channel 2	Channel 1	Channel 2
θ0	0	100	0	100	0	100		
θ1	35	90						
θ2	70	70	70	70	100	100	100	100
θ3	90	35						
θ4	100	0	100	0	100	0		

2-12) Examples of current waveforms in each micro-step mode

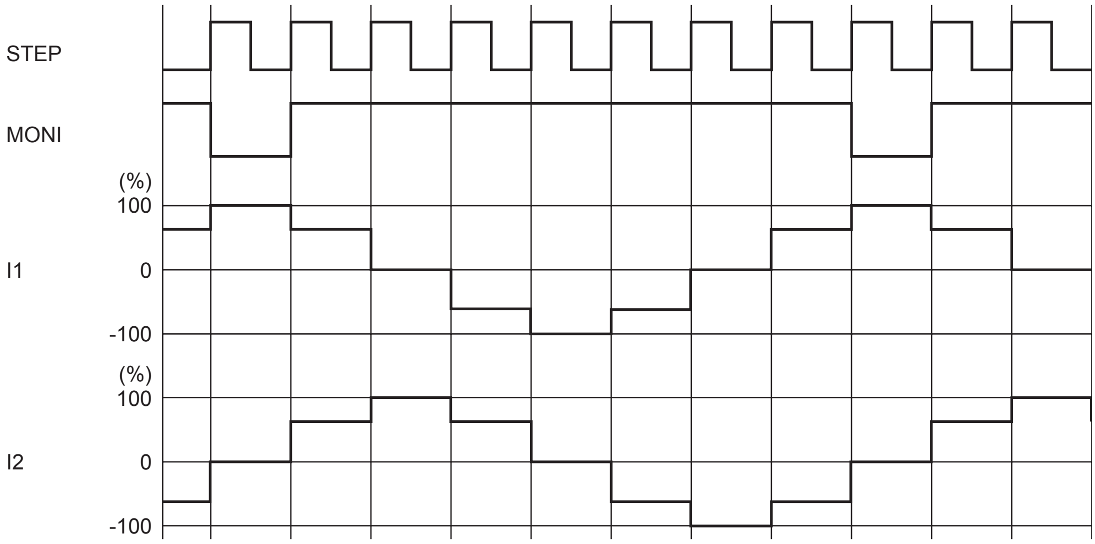
Full step (CW mode)



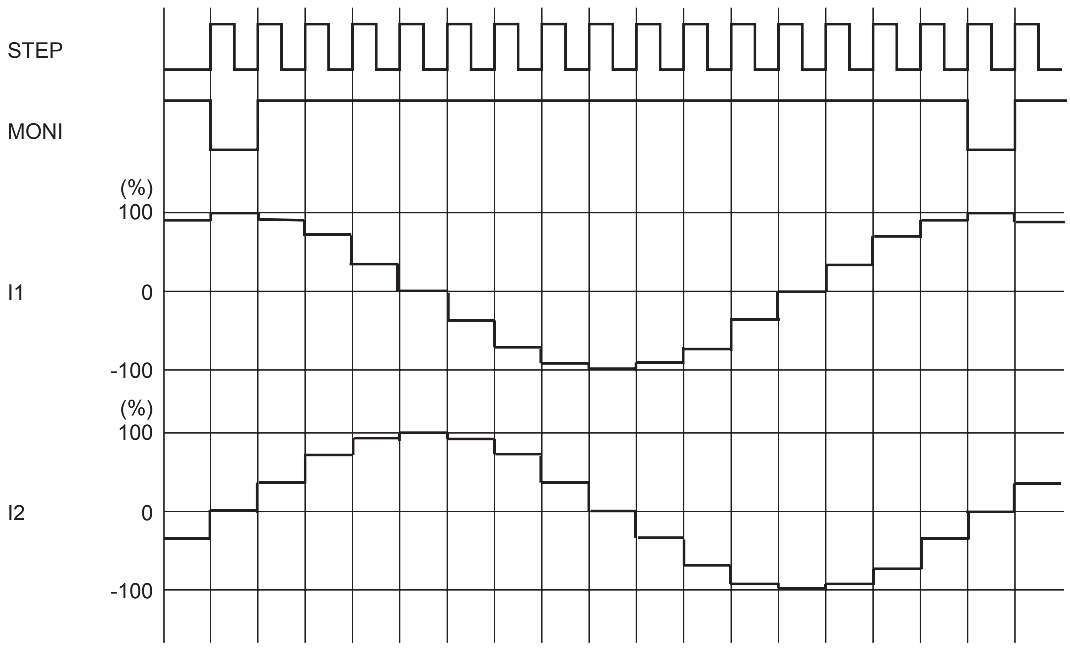
Half step full torque (CW mode)



Half step (CW mode)

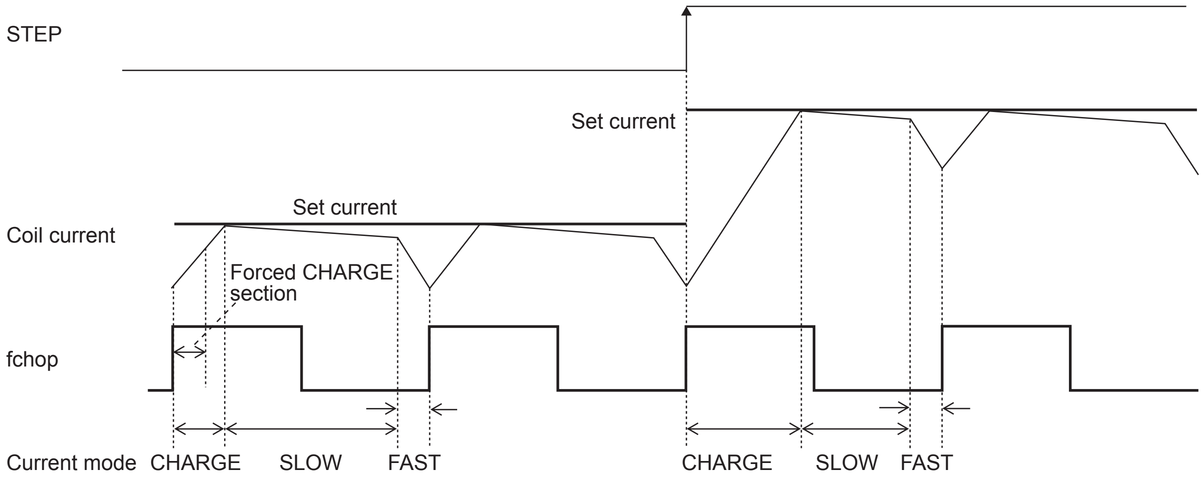


Quarter step (CW mode)

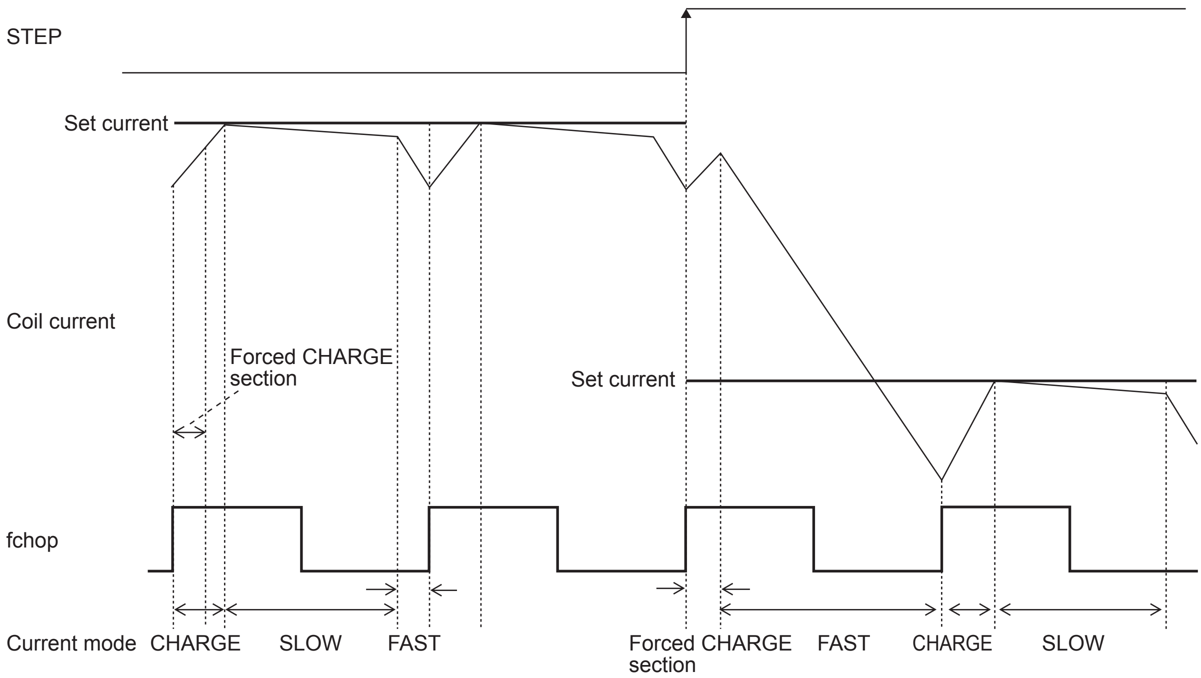


2-13) Current control operation specification

(Sine wave increasing direction)



(Sine wave decreasing direction)



In each current mode, the operation sequence is as described below :

- At rise of chopping frequency, the CHARGE mode begins.(The section in which the CHARGE mode is forced regardless of the magnitude of the coil current (ICOIL) and set current (IREF) exists for 1/16 of one chopping cycle.)
- The coil current (ICOIL) and set current (IREF) are compared in this forced CHARGE section.

  When (ICOIL<IREF) state exists in the forced CHARGE section ;

    CHARGE mode up to ICOIL ≥ IREF, then followed by changeover to the SLOW DECAY mode, and finally by the FAST DECAY mode for the 1/16 portion of one chopping cycle.

  When (ICOIL<IREF) state does not exist in the forced CHARGE section;

    The FAST DECAY mode begins. The coil current is attenuated in the FAST DECAY mode till one cycle of chopping is over.

Above operations are repeated. Normally, the SLOW (+FAST) DECAY mode continues in the sine wave increasing direction, then entering the FAST DECAY mode till the current is attenuated to the set level and followed by the SLOW DECAY mode.

3.DCM Mode (DM-High)

3-1) DCM mode output control logic

Parallel input		Output		Mode
DC11 (21)	DC12 (22)	OUT1 (2) A	OUT1 (2) B	
Low	Low	OFF	OFF	Standby
High	Low	High	Low	CW (Forward)
Low	High	Low	High	CCW (Reverse)
High	High	Low	Low	Brake

3-2) Reset function

RST	Operating mode	MONI
High or Low	Reset operation not performed	High output

The reset function does not operate in DCM mode. In addition, the MONI output is High, regardless of the RST pin state.

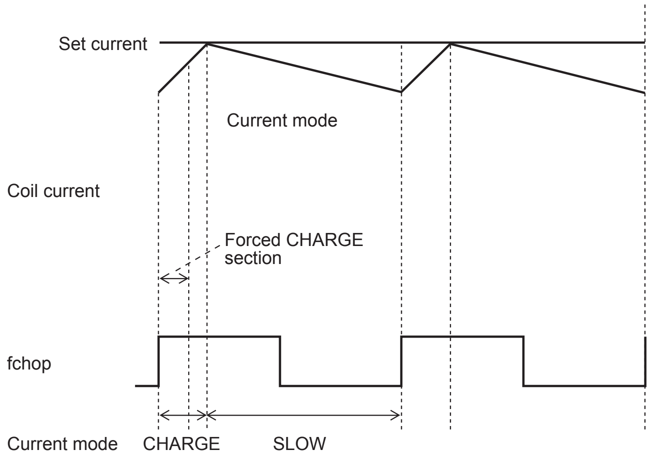
3-3) Output enable function

OE	Operating mode
High	Output OFF
Low	Output ON

When the OE pin is set High, the output is forced OFF and goes to high impedance. When the OE pin is set Low, output conforms to the control logic.

3-4) Current limit control time chart

When the current of the motor reaches up to the limit current by setting the current limit, this IC does the short brake control by the automatic operation so that the current should not increase more than it.



Moreover, the voltage impressed to the terminal VREF can be switched to the setting of four stages by the state of two input of ATT1 and ATT2.

VREF input voltage attenuation function

ATT1	ATT2	Current setting reference voltage
Low	Low	100%
High	Low	66.7%
Low	High	50%
High	High	33.3%

The output ammeter calculation type when the attenuation function of the VREF input voltage is used is as follows.

IOUT=(VREF/5)×(Attenuation ratio)/RF resistance

(Example) When VREF = 1.5V, setting current ratio = 100% [(ATT1, ATT2) = (Low, Low)] and RF resistor = 0.22Ω, the following output current flows :

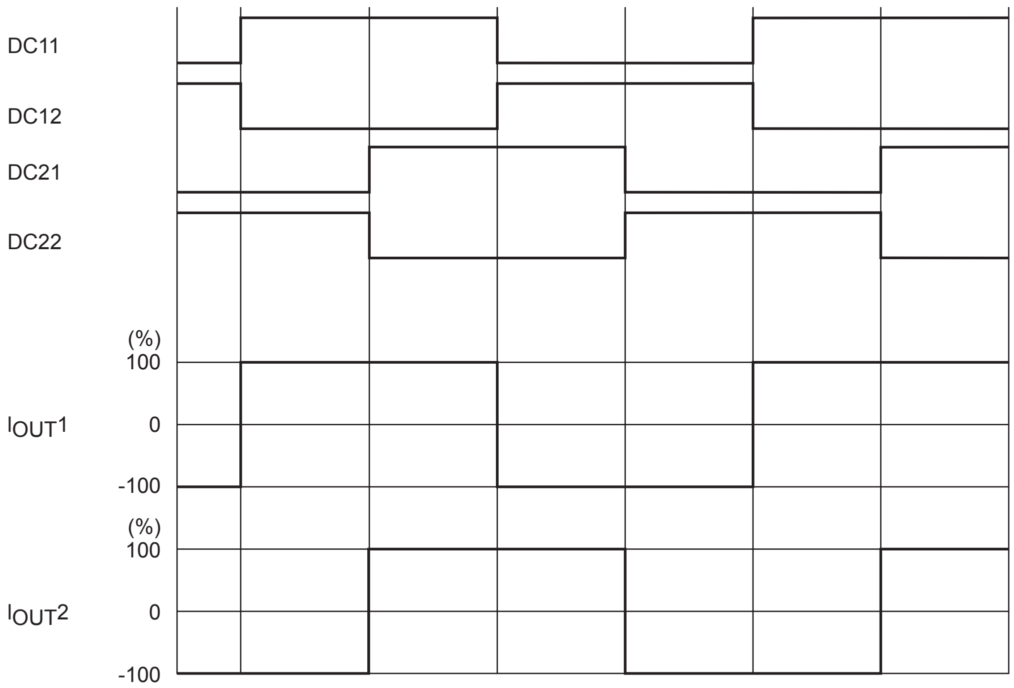
I_{OUT} = 1.5V/5×100%/0.22Ω=1.36A

Under such a condition, when assuming (ATT1, ATT2) = (High, High).

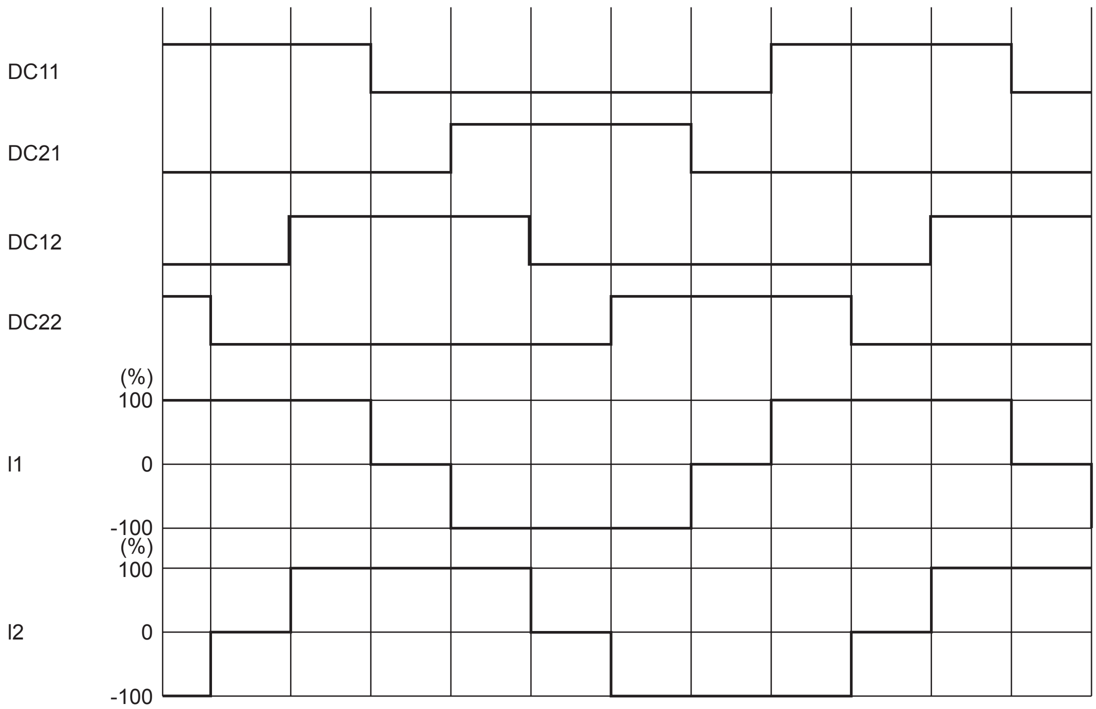
I_{OUT} = 1.36A×33.3%=453mA

3-5) Examples of current waveform in each micro-step mode when stepper motor parallel input control

Full step (CW mode)



Half step full torque (CW mode)



4.Output short-circuit protection circuit

This output short protection circuit that makes the output a standby mode to prevent the thing that IC destroys when the output is short-circuited by a voltage short and the earth fault, etc. , and turns on the warning output to IC is built into.

4-1) Output short-circuit protection mode switching function

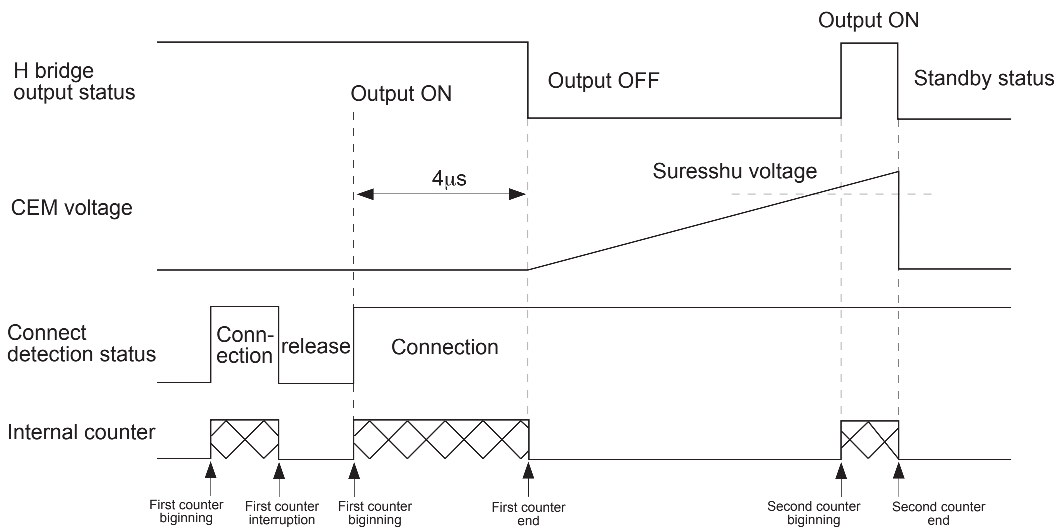
Output short-circuit protection mode of IC can be switched by the setting of EMM pin.

EMM	State
Low or Open	Latch method
High	Auto reset method

4-2) Latch method

In the latch mode, the output is turned off when the output current exceeds the detection current, and the state is maintained.

The output short protection circuit starts operating so that IC may detect a short output. When the short-circuit is the consecutive between internal timers (≈4μs), the output where the short-circuit is first detected is turned off. Even if the following time (Tcem) of the timer latch is exceeded, the output is turned ON again, and afterwards, when the short-circuit is detected, all the outputs of correspondence ch side are still switched to the standby mode, and the state is maintained. This state is released by making it to ST ="L".



4-3) Automatic return method

In the automatic return mode, the output wave type changes into the switching wave type when the output current exceeds the detection current.

The short-circuit detection circuit operates when a short output is detected as well as the latch method. The output is switched to the standby mode when the operation of the short-circuit detection circuit exceeds the following time (Tcem) of the timer latch, and it returns to the turning on mode again after 2ms(TYP). At this time, the above-mentioned switching mode is repeated when is still in the over current mode until the over current mode is made clear.

4-4) Abnormal state warning output pin

When IC operates the protection circuit detecting abnormality, the EMO pin has been installed as a terminal that outputs this abnormality to CPU side. This pin is an open drain output, and if abnormality is detected, the EMO output becomes (EMO="L") of ON.

EMO pin enters on a state in the following.

- When a voltage short, the earth fault or the load is short-circuited and the output short-circuit protection circuit operates, the output pin
- When the junction temperature of IC rises, and the overheating protection circuit operates

4-5) Timer latch time (Tcem)

The time to output OFF when an output short-circuit occurs can be set by the capacitor connected between the CEM pin and GND. The capacitor (Ccem) value can be determined as follows :

Timer latch : Tcem $Tcem \approx C \times V/I$ [sec]

V : Threshold voltage of comparator TYP 1V

I : CEM charge current TYP 10μA

5.Thermal shutdown function

The thermal shutdown circuit is included, and the output is turned off when junction temperature Tj exceeds 180°C and the abnormal state warning output is turned on at the same time.

When the temperature falls hysteresis level, output is driven again (automatic restoration)

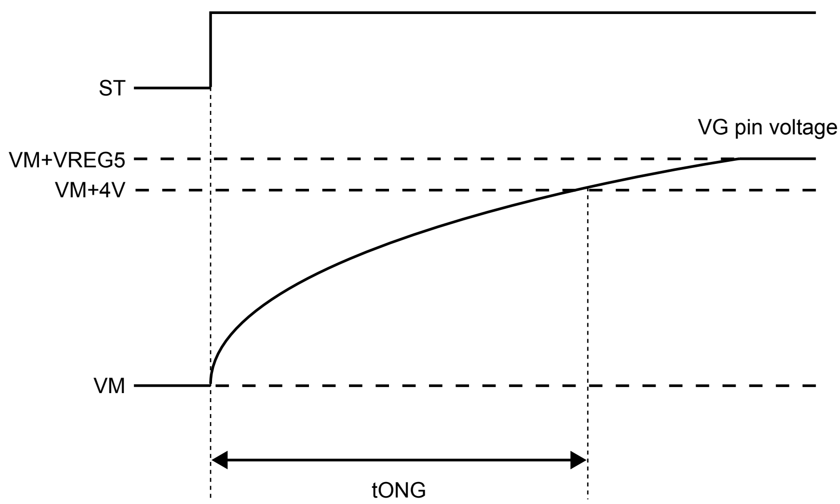
The thermal shutdown circuit doesn't guarantee protection of the set and the destruction prevention of IC, because it works at the temperature that is higher than rating (Tjmax=150°C) of the junction temperature

TTSD = 180°C (typ)

ΔTSD = 40°C (typ)

6.Charge Pump Circuit

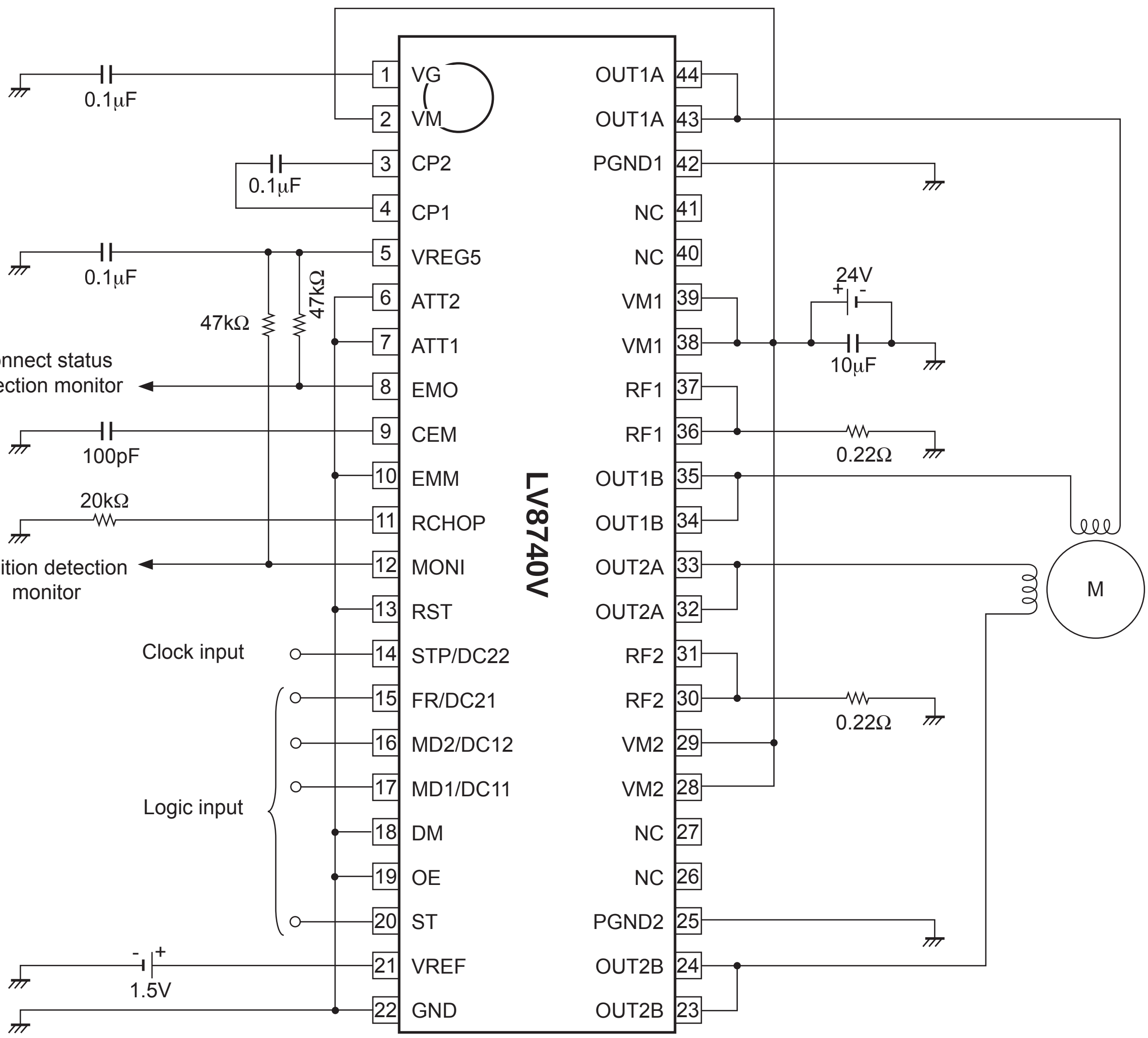
When the ST pin is set High, the charge pump circuit operates and the VG pin voltage is boosted from the VM voltage to the VM + VREG5 voltage. If the VG pin voltage is not boosted to VM+4V or more, the output pin cannot be turned on. Therefore it is recommended that the drive of motor is started after the time has passed tONG or more.



VG Pin Voltage Schematic View

Application Circuits

1. Stepper motor driver application circuit example(DM=”L”)



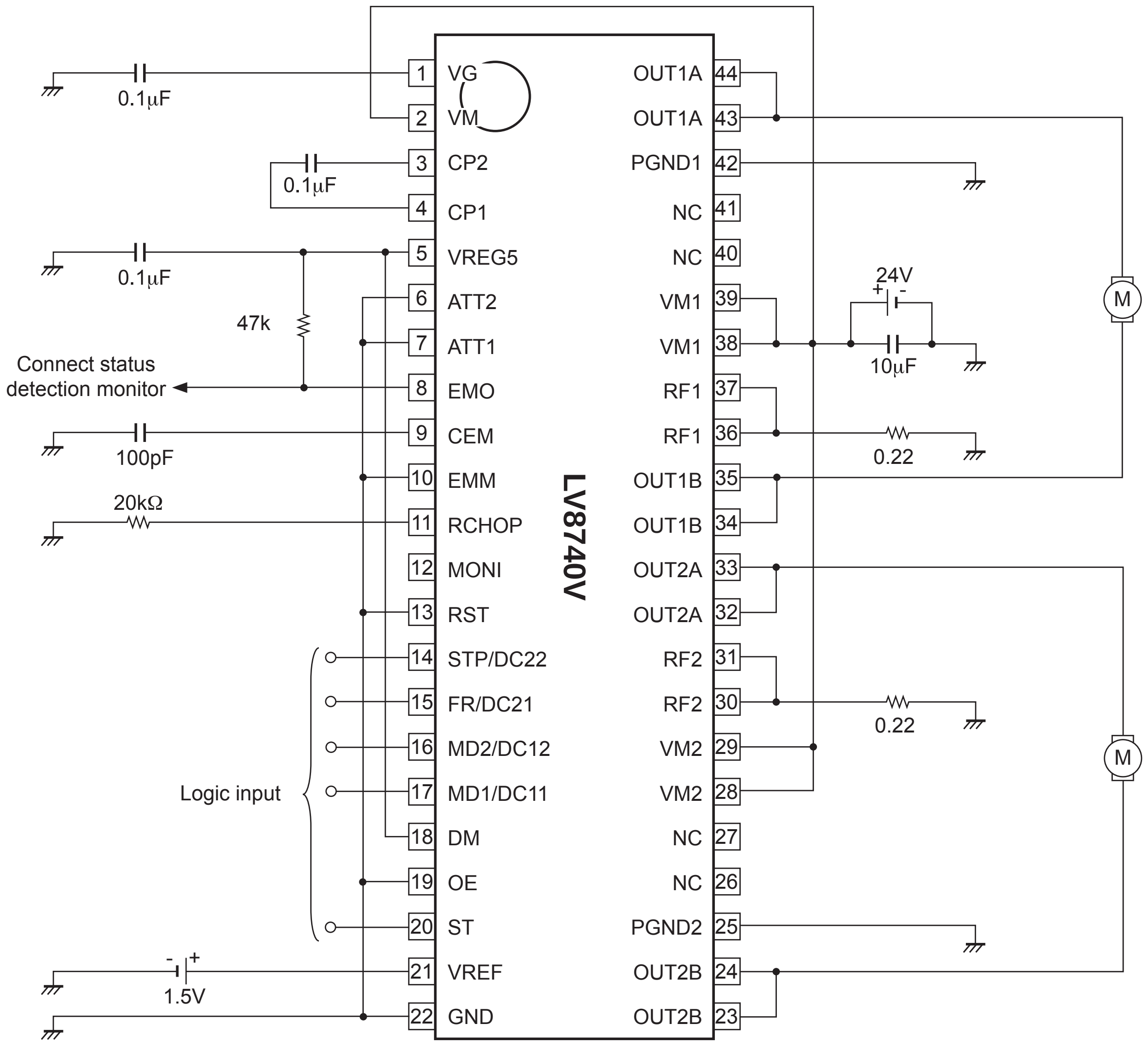
Each constant setting type in the example of the above-mentioned circuit is as follows.
When setting current ratio = 100%, VREF = 1.5V, the following output current flows :

I_{OUT} = VREF/5/RF resistance
= 1.5V/5×100%/0.22Ω=1.36A

Chopping frequency setting.
62.5kHz (RCHOP=20kΩ)

Time of timer latch when output is short-circuited
Tcem = Ccem * Vtcem/Icem
= 100pF * 1V/10μA = 10μs

2. DC motor driver application circuit example



Each constant setting type in the example of the above-mentioned circuit is as follows.

When setting current LIMIT = 100%, VREF = 1.5V, the following output current flows :

Ilimit = VREF/5/RF resistance

= 1.5V/5×100%/0.22Ω=1.36A

Chopping frequency setting.

62.5kHz (RCHOP=20kΩ)

Time of timer latch when output is short-circuited

Tcem = Ccem * Vtcem/Icem

= 100pF * 1V/10μA = 10μs

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV8740V-TLM-E	SSOP44J (275mil) (Pb-Free)	2000 / Tape & Reel
LV8740V-MPB-E	SSOP44J (275mil) (Pb-Free)	30 / Fan-Fold