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LV8760T

Bi-CMOS LSI

Forward/Reverse H-bridge Driver

Overview

The LV8760T is an H-bridge driver that can control four operation modes (forward, reverse, brake, and standby) of a motor. The low on-resistance, zero standby current, highly efficient IC is optimal for use in driving brushed DC motors for office equipment.

Features

- Forward/reverse H-bridge motor driver: 1 channel
- Built-in current limiter circuit
- Built-in thermal protection circuit
- Built-in short-circuit protection function

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|--------------|----------------------------------|----------------------|------------------|
| Supply voltage | V_M max | | 38 | V |
| | V_{CC} max | | 6 | V |
| Output peak current | I_O peak | $t_w \leq 20\text{ms}$, duty 5% | 4 | A |
| Output continuous current | I_O max | | 3 | A |
| Logic input voltage | V_{IN} | | -0.3 to $V_{CC}+0.3$ | V |
| Allowable power dissipation | P_d max | Mounted on a specified board. * | 3.3 | W |
| Operating temperature | T_{opr} | | -20 to +85 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +150 | $^\circ\text{C}$ |

* Specified circuit board : 90mm×90mm×1.6mm, glass epoxy 2-layer board (2SOP), with backside mounting.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Allowable Operating Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------|-----------------|------------|---------------------------|------|
| Supply voltage range | VM | | 9 to 35 | V |
| | V _{CC} | | 3 to 5.5 | V |
| VREF input voltage | VREF | | 0 to V _{CC} -1.8 | V |
| Logic input voltage | V _{IN} | | 0 to V _{CC} | V |

Electrical Characteristics at Ta = 25°C, VM = 24V, V_{CC} = 5V, VREF = 1.5V

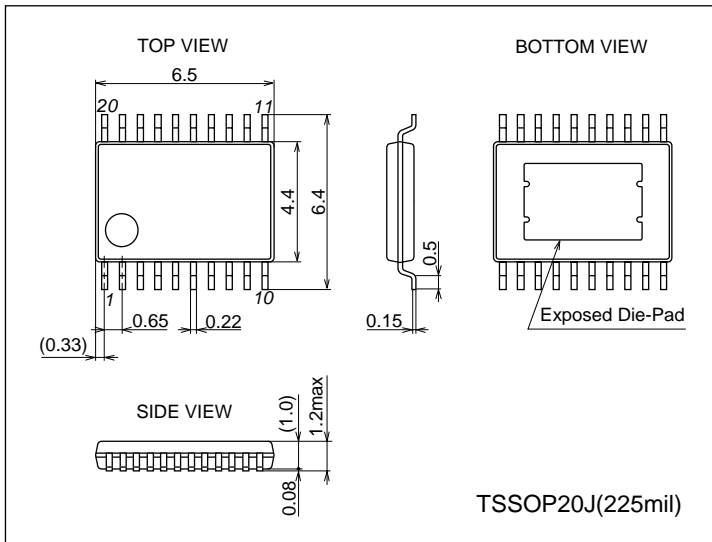
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|-------------------------------|--|---------|------|-------|------|
| | | | min | typ | max | |
| General | | | | | | |
| Standby mode current drain 1 | IMst | PS = "L" | | | 1 | μA |
| Standby mode current drain 2 | I _{CCst} | PS = "L" | | | 1 | μA |
| Operating mode current drain 1 | IM | PS = "H", IN1 = "H", with no load | | 1 | 1.3 | mA |
| Operating mode current drain 2 | I _{CC} | PS = "H", IN1 = "H", with no load | | 3 | 4 | mA |
| VREG output voltage | VREG | I _O = -1mA | 4.75 | 5 | 5.25 | V |
| V _{CC} low-voltage cutoff voltage | V _{thV_{CC}} | | 2.5 | 2.7 | 2.9 | V |
| Low-voltage hysteresis voltage | V _{thHIS} | | 120 | 150 | 180 | mV |
| Thermal shutdown temperature | TSD | Design guarantee * | 155 | 170 | 185 | °C |
| Thermal hysteresis width | ΔTSD | Design guarantee * | | 40 | | °C |
| Output block | | | | | | |
| Output on resistance | Ron1 | I _O = 3A, sink side | | 0.2 | 0.25 | Ω |
| | Ron2 | I _O = -3A, source side | | 0.32 | 0.40 | Ω |
| Output leakage current | I _{Oleak} | V _O = 35V | | | 50 | μA |
| Rising time | tr | 10% to 90% | | 200 | 500 | ns |
| Falling time | tf | 90% to 10% | | 200 | 500 | ns |
| Input output delay time | tpLH | IN1 or IN2 to OUTA or OUTB (L → H) | | 550 | 700 | ns |
| | tpHL | IN1 or IN2 to OUTA or OUTB (H → L) | | 550 | 700 | ns |
| Charge pump block | | | | | | |
| Step-up voltage | VGH | VM = 24V | 28.0 | 28.7 | 29.8 | V |
| Rising time | tONG | VG = 0.1μF | | 250 | 500 | μs |
| Oscillation frequency | Fcp | | 115 | 140 | 165 | kHz |
| Control system input block | | | | | | |
| Logic pin input current 1 | I _{INL} | V _{IN} = 0.8V adaptive pin : PS | 5.6 | 8 | 10.4 | μA |
| | I _{INH} | V _{IN} = 5V adaptive pin : PS | 56 | 80 | 104 | μA |
| Logic pin input current 2 | I _{INL} | V _{IN} = 0.8V adaptive pin : IN1, IN2 | 5.6 | 8 | 10.4 | μA |
| | I _{INH} | V _{IN} = 5V adaptive pin : IN1, IN2 | 35 | 50 | 65 | μA |
| Logic pin input H-level voltage | V _{INH} | adaptive pin : PS, IN1, IN2 | 2.0 | | | V |
| Logic pin input L-level voltage | V _{INL} | adaptive pin : PS, IN1, IN2 | | | 0.8 | V |
| Current limiter block | | | | | | |
| VREF input current | IREF | | -0.5 | | | μA |
| Current limit comparator threshold voltage | V _{thlim} | VREF = 1.5V | 0.285 | 0.3 | 0.315 | V |
| Blanking time | Tblk | | 1.6 | 2.0 | 2.4 | μs |
| Short-circuit protection block | | | | | | |
| SCP pin charge current | Iscp | SCP = 0V | 3.5 | 5 | 6.5 | μA |
| Comparator threshold voltage | V _{thscp} | | 0.8 | 1 | 1.2 | V |

* Design guarantee value and no measurement is made.

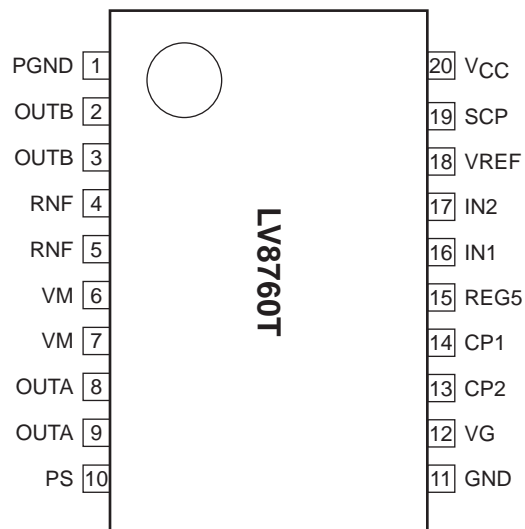
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Package Dimensions

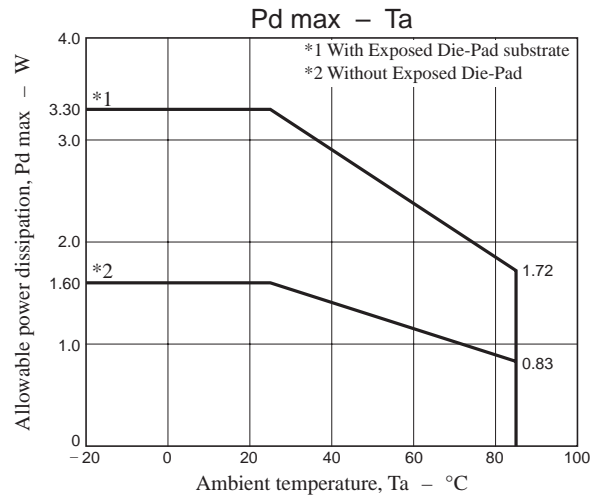
unit : mm (typ)
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Pin Assignment

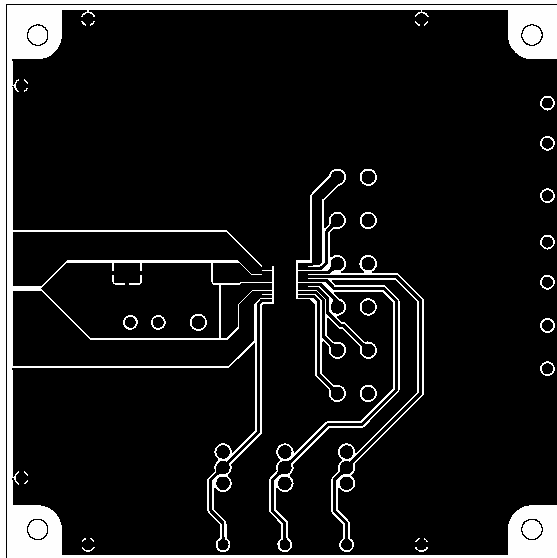


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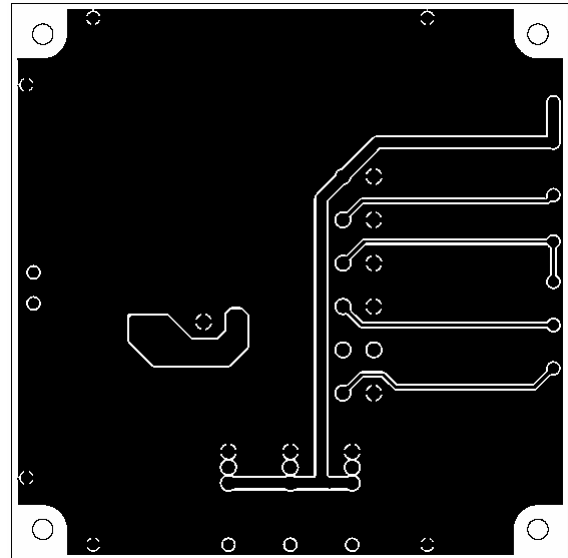


Substrate Specifications (Substrate recommended for operation of LV8760T)

Size : 90mm × 90mm × 1.6mm (two-layer substrate [2S0P])
Material : Glass epoxy
Copper wiring density : L1 = 95% / L2 = 95%



L1 : Copper wiring pattern diagram

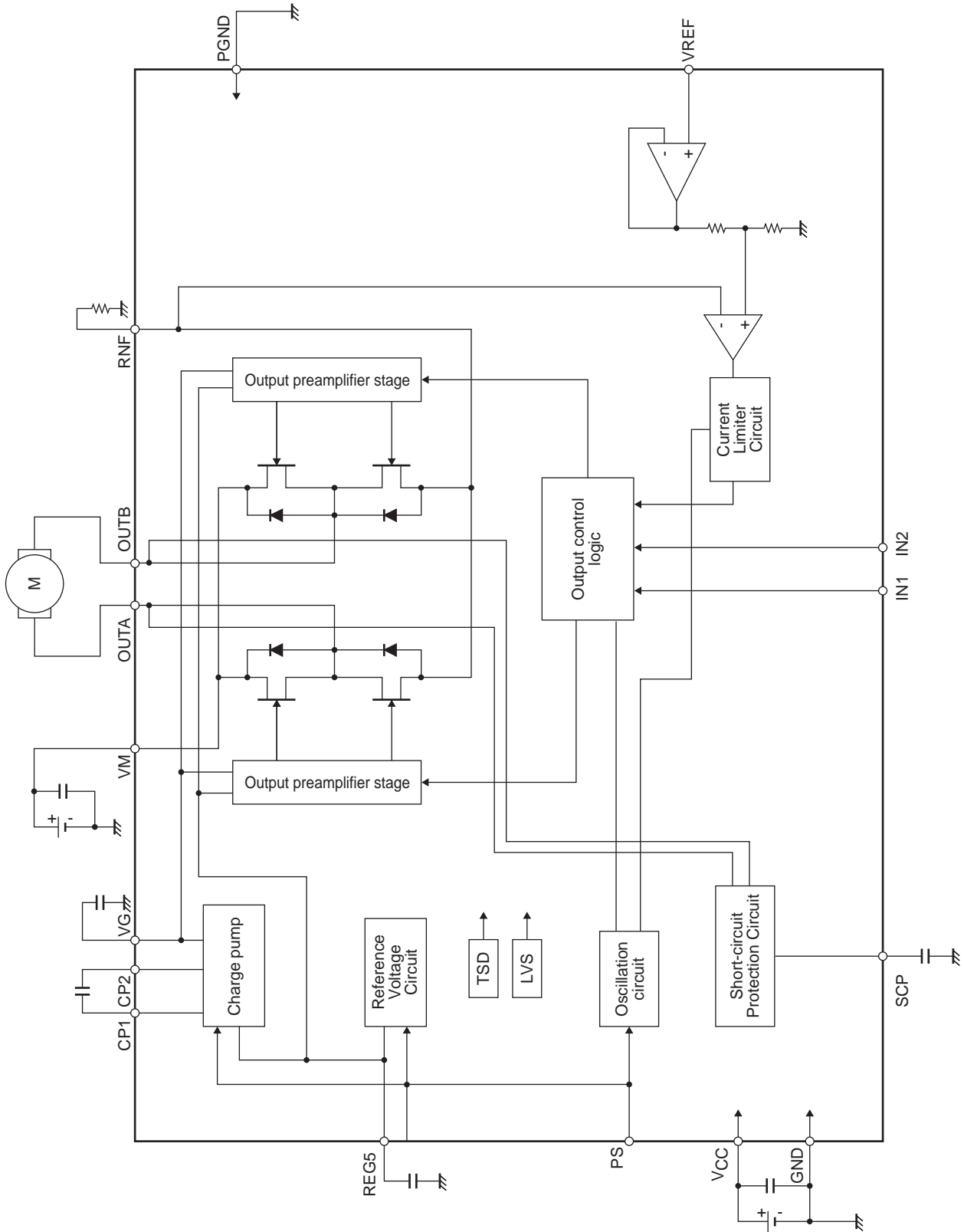


L2 : Copper wiring pattern diagram

Cautions

- 1) The data for the case with the Exposed Die-Pad substrate mounted shows the values when 90% or more of the Exposed Die-Pad is wet.
- 2) For the set design, employ the derating design with sufficient margin.
Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stresses such as vibration, impact, and tension.
Accordingly, the design must ensure these stresses to be as low or small as possible.
The guideline for ordinary derating is shown below :
 - (1)Maximum value 80% or less for the voltage rating
 - (2)Maximum value 80% or less for the current rating
 - (3)Maximum value 80% or less for the temperature rating
- 3) After the set design, be sure to verify the design with the actual product.
Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc.
Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal conduction, possibly resulting in thermal destruction of IC.

Block Diagram



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Pin Functions

| Pin No. | Pin Name | Pin Function | Equivalent Circuit |
|----------|-----------------|--|--------------------|
| 16 17 | IN1 IN2 | Output control signal input pin 1. Output control signal input pin 2. | |
| 10 | PS | Power save signal input pin. | |
| 18 | VREF | Reference voltage input pin for output current limit setting. | |
| 19 | SCP | Short-circuit protection circuit, detection time setting capacitor connection pin. | |
| 20 | V _{CC} | Power supply connection pin for control block. | |

Continued on next page.

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Continued from preceding page.

| Pin No. | Pin Name | Pin Function | Equivalent Circuit |
|-----------------------------------|-----------------------------------|---|--------------------|
| 6, 7 8, 9 4, 5 2, 3 1 | VM OUTA RNF OUTB PGND | Motor power-supply connection pin. OUTA output pin. Current sense resistor connection pin. OUTB output pin. Power ground. | |
| 14 13 12 | CP1 CP2 VG | Charge pump capacitor connection pin. Charge pump capacitor connection pin. Charge pump capacitor connection pin. | |
| 15 | REG5 | Internal reference voltage output pin. | |
| 11 | GND | Ground. | |

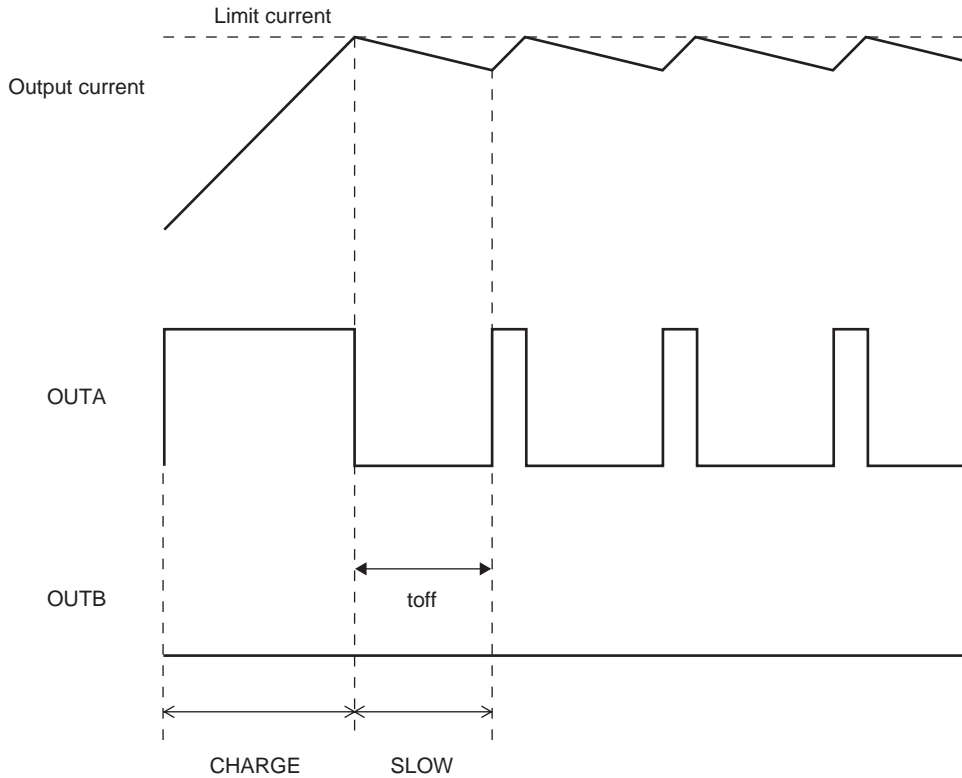
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DC Motor Driver

1.DCM output control logic

| Control Input | | | Output | | Mode |
|---------------|-----|-----|--------|------|---------------|
| PS | IN1 | IN2 | OUTA | OUTB | |
| L | * | * | OFF | OFF | Standby |
| H | L | L | OFF | OFF | Output OFF |
| H | H | L | H | L | CW (forward) |
| H | L | H | L | H | CCW (reverse) |
| H | H | H | L | L | Brake |

2.Current limit control timing chart



Braking operation time in current limit mode can be set by connecting a capacitor between SCP and GND pins. This setting is the same as the time setting required to turn off the outputs when an output short-circuit occurs as explained in the section entitled "Output Short-circuit Protection Function." See "Output Short-circuit Protection Function," for the setting procedure.

3.Setting the current limit value

The current limit value of the DCM driver is determined by the VREF voltage and the resistance (RNF) connected across the RNF and GND pins using the following formula :

$$I_{\text{limit}} [\text{A}] = (\text{VREF} [\text{V}] / 5) / \text{RNF} [\Omega]$$

Assuming VREF = 1.5V, RNF = 0.2Ω, the current limit is :

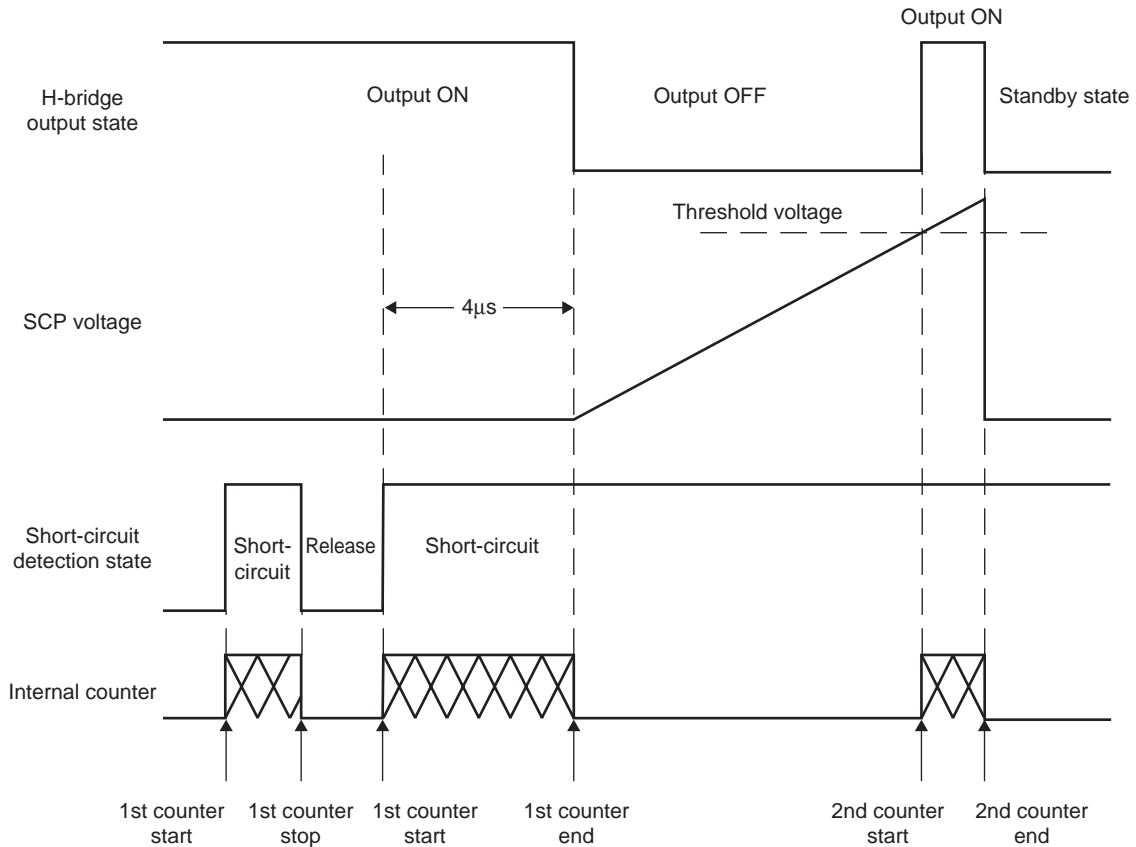
$$I_{\text{limit}} = 1.5\text{V} / 5 / 0.2\Omega = 1.5\text{A}$$

Output short-circuit protection function

The LV8760T incorporates an output short-circuit protection circuit. It turns the outputs off to prevent destruction of the IC if a problem such as an output pin being shorted to the motor power supply or ground occurs.

1. Protection function operation (Latch method)

The short-circuit protection circuit is activated when it detects the output short-circuit state. If the short-circuit state continues for the internally preset period ($\approx 4\mu\text{s}$), the protection circuit turns off the output from which the short-circuit state has been detected. Then it turns the output on again after a lapse of the timer latch time described later. If the short-circuit state is still detected, it changes all the outputs to the standby mode and retains the state. The latched state is released by setting the PS to L.



2. How to set the SCP pin constant (timer latch-up setting)

The user can set the time at which the outputs are turned off when a short-circuit occurs by connecting a capacitor across the SCP and GND pins. The value of the capacitor can be determined by the following formula :

Timer latch-up : T_{ocp}

$$T_{ocp} \approx C \times V / I \text{ [s]}$$

V : Comparator threshold voltage (1V typical)

I : SCP charge current ($5\mu\text{A}$ typical)

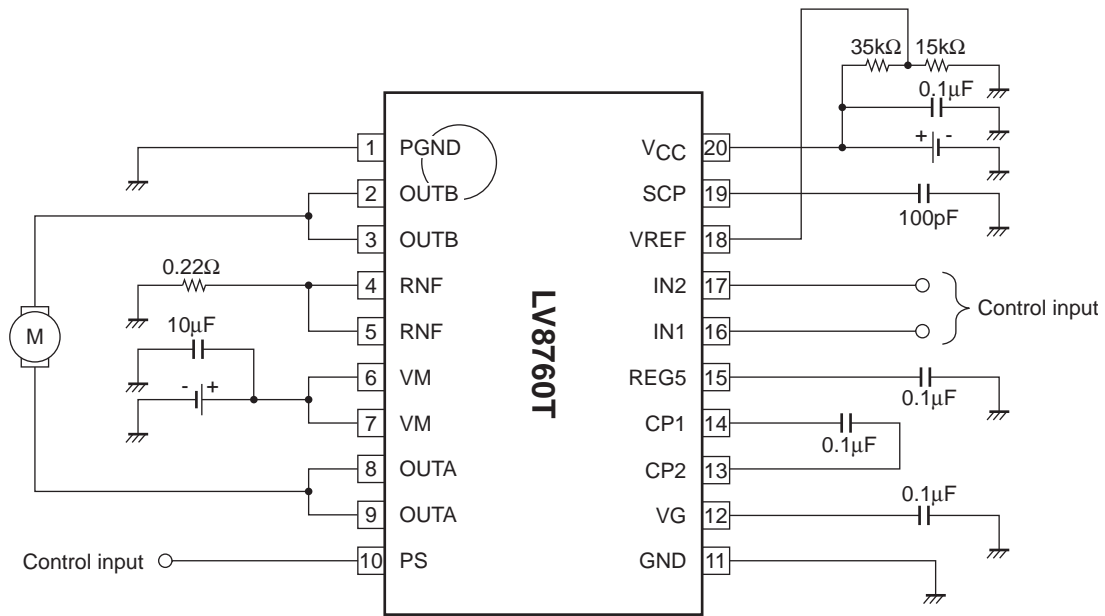
When a capacitor with a capacitance of 50pF is connected across the SCP and GND pins, for example, T_{scp} is calculated as follows :

$$T_{scp} = 50\text{pF} \times 1\text{V} / 5\mu\text{A} = 10\mu\text{s}$$

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Application Circuit Example

(When you use the current limit function)



Setting the current limit value

When $V_{CC} = 5V$,

$V_{ref} = 1.5V$

$I_{limit} = V_{ref}/5/R_{NF}$

$= 1.5V/5/0.22\Omega = 1.36A$

Setting the current limit regeneration time and short-circuit detection time

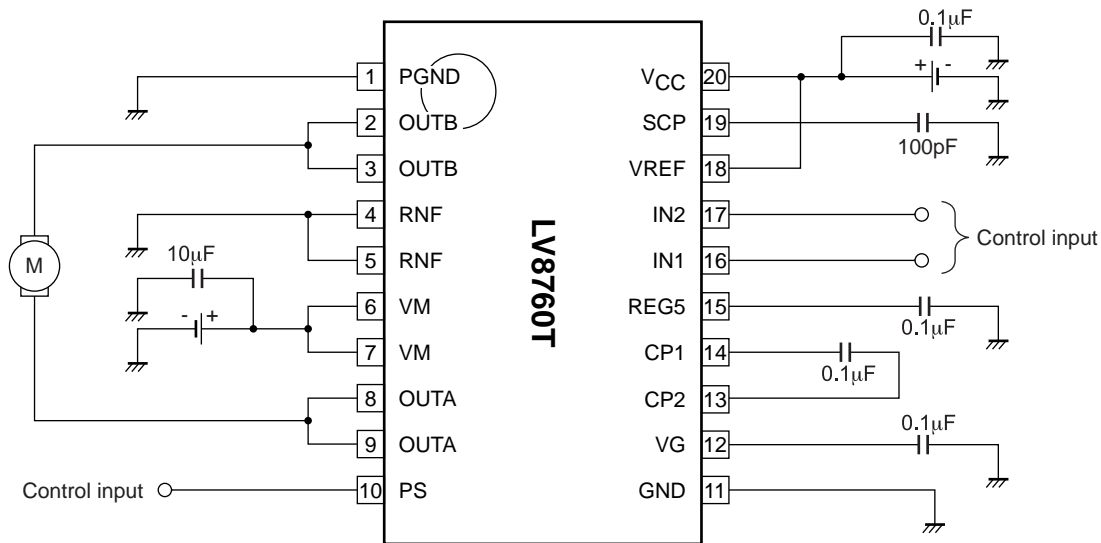
$T_{scp} \approx C \times V/I$

$= 100pF \times 1V/5\mu A$

$= 20\mu s$

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(When you do not use the current limit function)



Setting at short-circuit state detection time

$$\begin{aligned}
 T_{SCP} &\approx C \cdot V / I \\
 &= 100\text{pF} \cdot 1\text{V} / 5\mu\text{A} \\
 &= 20\mu\text{s}
 \end{aligned}$$

*Do the following processing when you do not use the current limit function.

- It is short between RNF-GND.
- The terminal VREF is hung on suitable potential of VCC or less.

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