## LV8860V

Bi-CMOS IC
Fan Motor Driver
ON Semiconductor ${ }^{\text {® }}$
http://onsemi.com

## Single-Phase Full-Wave Driver

## Overview

LV8860V is a driver IC used for single-phase fan motor. High-efficiency and low-noise are realized by reducing reactive power using Silent PWM.
The operating range of LV8860V is wide. LV8860V also corresponds to 24 V . Therefore, it is optimal for office automation equipment and factory automation equipment.

## Functions

- Single-phase full wave operation by Silent PWM drive.
- Speed is controllable by PWM input.
- Hall bias output pin.
- Integrated Quick Start Circuit.
- FG (rotation detection) / RD (lock detection) output pin (open drain output)
- Integrated current limiter circuit (limit at $\mathrm{I}=450 \mathrm{~mA}$ with $\mathrm{Rf}=0.5 \Omega$ connection, limit value is determined based on Rf.)
- Integrated lock protector circuit and automatic recovery circuit.
- Integrated thermal shut-down (TSD) circuit.


## Specifications

Maximum Ratings at $\mathrm{Ta}=25^{\circ} \mathrm{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Maximum supply voltage | $\mathrm{V}_{\text {CC }}$ max |  | 36 | V |
| OUT pin output current | IOUT max |  | 0.7 | A |
| Output withstand | $\mathrm{V}_{\text {OUT }}$ max |  | 36 | V |
| RD/FG output pin withstand | $V_{\text {RD/FG }}$ max |  | 36 | V |
| RD/FG output maximum current | IRD/FG max |  | 10 | mA |
| RGL output maximum current | ${ }^{\text {IRGL }}$ max |  | 5 | mA |
| HB output maximum current | IHB max |  | 10 | mA |
| PWM input pin withstand | VPWM max |  | 6 | V |
| Allowable power dissipation | Pd max | * On a specified board | 0.8 | W |
| Operating temperature | Topr |  | -40 to +95 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | Tstg |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

*Specified board: $114.3 \mathrm{~mm} \times 76.1 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ fiberglass epoxy printed circuit board
Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.
Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

[^0] Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at $\mathrm{Ta}=25^{\circ} \mathrm{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Operating supply voltage range | $\mathrm{V}_{\mathrm{CC}}$ op1 | Recommended supply voltage range | 7 to 34 | V |
|  | $\mathrm{V}_{\mathrm{CC}}$ op2 | Boot guarantee supply voltage range | 6 to 34 | V |
| Hall input common phase input voltage range | VICM |  | 0.3 to VRGL-2.0 | V |
| SSW pin input voltage range | SSW |  | 1.0 to 3.0 | V |
| Input PWM frequency range | PWMF |  | 20 to 50 | kHz |

Electrical Characteristics at $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=24 \mathrm{~V}$

| Parameter | Symbol | Conditions | Ratings |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | min | typ | max |  |
| Circuit consumption current | ${ }^{\text {ICC }}$ | Active |  | 2.2 | 3.5 | mA |
|  | ${ }^{\text {I CCO }}$ | Stand-by |  | 1.7 | 2.7 | mA |
| RGL pin output voltage | VRGL |  | 4.7 | 5.0 | 5.3 | V |
| RGH pin output voltage | VRGH |  | $\mathrm{V}_{\mathrm{CC}}-4.3$ | $\mathrm{V}_{\mathrm{CC}}-4.8$ | $\mathrm{V}_{\text {CC }}-5.3$ | V |
| HB pin output voltage | VHB | $1 \mathrm{HB}=5 \mathrm{~mA}$ | 1.16 | 1.25 | 1.28 | V |
| Output ON resistance | Ron | $\mathrm{I}_{\mathrm{O}}=0.3 \mathrm{~A}$, upper and lower ON resistance |  | 1.4 | 2.0 | $\Omega$ |
| Hall input bias current | IHIN |  |  |  | 1.0 | $\mu \mathrm{A}$ |
| Current limiter | VRF |  | 200 | 225 | 250 | mV |
| PWM pin input Low level | VPWML |  | 0 |  | 1.0 | V |
| PWM pin input High level | VPWMH |  | 2.5 |  | VRGL | V |
| PWM input minimum pulse width | TPWM |  |  | 2 |  | $\mu \mathrm{s}$ |
| RD/FG output pin Low voltage | VRD/FG | ${ }^{1} \mathrm{RD} / \mathrm{FG}=3 \mathrm{~mA}$ |  | 0.22 | 0.3 | V |
| FG output leakage current | IRDL/FGL | $\mathrm{V}_{\mathrm{RD} / \mathrm{FG}}=24 \mathrm{~V}$ |  |  | 10 | $\mu \mathrm{A}$ |
| FG comparator hysteresis width | $\triangle \mathrm{VHYS}$ | including offset | $\pm 5$ | $\pm 12$ | $\pm 18$ | mV |
| Output ON time in Lock-detection | TACT |  | 0.74 | 0.95 | 1.16 | sec |
| Output OFF time in Lock-detection | TDET |  | 7.0 | 9.0 | 11.0 | sec |
| Output ON/OFF ratio in Lock-detection | TRTO | TRTO=TDET/TACT | 7.5 | 9.0 | 11.0 |  |
| Thermal shutdown operating temperature | TSD | * Design guarantee |  | 180 |  | ${ }^{\circ} \mathrm{C}$ |
| Thermal shutdown hysteresis width | $\Delta T S D$ | * Design guarantee |  | 40 |  | ${ }^{\circ} \mathrm{C}$ |

* Design guarantee: Signifies target value in design. These parameters are not tested in an independent IC.

Truth table

| Operating state | IN1 | IN2 | PWM | OUT1 | OUT2 | FG | RD |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Rotation - drive mode | H | L | H | H | L | L | L |
|  | L | H |  | L | H | OFF | L |
| Rotation - regeneration mode | H | L | L | L | L | L | L |
|  | L | H |  | L | L | OFF | L |
| Stand-by mode | - | - | L | L | OFF | OFF | L |
| Lock protector | H | L | - | OFF | L | L | OFF |
|  | L | H |  | L | OFF | OFF | OFF |

## Package Dimensions

unit: mm (typ)
3178B



## Pin Assignment



## Block Diagram



## PIN function

*On circuit bord, $\uparrow$ means $\mathrm{V}_{\mathrm{CC}}$, $\uparrow$ means RGL.

\begin{tabular}{|c|c|c|c|}
\hline NO. \& Pin name \& Function \& Equivalent circuit \\
\hline 1 \& OUT1 \& Output pin for motor driver \&  \\
\hline 2 \& NC \& No connect pin \& \\
\hline 3 \& NC \& No connect pin \& \\
\hline 4 \& \(\mathrm{V}_{\mathrm{CC}}\) \& Power supply pin \& \\
\hline 5 \& RGH \& Regulator voltage output pin for the upper output Tr driver \&  \\
\hline 6 \& PWM \& \begin{tabular}{l}
Input pin for PWM control \\
* OPEN: pull up to High \\
* When input is High \(\rightarrow\) output is High \\
When input is Low \(\rightarrow\) output is Low
\end{tabular} \&  \\
\hline 7

8 \& \begin{tabular}{c}
FG <br>
<br>
<br>
\hline$R D$

 \& 

FG (rotation detection) pulse output pin <br>
RD (lock detection) signal output pin <br>

* During rotation $\rightarrow$ output is Low <br>
During lock $\rightarrow$ output is High
\end{tabular} \&  <br>

\hline 9

11 \& IN1

IN2 \& Hall input + pin
Hall input - pin \&  <br>
\hline 10 \& HB \& Hall bias output pin \&  <br>
\hline
\end{tabular}

Continued on next page.

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| NO. | Pin name | Function | Equivalent circuit |
| :---: | :---: | :---: | :---: |
| 12 | RGL | Regulator voltage output pin for internal circuit and lower output Tr driver |  |
| 13 | SSW | Voltage input pin for control between soft switches <br> * OPEN: pin voltage is 2 V <br> * Soft switch zone is changed by connecting a resistance to RGL or GND to adjust pin voltage. |  |
| 14 | GND | Ground pin |  |
| 15 | RF | Resistive connection pin for current limiter |  |

## Sample Application Circuit


*1 When diode Di is used to prevent destruction of IC from reverse connection, make sure to implement capacitor Cr to secure regenerative current route.
*2 If kickback at a phase change is greater, insert zener diode between GND and $V_{C C}$ or implement the larger capacitor between GND and $V_{\text {CC }}$ mentioned in *1
*3 Make sure to implement enough capacitance $0.1 \mu \mathrm{~F}$ or greater between RGH pin and $\mathrm{V}_{\mathrm{CC}}$ pin for stable performance.
*4 Make sure to implement enough capacitance $0.1 \mu \mathrm{~F}$ or greater between RGL pin and GND pin for stable performance.
*5 FG pin and RD pin are open drain output. Keep the pins open when unused
*6 The current limiter is activated when the current detection resistor voltage exceeds 225 mV between RF and GND Where $R f=0.5 \Omega$, current limiter is activated at $I_{O}=450 \mathrm{~mA}$. Setting is made using $R f$ resistance.
*7 Hall element outputs stable hall signal with good temperature characteristic when it is biased with constant voltage from HB pin. If you wish to alleviate heating of IC, do not use HB pin. When you do not use this Pin (Pin HB), pull down with resistor of around $10 \mathrm{k} \Omega$ (recommended)

## Adjustment of a direction between soft switches



LV8860V realizes high efficiency and low noise by controlling reactive power using soft switch before and after phase switch by variable PWM-duty.
The width of soft switch before and after switching is controlled by SSW pin voltage. Therefore, it is adjustable by connecting an external resistance to SSW. Adjustment voltage range is between 1 V and 3 V .

* Without adjustment (SSW is open * this is a reference width of soft switch)
$\ldots$ with IC's internal resistance: VSSW $=5 \times 60 \mathrm{k} /(90 \mathrm{k}+60 \mathrm{k})=2 \mathrm{~V}$
* To widen width of soft switch (connect Rw (resistance) between RGL and SSW.)
$\ldots \mathrm{VSSW}=5 \times 60 \mathrm{k} /(60 \mathrm{k}+1 /(1 / \mathrm{Rw}+1 / 90 \mathrm{k}))$
ex.) Connect $\mathrm{Rw}=75 \mathrm{k} \Omega$
$\mathrm{VSSW}=5 \times 60 \mathrm{k} /(60 \mathrm{k}+1 /(1 / 75 \mathrm{k}+1 / 90 \mathrm{k}))=2.97 \mathrm{~V}$
* To narrow soft switch width (connect Rn (resistance) between SSW and GND.)

$$
\begin{aligned}
& \ldots V S S W=5 \times((1 /(1 / \mathrm{Rn}+1 / 60 \mathrm{k})) /(90 \mathrm{k}+1 /(1 / \mathrm{Rn}+1 / 60 \mathrm{k}))) \\
& \text { ex. }) \text { Connect } \operatorname{Rn}=39 \mathrm{k} \Omega \\
& \quad \operatorname{VSSW}=5 \times((1 /(1 / 39 \mathrm{k}+1 / 60 \mathrm{k})) /(90 \mathrm{k}+1 /(1 / 39 \mathrm{k}+1 / 60 \mathrm{k})))=1.04 \mathrm{~V}
\end{aligned}
$$

## LV8860V

## Setting value of input signal amplitude

The width of soft switch in LV8860V is controlled by input signal, IN1/IN2. The difference of input voltage ( VINp-p ) that creates width of soft switch is adjustable by SSW voltage (VSSW) of an external pin. The range of SSW input voltage is between 1 V and 3 V .

Difference of input signal amplitude in VSSW range:

- When VSSW $=1 \mathrm{~V}(\mathrm{~min}), \mathrm{V}_{\text {INp}}-\mathrm{p}=30 \mathrm{mV} \rightarrow$ make sure to input Hall signal with amplitude difference greater than 30 mV .
- When VSSW $=2 \mathrm{~V}$ (open), $\mathrm{V}_{\text {INp-p }}=90 \mathrm{mV} \rightarrow$ make sure to input Hall signal with amplitude difference greater than 90 mV .
- When VSSW $=3 \mathrm{~V}(\max ), V_{\text {INp }}-\mathrm{p}=150 \mathrm{mV} \rightarrow$ make sure to input Hall signal with amplitude difference greater than 150 mV .
* When input signal amplitude is greater than $\mathrm{V}_{\text {INp-p }}$ (as shown in Fig. A below).

Width of soft switch is defined as shown in Fig. A

* When input signal amplitude is less than $\mathrm{V}_{\text {IN }} \mathrm{p}-\mathrm{p}$ (as shown in Fig. B below).

Since input signal is within the range of $V_{I N p}$-p in all rotations, the entire zone is the soft switch zone. Consequently, IC does not operate properly.

For such reason, make sure to input Hall signal with enough amplitude difference to SSW setting value so that IC operates properly.


Fig.A


Between
Soft Switches

Fig.B

## Description of operation

- PWM speed control waveform

- Lock protection operation waveform

- Stand-by mode operation waveform


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[^0]:    Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating

