

-5 V Differential ECL to TTL Translator

MC10ELT25, MC100ELT25



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Description

The MC10ELT/100ELT25 is a differential ECL to TTL translator. Because ECL levels are used, a +5 V, -5.2 V (or -4.5 V) and ground are required. The small outline 8-lead package and the single gate of the ELT25 makes it ideal for those applications where space, performance and low power are at a premium.

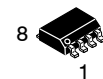
The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

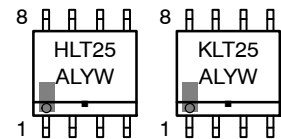
Features

- 2.6 ns Typical Propagation Delay
- 100 MHz F_{MAX} CLK
- 24 mA TTL Outputs
- Flow Through Pinouts
- Operating Range: $V_{CC} = 4.5$ V to 5.5 V with $GND = 0$ V;
 $V_{EE} = -4.2$ V to -5.7 V with $GND = 0$ V
- Internal Input 50 k Ω Pulldown Resistors
- Q Output will default HIGH with inputs open or < 1.3 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

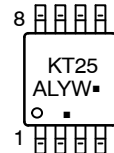
MARKING DIAGRAMS*



SOIC-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
MC10ELT25DG	SOIC-8 (Pb-Free)	98 Units / Tube
MC10ELT25DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT25DG	SOIC-8 (Pb-Free)	98 Units / Tube
MC100ELT25DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT25DTG	TSSOP-8 (Pb-Free)	100 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MC10ELT25, MC100ELT25

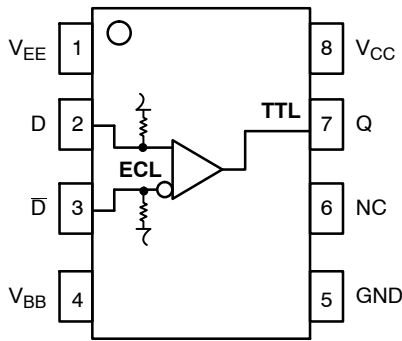


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Function
D, \bar{D}	ECL Differential Inputs
Q	TTL Output
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground
NC	No Connect

Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 k Ω
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model	> 1 kV > 400 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
SOIC-8 TSSOP-8	Level 1 Level 3
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	38 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V	$V_{EE} = -5.0$ V	7	V
V_{EE}	Negative Power Supply	GND = 0 V	$V_{CC} = +5.0$ V	-8	V
V_{IN}	Input Voltage	GND = 0 V		0 to V_{EE}	V
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			-40 to +85	$^{\circ}$ C
T_{stg}	Storage Temperature Range			-65 to +150	$^{\circ}$ C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 SOIC-8	190 130	$^{\circ}$ C/W $^{\circ}$ C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44	$^{\circ}$ C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	$^{\circ}$ C/W $^{\circ}$ C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 $\pm 5\%$	$^{\circ}$ C/W
T_{sol}	Wave Solder	Pb-Free	<2 to 3 sec @ 260 $^{\circ}$ C	265	$^{\circ}$ C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

MC10ELT25, MC100ELT25

Table 4. 10ELT SERIES NECL INPUT DC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$; $V_{EE} = -5.0\text{ V}$; $GND = 0\text{ V}$ (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 4)	-1230		-890	-1130		-810	-1060		-720	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Note 4)	-1950		-1500	-1950		-1480	-1950		-1445	mV
V_{BB}	Output Voltage Reference	-1.43		-1.30	-1.35		-1.25	-1.31		-1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Notes 4 and 5)	-2.8		0.0	-2.8		0.0	-2.8		0.0	V
I_{IH}	Input HIGH Current			255			175			175	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

3. Input parameters vary 1:1 with GND. V_{EE} can vary +0.06 V to -0.5 V.
4. TTL output $R_L = 500\ \Omega$ to GND
5. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with GND.

Table 5. 100ELT SERIES NECL INPUT DC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$; $V_{EE} = -5.0\text{ V}$; $GND = 0\text{ V}$ (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 7)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Note 7)	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{BB}	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Notes 7 and 8)	-2.8		0.0	-2.8		0.0	-2.8		0.0	V
I_{IH}	Input HIGH Current			255			175			175	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

6. Input parameters vary 1:1 with GND. V_{EE} can vary +0.8 V to -0.5 V.
7. TTL output $R_L = 500\ \Omega$ to GND
8. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with GND.

Table 6. TTL OUTPUT DC CHARACTERISTICS $V_{CC} = 4.5\text{ V to }5.5\text{ V}$; $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.0\text{ mA}$	2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 24\text{ mA}$			0.5	V
I_{CCH}	Power Supply Current			11	16	mA
I_{CCL}	Power Supply Current			13	18	mA
I_{EE}	Negative Power Supply Current			15	21	mA
I_{OS}	Output Short Circuit Current		-150		-60	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

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Table 7. AC CHARACTERISTICS $V_{CC}= 5.0\text{ V}$; $V_{EE}= -5.0\text{ V}$; $GND= 0\text{ V}$ (Note 9 and Note 10)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{\max}	Maximum Toggle Frequency					100					MHz
t_{PLH}	Propagation Delay @ 1.5 V	1.7		3.6	1.7		3.6	1.7		3.6	ns
t_{PHL}	Propagation Delay @ 1.5 V	2.6		4.1	2.6		4.1	2.6		4.1	ns
t_{JITTER}	Random Clock Jitter (RMS)					35					ps
t_r t_f	Output Rise/Fall Times QTTL 10% – 90%					1.9 2.3					ns
V_{PP}	Input Swing (Note 11)	200		1000	200		1000	200		1000	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

9. V_{CC} can vary $\pm 0.25\text{ V}$.

V_{EE} can vary +0.06 V to -0.5 V for 10ELT; V_{EE} can vary +0.8 V to -0.5 V for 100ELT.

10. $R_L = 500\ \Omega$ to GND and $C_L = 20\text{ pF}$ to GND. Refer to Figure 2.

11. $V_{PP}(\min)$ is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40 .

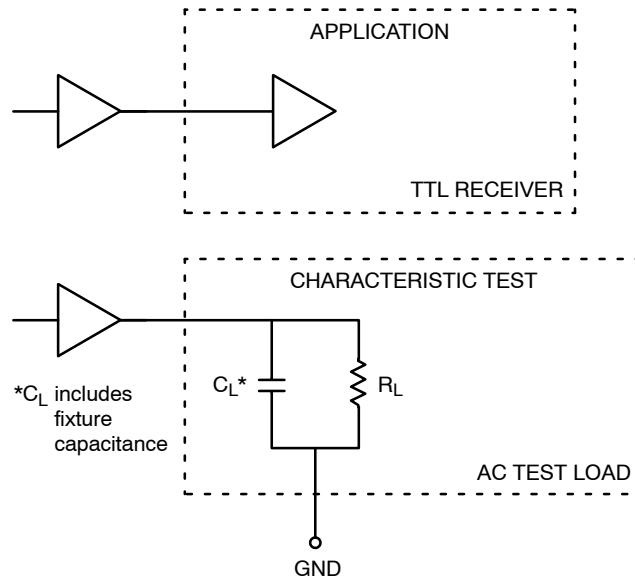


Figure 2. TTL Output Loading Used for Device Evaluation

Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

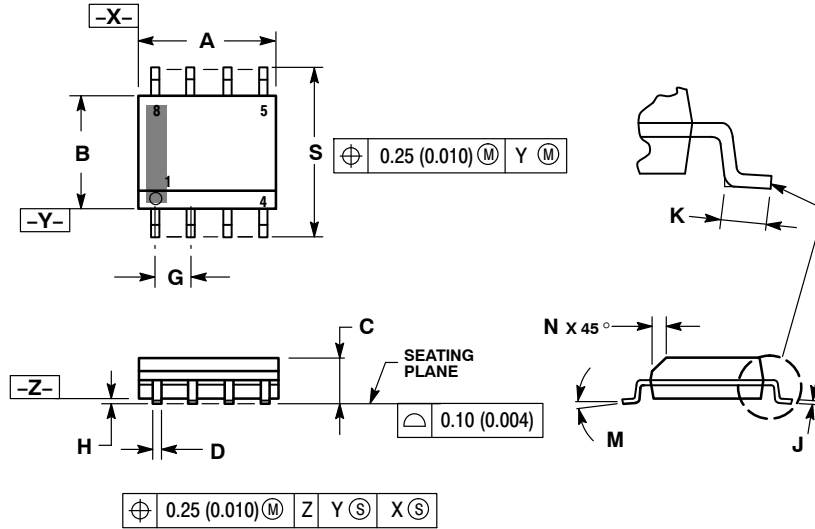
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SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

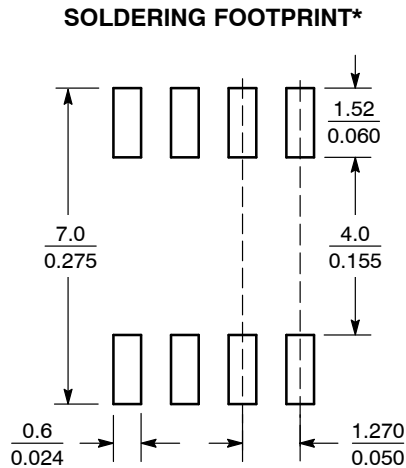
DATE 16 FEB 2011



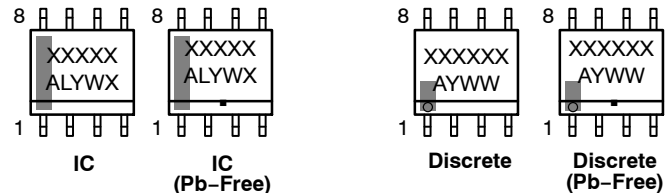
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*



SCALE 6:1 (mm/inches)



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|--|---|---|---|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

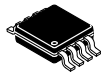
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

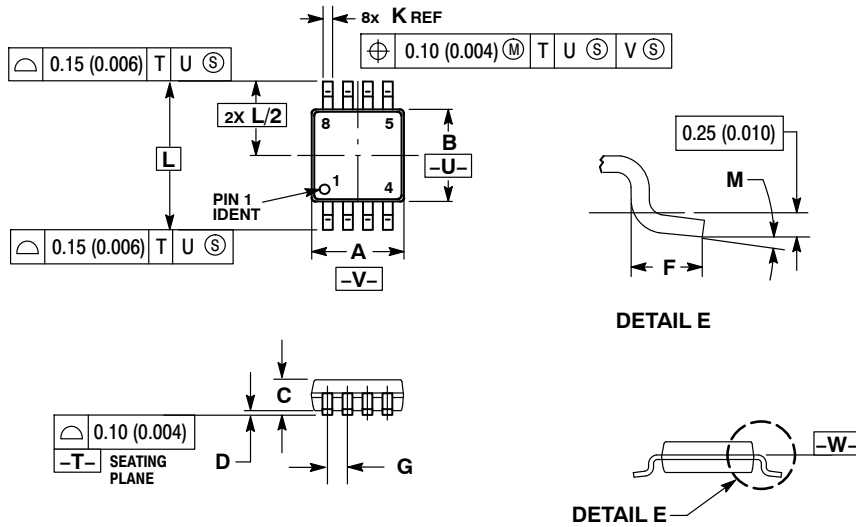
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SCALE 2:1

TSSOP 8 CASE 948R-02 ISSUE A

DATE 04/07/2000



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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