### 3.3 V/5 V ECL Differential Receiver/Driver with High Gain and Enable Output

## MC100EP16VC

## Description

The EP16VC is a differential receiver/driver. The device is functionally equivalent to the EP16 and LVEP16 devices but with high gain and enable output.

The EP16VC provides an $\overline{E N}$ input which is synchronized with the data input (D) signal in a way that provides glitchless gating of the QHG and $\overline{\mathrm{QHG}}$ outputs.

When the $\overline{\mathrm{EN}}$ signal is LOW, the input is passed to the outputs and the data output equals the data input. When the data input is HIGH and $\overline{\mathrm{EN}}$ goes HIGH, it will force the $\mathrm{Q}_{\mathrm{HG}}$ LOW and the $\overline{\mathrm{Q}_{\mathrm{HG}}}$ HIGH on the next negative transition of the data input. If the data input is LOW when the EN goes HIGH, the next data transition to a HIGH is ignored and $\mathrm{Q}_{\mathrm{HG}}$ remains LOW and $\overline{\mathrm{Q}_{\mathrm{HG}}}$ remains HIGH. The next positive transition of the data input is not passed on to the data outputs under these conditions. The $\mathrm{Q}_{\mathrm{HG}}$ and $\overline{\mathrm{Q}_{\mathrm{HG}}}$ outputs remain in their disabled state as long as the EN input is held HIGH. The EN input has no influence on the $\overline{\mathrm{Q}}$ output and the data input is passed on (inverted) to this output whether $\overline{\text { EN }}$ is HIGH or LOW. This configuration is ideal for crystal oscillator applications where the oscillator can be free running and gated on and off synchronously without adding extra counts to the output.
The $\mathrm{V}_{\mathrm{BB}} / \overline{\mathrm{D}}$ pin is internally dedicated and available for differential interconnect. $\mathrm{V}_{\mathrm{BB}} / \overline{\mathrm{D}}$ may rebias AC coupled inputs. When used, decouple $\mathrm{V}_{\mathrm{BB}} / \overline{\mathrm{D}}$ and $\mathrm{V}_{\mathrm{CC}}$ via a $0.01 \mu \mathrm{~F}$ capacitor and limit current sourcing or sinking to 1.5 mA . When not used, $\mathrm{V}_{\mathrm{BB}} / \overline{\mathrm{D}}$ should be left open.

The 100 Series contains temperature compensation.

## Features

- 310 ps Typical Prop Delay $\overline{\mathrm{Q}}$, 380 ps Typical Prop Delay QHG, $\overline{\mathrm{QHG}}$
- Gain > 200
- Maximum Frequency $>3 \mathrm{GHz}$ Typical
- PECL Mode Operating Range:
- $\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}$ to 5.5 V with $\mathrm{V}_{\mathrm{EE}}=0 \mathrm{~V}$
- NECL Mode Operating Range:
- $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}$ with $\mathrm{V}_{\mathrm{EE}}=-3.0 \mathrm{~V}$ to -5.5 V
- Open Input Default State
- $\mathrm{Q}_{\mathrm{HG}}$ Output Will Default LOW with D Inputs Open or at $\mathrm{V}_{\mathrm{EE}}$
- $\mathrm{V}_{\mathrm{BB}}$ Output
- These Devices are $\mathrm{Pb}-$ Free, Halogen Free and are RoHS Compliant

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ORDERING INFORMATION

| Device | Package | Shipping $^{\dagger}$ |
| :---: | :---: | :---: |
| MC100EP16VCDTR2G | TSSOP-8 | $2500 /$ |
|  | (Pb-Free) | Tape \& Reel |

$\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MC100EP16VC



Table 1. PIN DESCRIPTION

| Pin | Function |
| :---: | :--- |
| $\mathrm{D}^{\star}$ | ECL Data Input |
| $\overline{\mathrm{Q}}$ | ECL Data Output |
| $\mathrm{Q}_{\mathrm{HG}}, \mathrm{Q}_{\mathrm{HG}}$ | ECL High Gain Data Outputs |
| $\mathrm{EN}^{\star}$ | ECL Enable Input |
| $\mathrm{V}_{\mathrm{BB}} / \mathrm{D}$ | Reference Voltage Output / ECL Data Input |
| $\mathrm{V}_{\mathrm{CC}}$ | Positive Supply |
| $\mathrm{V}_{\mathrm{EE}}$ | Negative Supply |

*Pins will default LOW when left open.

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 2. ATTRIBUTES

| Characteristics | Value |
| :---: | :---: |
| Internal Input Pulldown Resistor | $75 \mathrm{k} \Omega$ |
| Internal Input Pullup Resistor | N/A |
| ESD Protection Human Body Model Machine Model Charged Device Model | $\begin{gathered} >4 \mathrm{kV} \\ >200 \mathrm{~V} \\ >2 \mathrm{kV} \end{gathered}$ |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb-Free Pkg |
| TSSOP-8 | Level 3 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 167 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test |  |

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | PECL Mode Power Supply | $\mathrm{V}_{\mathrm{EE}}=0 \mathrm{~V}$ |  | 6 | V |
| $\mathrm{V}_{\mathrm{EE}}$ | NECL Mode Power Supply | $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}$ |  | -6 | V |
| $\mathrm{V}_{1}$ | PECL Mode Input Voltage NECL Mode Input Voltage | $\begin{aligned} & V_{E E}=0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{1} \leq \mathrm{V}_{\mathrm{CC}} \\ & \mathrm{~V}_{1} \geq \mathrm{V}_{\mathrm{EE}} \end{aligned}$ | $\begin{gathered} \hline 6 \\ -6 \end{gathered}$ | V |
| $\mathrm{I}_{\text {out }}$ | Output Current | Continuous Surge |  | $\begin{gathered} \hline 50 \\ 100 \end{gathered}$ | mA |
| $\mathrm{I}_{\text {BB }}$ | $\mathrm{V}_{\text {BB }}$ Sink/Source |  |  | $\pm 1.5$ | mA |
| $\mathrm{T}_{\text {A }}$ | Operating Temperature Range |  |  | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {stg }}$ | Storage Temperature Range |  |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| $\theta_{\mathrm{JA}}$ | Thermal Resistance (Junction-to-Ambient) | $\begin{aligned} & \hline 0 \text { lfpm } \\ & 500 \mathrm{lfpm} \end{aligned}$ |  | $\begin{aligned} & 185 \\ & 140 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\theta_{\text {Jc }}$ | Thermal Resistance (Junction-to-Case) | Standard Board |  | 41 to 44 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{T}_{\text {sol }}$ | Wave Solder (Pb-Free) |  |  | 265 | ${ }^{\circ} \mathrm{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board - 2S2P (2 signal, 2 power)

Table 4. 100EP DC CHARACTERISTICS, PECL (VCC=3.3V, $\mathrm{V}_{\mathrm{EE}}=0 \mathrm{~V}$ (Note 1))

| Symbol | Characteristic | $-40^{\circ} \mathrm{C}$ |  |  | $25^{\circ} \mathrm{C}$ |  |  | $85^{\circ} \mathrm{C}$ |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| $\mathrm{I}_{\text {EE }}$ | Power Supply Current | 27 | 37 | 47 | 32 | 42 | 52 | 34 | 44 | 54 | mA |
| $\mathrm{V}_{\mathrm{OH}}$ | Output HIGH Voltage (Note 2) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| $\mathrm{V}_{\text {OL }}$ | Output LOW Voltage (Note 2) | 1305 | 1400 | 1555 | 1305 | 1400 | 1555 | 1305 | 1400 | 1555 | mV |
| $\mathrm{V}_{\mathrm{IH}}$ | Input HIGH Voltage (Single-Ended) | 2075 |  | 2420 | 2075 |  | 2420 | 2075 |  | 2420 | mV |
| $\mathrm{V}_{\mathrm{IL}}$ | Input LOW Voltage (Single-Ended) | 1355 |  | 1675 | 1355 |  | 1675 | 1355 |  | 1675 | mV |
| $\mathrm{V}_{\mathrm{BB}}$ | Output Voltage Reference | 1775 | 1890 | 2045 | 1775 | 1890 | 2045 | 1775 | 1890 | 2045 | mV |
| $\mathrm{V}_{\text {IHCMR }}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.0 |  | 3.3 | 2.0 |  | 3.3 | 2.0 |  | 3.3 | V |
| IIH | Input HIGH Current |  |  | 150 |  |  | 150 |  |  | 150 | $\mu \mathrm{A}$ |
| IIL | Input LOW Current D | 0.5 |  |  | 0.5 |  |  | 0.5 |  |  | $\mu \mathrm{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary $1: 1$ with $\mathrm{V}_{\mathrm{CC}}$. $\mathrm{V}_{\mathrm{EE}}$ can vary +0.3 V to -2.2 V .
2. All loading with $50 \Omega$ to $\mathrm{V}_{\mathrm{CC}}-2.0 \mathrm{~V}$.
3. $\mathrm{V}_{\text {IHCMR }}$ min varies $1: 1$ with $\mathrm{V}_{\mathrm{EE}}, \mathrm{V}_{\text {IHCMR }}$ max varies $1: 1$ with $\mathrm{V}_{\mathrm{CC}}$. The $\mathrm{V}_{\text {IHCMR }}$ range is referenced to the most positive side of the differential input signal.

Table 5. 100EP DC CHARACTERISTICS, PECL $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}\right.$ (Note 1))

|  | Characteristic | $-40^{\circ} \mathrm{C}$ |  |  | $25^{\circ} \mathrm{C}$ |  |  | $85^{\circ} \mathrm{C}$ |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| $\mathrm{I}_{\text {EE }}$ | Power Supply Current | 27 | 37 | 47 | 32 | 42 | 52 | 34 | 44 | 54 | mA |
| $\mathrm{V}_{\mathrm{OH}}$ | Output HIGH Voltage (Note 2) | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | mV |
| $\mathrm{V}_{\text {OL }}$ | Output LOW Voltage (Note 2) | 3005 | 3100 | 3255 | 3005 | 3100 | 3255 | 3005 | 3100 | 3255 | mV |
| $\mathrm{V}_{\mathrm{IH}}$ | Input HIGH Voltage (Single-Ended) | 3775 |  | 4120 | 3775 |  | 4120 | 3775 |  | 4120 | mV |
| $\mathrm{V}_{\text {IL }}$ | Input LOW Voltage (Single-Ended) | 3055 |  | 3375 | 3055 |  | 3375 | 3055 |  | 3375 | mV |
| $\mathrm{V}_{\text {BB }}$ | Output Voltage Reference | 3475 | 3490 | 3705 | 3475 | 3490 | 3705 | 3475 | 3490 | 3705 | mV |
| $\mathrm{V}_{\text {IHCMR }}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.0 |  | 5.0 | 2.0 |  | 5.0 | 2.0 |  | 5.0 | V |
| $\mathrm{IIH}^{\text {H }}$ | Input HIGH Current |  |  | 150 |  |  | 150 |  |  | 150 | $\mu \mathrm{A}$ |
| IIL | Input LOW Current D | 0.5 |  |  | 0.5 |  |  | 0.5 |  |  | $\mu \mathrm{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary $1: 1$ with $\mathrm{V}_{\mathrm{CC}} . \mathrm{V}_{\mathrm{EE}}$ can vary +2.0 V to -0.5 V .
2. All loading with $50 \Omega$ to $\mathrm{V}_{\mathrm{CC}}-2.0 \mathrm{~V}$.
3. $\mathrm{V}_{\mathrm{IHCMR}}$ min varies $1: 1$ with $\mathrm{V}_{\mathrm{EE}}, \mathrm{V}_{\mathrm{IHCMR}}$ max varies $1: 1$ with $\mathrm{V}_{\mathrm{CC}}$. The $\mathrm{V}_{\mathrm{IHCMR}}$ range is referenced to the most positive side of the differential input signal.

Table 6. 100EP DC CHARACTERISTICS, NECL ( $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{EE}}=-5.5 \mathrm{~V}$ to -3.0 V (Note 1))

|  | Characteristic | $-40^{\circ} \mathrm{C}$ |  |  | $25^{\circ} \mathrm{C}$ |  |  | $85^{\circ} \mathrm{C}$ |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| $\mathrm{I}_{\text {EE }}$ | Power Supply Current | 27 | 37 | 47 | 32 | 42 | 52 | 34 | 44 | 54 | mA |
| $\mathrm{V}_{\mathrm{OH}}$ | Output HIGH Voltage (Note 2) | -1145 | -1020 | -895 | -1145 | -1020 | -895 | -1145 | -1020 | -895 | mV |
| $\mathrm{V}_{\text {OL }}$ | Output LOW Voltage (Note 2) | -1995 | -1900 | -1745 | -1995 | -1900 | -1745 | -1995 | -1900 | -1745 | mV |
| $\mathrm{V}_{\mathrm{IH}}$ | Input HIGH Voltage (Single-Ended) | -1225 |  | -880 | -1225 |  | -880 | -1225 |  | -880 | mV |
| $\mathrm{V}_{\text {IL }}$ | Input LOW Voltage (Single-Ended) | -1945 |  | -1625 | -1945 |  | -1625 | -1945 |  | -1625 | mV |
| $\mathrm{V}_{\mathrm{BB}}$ | Output Voltage Reference | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | mV |
| $\mathrm{V}_{\text {IHCMR }}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | $\mathrm{V}_{\mathrm{EE}}+2.0$ |  | 0.0 | $\mathrm{V}_{\mathrm{EE}}+2.0$ |  | 0.0 | $\mathrm{V}_{\mathrm{EE}}+2.0$ |  | 0.0 | V |
| IIH | Input HIGH Current |  |  | 150 |  |  | 150 |  |  | 150 | $\mu \mathrm{A}$ |
| 1 IL | Input LOW Current | 0.5 |  |  | 0.5 |  |  | 0.5 |  |  | $\mu \mathrm{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary $1: 1$ with $\mathrm{V}_{\mathrm{CC}}$.
2. All loading with $50 \Omega$ to $\mathrm{V}_{\mathrm{CC}}-2.0 \mathrm{~V}$.
3. $\mathrm{V}_{\text {IHCMR }}$ min varies $1: 1$ with $\mathrm{V}_{\text {EE }}, \mathrm{V}_{\text {IHCMR }}$ max varies $1: 1$ with $\mathrm{V}_{\mathrm{CC}}$. The $\mathrm{V}_{\text {IHCMR }}$ range is referenced to the most positive side of the differential input signal.

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Table 7. AC CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{EE}}=-3.0 \mathrm{~V}\right.$ to -5.5 V or $\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}$ to $5.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{EE}}=0 \mathrm{~V}$ (Note 1))

| Symbol | Characteristic | $-40^{\circ} \mathrm{C}$ |  |  | $25^{\circ} \mathrm{C}$ |  |  | $85^{\circ} \mathrm{C}$ |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| $\mathrm{f}_{\text {max }}$ | Maximum Frequency (Figure 2) |  | > 3 |  |  | >3 |  |  | > 3 |  | GHz |
| $\begin{aligned} & \text { tpLH, } \\ & t_{\text {tpHI }} \end{aligned}$ | Propagation Delay (Differential) $\bar{Q}$ (Differential) QHG, QHG (Single-Ended) $\bar{Q}$ (Single-Ended) QHG, QHG | $\begin{array}{r} 200 \\ 250 \\ 250 \\ 300 \\ \hline \end{array}$ | $\begin{aligned} & 280 \\ & 360 \\ & 330 \\ & 410 \\ & \hline \end{aligned}$ | $\begin{aligned} & 350 \\ & 450 \\ & 400 \\ & 500 \\ & \hline \end{aligned}$ | $\begin{aligned} & 250 \\ & 300 \\ & 300 \\ & 350 \end{aligned}$ | $\begin{array}{r} 310 \\ 380 \\ 360 \\ 430 \\ \hline \end{array}$ | $\begin{array}{r} 400 \\ 500 \\ 450 \\ 550 \\ \hline \end{array}$ | $\begin{aligned} & 275 \\ & 325 \\ & 325 \\ & 375 \\ & \hline \end{aligned}$ | $\begin{aligned} & 340 \\ & 430 \\ & 390 \\ & 480 \\ & \hline \end{aligned}$ | $\begin{array}{r} 425 \\ 525 \\ 475 \\ 575 \\ \hline \end{array}$ | ps |
| ts | $\begin{gathered} \text { Setup Time } \\ E N=L \text { to } D \\ E N=H \text { to } D \end{gathered}$ | $\begin{gathered} \hline 50 \\ 100 \end{gathered}$ | $\begin{aligned} & 15 \\ & 60 \end{aligned}$ |  | $\begin{gathered} 50 \\ 100 \end{gathered}$ | $\begin{gathered} 5 \\ 40 \end{gathered}$ |  | $\begin{gathered} \hline 50 \\ 100 \end{gathered}$ | $\begin{aligned} & 18 \\ & 10 \end{aligned}$ |  | ps |
| $\mathrm{t}_{\mathrm{H}}$ | Hold Time $E N=L$ to $D$ $E N=H$ to $D$ | $\begin{gathered} 100 \\ 50 \end{gathered}$ | $\begin{aligned} & 50 \\ & 15 \end{aligned}$ |  | $\begin{gathered} 100 \\ 50 \end{gathered}$ | $\begin{aligned} & 40 \\ & 20 \end{aligned}$ |  | $\begin{aligned} & 100 \\ & 50 \end{aligned}$ | $\begin{gathered} 5 \\ 20 \end{gathered}$ |  | ps |
| ${ }^{\text {tskew }}$ | Duty Cycle Skew (Note 2) |  | 5.0 | 20 |  | 5.0 | 20 |  | 5.0 | 20 | ps |
| $\mathrm{t}_{\text {JITTER }}$ | RMS Random Clock Jitter (Figure 2) |  | 0.2 | <1 |  | 0.2 | <1 |  | 0.2 | < 1 | ps |
| $\mathrm{V}_{\mathrm{PP}}$ | Input Voltage Swing HG <br> (Differential Configuration) Q | $\begin{gathered} 25 \\ 150 \end{gathered}$ | $\begin{aligned} & 800 \\ & 800 \end{aligned}$ | $\begin{aligned} & 1200 \\ & 1200 \end{aligned}$ | $\begin{gathered} 25 \\ 150 \end{gathered}$ | $\begin{aligned} & 800 \\ & 800 \end{aligned}$ | $\begin{aligned} & 1200 \\ & 1200 \end{aligned}$ | $\begin{gathered} \hline 25 \\ 150 \end{gathered}$ | $\begin{aligned} & 800 \\ & 800 \end{aligned}$ | $\begin{aligned} & 1200 \\ & 1200 \end{aligned}$ | mV |
| $\begin{aligned} & \mathrm{t}_{\mathrm{r}} \\ & \mathrm{t}_{\mathrm{f}} \end{aligned}$ | Output Rise/Fall Times <br> Q <br> (20\%-80\%) QHG, QHG | $\begin{aligned} & 200 \\ & 70 \end{aligned}$ | $\begin{aligned} & 300 \\ & 130 \end{aligned}$ | $\begin{aligned} & 400 \\ & 220 \end{aligned}$ | $\begin{gathered} 250 \\ 80 \end{gathered}$ | $\begin{aligned} & 350 \\ & 150 \end{aligned}$ | $\begin{aligned} & 450 \\ & 240 \end{aligned}$ | $\begin{aligned} & 250 \\ & 100 \end{aligned}$ | $\begin{aligned} & 350 \\ & 170 \end{aligned}$ | $\begin{aligned} & 500 \\ & 270 \end{aligned}$ | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Measured using a 750 mV source, $50 \%$ duty cycle clock source. All loading with $50 \Omega$ to $\mathrm{V}_{\mathrm{cc}}-2.0 \mathrm{~V}$.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.


Figure 2. $\mathrm{F}_{\text {max }} / \mathrm{Jitter}$ for QHG, QHG Output

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Figure 3. $\mathbf{F}_{\text {max }} /$ Jitter for $\mathbf{Q}$ Output


Figure 4. Fmax $_{\text {ma }}$ Jitter for QHG, QHG Output

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Figure 5. $\mathbf{F}_{\text {max }} /$ Jitter for $\mathbf{Q}$ Output


Figure 6. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D - Termination of ECL Logic Devices.)

| Res | ference of Application Notes |
| :---: | :---: |
| AN1405/D | - ECL Clock Distribution Techniques |
| AN1406/D | - Designing with PECL (ECL at +5.0 V ) |
| AN1503/D | - ECLinPS ${ }^{\text {m }}$ I/O SPiCE Modeling Kit |
| AN1504/D | - Metastability and the ECLinPS Family |
| AN1568/D | - Interfacing Between LVDS and ECL |
| AN1672/D | The ECL Translator Guide |
| AND8001/D | - Odd Number Counters Design |
| AND8002/D | - Marking and Date Codes |
| AND8020/D | - Termination of ECL Logic Devices |
| AND8066/D | - Interfacing with ECLinPS |
| AND8090/D | - AC Characteristics of ECL Devices |

TSSOP 8

## CASE 948R-02

ISSUE A
DATE 04/07/2000

## SCALE 2:1


notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PROTRUSI
PER SIDE
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

|  | MILLIMETERS |  | INCHES |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |  |  |
| A | 2.90 | 3.10 | 0.114 | 0.122 |  |  |
| B | 2.90 | 3.10 | 0.114 | 0.122 |  |  |
| C | 0.80 | 1.10 | 0.031 | 0.043 |  |  |
| D | 0.05 | 0.15 | 0.002 | 0.006 |  |  |
| F | 0.40 | 0.70 | 0.016 | 0.028 |  |  |
| G | 0.65 BSC |  | 0.026 BSC |  |  |  |
| K | 0.25 |  | 0.40 | 0.010 |  | 0.016 |
| L | 4.90 BSC |  | 0.193 BSC |  |  |  |
| M | $0^{\circ}$ |  | $6^{\circ}$ | $0^{\circ}$ |  | $6^{\circ}$ |


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| ---: | :--- | :--- | :--- |
| DESCRIPTION: | TSSOP 8 | PAGE 1 OF 1 |

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