

MC100LVEL91

3.3 V Triple LVPECL Input to -3.3 V to -5.0 V ECL Output Translator

Description

The MC100LVEL91 is a triple LVPECL input to ECL output translator. The device receives low voltage differential PECL signals, determined by the V_{CC} supply level, and translates them to differential -3.3 V to -5.0 V ECL output signals.

To accomplish the level translation the LVEL91 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via 0.01 μ F capacitors.

Under open input conditions, the \bar{D} input will be biased at $V_{CC}/2$ and the D input will be pulled to GND. This condition will force the Q output to a low, ensuring stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

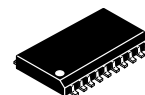
Features

- 620 ps Typical Propagation Delay
- The 100 Series Contains Temperature Compensation
- Operating Range: $V_{CC} = 3.8$ V to 3.0 V;
 $V_{EE} = -3.0$ V to -5.5 V; GND = 0 V
- Q Output will Default LOW with Inputs Open or at GND
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



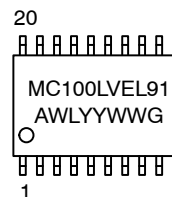
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SOIC-20 WB
DW SUFFIX
CASE 751D

MARKING DIAGRAM*



- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
MC100LVEL91DWG	SOIC-20 WB (Pb-Free)	38 Units/Tube
MC100LVEL91DWR2G	SOIC-20 WB (Pb-Free)	1000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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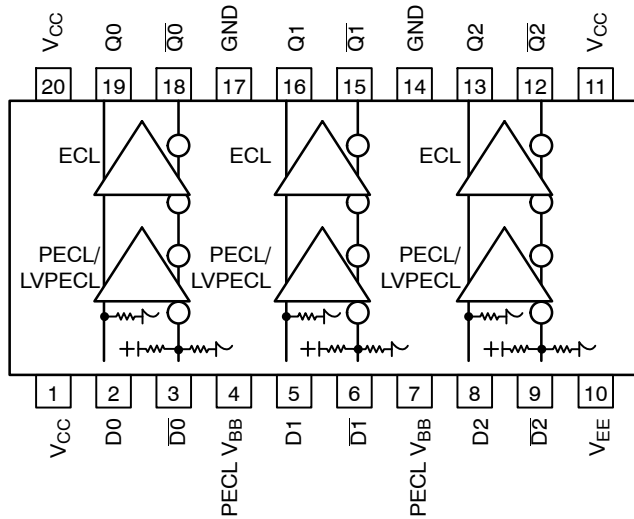


Figure 1. SO-20 Pinout (Top View) and Logic Diagram

* All V_{CC} pins are tied together on the die.

Warning: All V_{CC} , V_{EE} , and GND pins must be externally connected to Power Supply to guarantee proper operation.

Table 1. PIN DESCRIPTION

Pin	Function
D_n, \overline{D}_n	PECL/LVPECL Inputs
Q_n, \overline{Q}_n	ECL Outputs
PECL V_{BB}	PECL Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground

Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 k Ω
Internal Input Pullup Resistor	75 k Ω
ESD Protection	
Human Body Model	> 2 kV
Machine Model	> 100 V
Charged Device Model	> 2 kV
Moisture Sensitivity, (Note 1): Pb-Free	Level 3
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	282 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

MC100LEVEL91

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Power Supply	GND = 0 V		3.8	V
V _{EE}	NECL Power Supply	GND = 0 V		-6.0	V
V _I	PECL Input Voltage	GND = 0 V	V _I ≤ V _{CC}	3.8	V
I _{out}	Output Current	Continuous Surge		50 100	mA
I _{BB}	PECL V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-20 WB	90 60	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-20 WB	30 to 35	°C/W
T _{sol}	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. LVPECL INPUT DC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = -3.3 V to -5.0 V; GND = 0 V (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{CC}	V _{CC} Power Supply Current			11		6	11			11	mA
V _{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V _{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
LVPECL V _{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 2) V _{PP} < 500 mV V _{PP} ≥ 500 mV	1.0 1.2		2.9 2.9	0.9 1.1		2.9 2.9	0.9 1.1		2.9 2.9	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current D D̄	0.5 -600			0.5 -600			0.5 -600			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary +0.5 / -0.3 V.
2. V_{IHCMR} min varies 1:1 with GND. V_{IHCMR} max varies 1:1 with V_{CC}.

Table 5. NECL OUTPUT DC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = -3.3 V to -5.0 V; GND = 0 V (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	V _{EE} Power Supply Current			27		21	27			29	mA
V _{OH}	Output HIGH Voltage (Note 2)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V _{OL}	Output LOW Voltage (Note 2)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Output parameters vary 1:1 with GND. V_{CC} can vary +0.3 V / -0.5 V.
2. All loading with 50 Ω resistor to GND - 2.0 V.

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Table 6. AC CHARACTERISTICS ($V_{CC} = 3.3\text{ V}$; $V_{EE} = -3.0\text{ V}$ to -5.5 V ; $GND = 0\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{\max}	Maximum Toggle Frequency		600			600			600		MHz
T_{PLH}	Propagation Delay Differential Configuration	490	590	690	520	620	720	560	660	760	ps
t_{PHL}	D to Q Select-Ended	440	590	740	470	620	770	510	660	810	
t_{SKEW}	Skew Output-to-Output (Note 2) Part-to-Part (Differential Configuration) (Note 2) Duty Cycle (Differential Configuration) (Note 3)		40 25	100 200		40 25	100 200		40 25	100 200	ps
V_{PP}	Input Swing (Note 4)	200		1000	200		1000	200		1000	
t_r t_f	Output Rise/Fall Times Q (20% - 80%)	320	400	580	320	400	580	320	400	580	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- V_{CC} can vary $+0.5\text{ V} / -0.3\text{ V}$.
- Skews are valid across specified voltage range, part-to-part skew is for a given temperature.
- Duty cycle skew is the difference between a T_{PLH} and T_{PHL} propagation delay through a device.
- $V_{PP}(\min)$ is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40 .

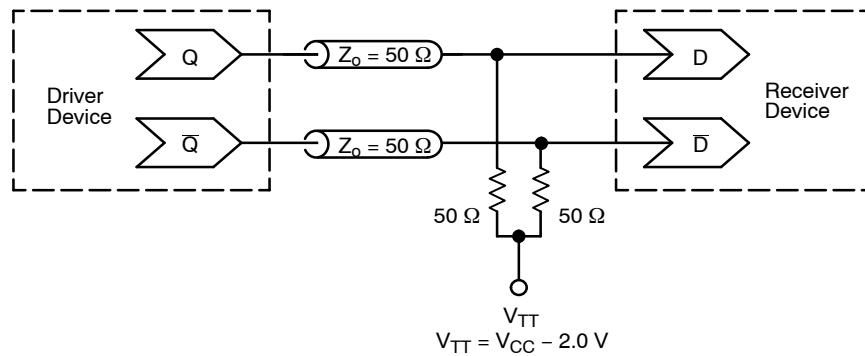


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

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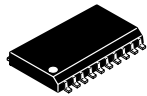
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1642/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

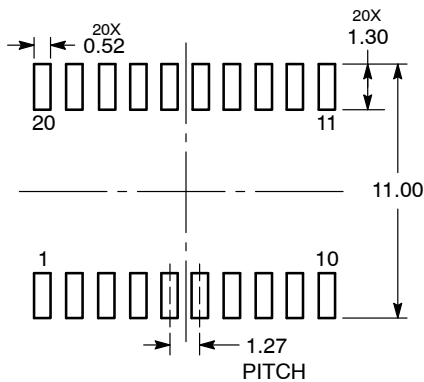


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

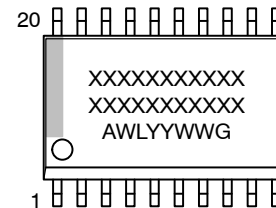
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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