MC34060A, MC33060A

Fixed Frequency, PWM, Voltage Mode Single Ended Controllers

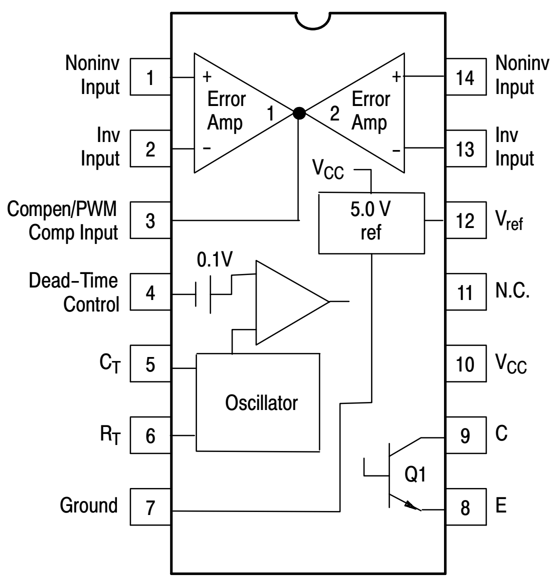
The MC34060A is a low cost fixed frequency, pulse width modulation control circuit designed primarily for single−ended SWITCHMODE™ power supply control.

The MC34060A is specified over the commercial operating temperature range of 0° to +70°C, and the MC33060A is specified over an automotive temperature range of −40° to +85°C.

Features

- Complete Pulse Width Modulation Control Circuitry
- On−Chip Oscillator with Master or Slave Operation
- On−Chip Error Amplifiers
- On−Chip 5.0 V Reference, 1.5% Accuracy
- Adjustable Dead−Time Control
- Uncommitted Output Transistor Rated to 200 mA Source or Sink
- Undervoltage Lockout
- These are Pb−Free and Halide−Free Devices

PIN CONNECTIONS



(Top View)

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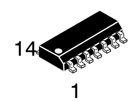
MARKING DIAGRAMS



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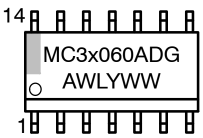
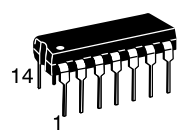
D SUFFIX
CASE 751A





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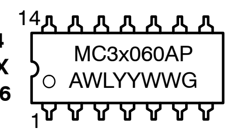


x	= 3 or 4
A	= Assembly Location
WL	= Wafer Lot
Y, YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	42	V
Collector Output Voltage	V_C	42	V
Collector Output Current (Note 3)	I_C	500	mA
Amplifier Input Voltage Range	V_{in}	−0.3 to +42	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	mW
Operating Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Ambient Temperature Range For MC34060A For MC33060A	T_A	 0 to +70 −40 to +85	°C
ESD Capability Machine Model Human Body Model		 200 2.0	 V kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Pins 1− 14: Human Body Model 2000 V per JEDEC Standard JESD22−A114E.
   Machine Model Method 200 V per JEDEC Standard JESD22−A115−A.
2. This device contains Latch−Up protection and exceeds ± 100 mA per JEDEC Standard JESD78.

THERMAL CHARACTERISTICS

Characteristics	Symbol	P Suffix Package	D Suffix Package	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	80	120	°C/W
Derating Ambient Temperature	T_A	45	45	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	–	30	40	V
Collector Output Current	I_C	–	–	200	mA
Amplifier Input Voltage	V_{in}	−0.3	–	V_{CC} −2	V
Current Into Feedback Terminal	I_{fb}	–	–	0.3	mA
Reference Output Current	I_{ref}	–	–	10	mA
Timing Resistor	R_T	1.8	47	500	kΩ
Timing Capacitor	C_T	0.00047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz
PWM Input Voltage (Pins 3 and 4)	–	−0.3	–	5.3	V

3. Maximum thermal limits must be observed.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

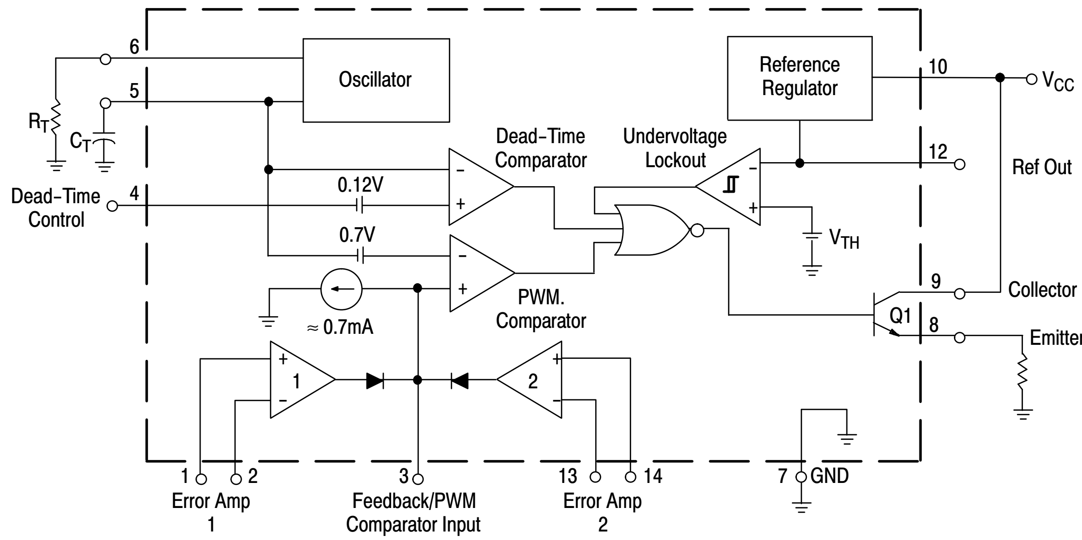
Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (I_O = 1.0 mA, T_A 25°C) T_A = T_{low} to T_{high} – MC34060A – MC33060A	V_{ref}	4.925 4.9 4.85	5.0 – –	5.075 5.1 5.1	V
Line Regulation (V_{CC} = 7.0 V to 40 V, I_O = 10 mA)	Reg_{line}	–	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	2.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	mA
OUTPUT SECTION					
Collector Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	–	2.0	100	μA
Emitter Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V, V_E = 0 V)	$I_{E(off)}$	–	–	–100	μA
Collector–Emitter Saturation Voltage (Note 4) Common–Emitter (V_E = 0 V, I_C = 200 mA) Emitter–Follower (V_C = 15 V, I_E = –200 mA)	$V_{sat(C)}$ $V_{sat(E)}$	– –	1.1 1.5	1.5 2.5	V
Output Voltage Rise Time (T_A = 25°C) Common–Emitter (See Figure 12) Emitter–Follower (See Figure 13)	t_r	 – –	 100 100	 200 200	ns
Output Voltage Fall Time (T_A = 25°C) Common–Emitter (See Figure 12) Emitter–Follower (See Figure 13)	t_r	 – –	 40 40	 100 100	ns
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O[Pin\ 3]}$ = 2.5 V)	V_{IO}	–	2.0	10	mV
Input Offset Current ($V_{C[Pin\ 3]}$ = 2.5 V)	I_{IO}	–	5.0	250	nA
Input Bias Current ($V_{O[Pin\ 3]}$ = 2.5 V)	I_{IB}	–	–0.1	–2.0	μA
Input Common Mode Voltage Range (V_{CC} = 40 V)	V_{ICR}	0 to V_{CC} –2.0	–	–	V
Inverting Input Voltage Range	$V_{IR(INV)}$	–0.3 to V_{CC}–2.0	–	–	V
Open–Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	–	dB
Unity–Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_c	–	600	–	kHz
Phase Margin at Unity–Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	–	65	–	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V, V_{in} = 0 V to 38 V))	CMRR	65	90	–	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	–	100	–	dB
Output Sink Current ($V_{O[Pin\ 3]}$ = 0.7 V)	I_O-	0.3	0.7	–	mA
Output Source Current ($V_{O[Pin\ 3]}$ = 3.5 V)	I_O+	–2.0	–4.0	–	mA

4. Low duty cycle techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.
T_{low} = –40°C for MC33060A T_{high} = +85°C for MC33060A
= 0°C for MC34060A = +70°C for MC34060A

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted.
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR SECTION (Test circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	–	3.5	4.5	V
Input Sink Current ($V_{[Pin\ 3]}$ = 0.7 V)	I_I	0.3	0.7	–	mA
DEAD–TIME CONTROL SECTION (Test circuit Figure 11)					
Input Bias Current (Pin 4) (V_{in} = 0 V to 5.25 V)	$I_{IB(DT)}$	–	−1.0	−10	μA
Maximum Output Duty Cycle (V_{in} = 0 V, C_T = 0.01 μF, R_T = 12 kΩ) (V_{in} = 0 V, C_T = 0.001 μF, R_T = 47 kΩ)	DC_{max}	 90 –	 96 92	 100 –	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 – 0	 2.8 –	 3.3 –	V
OSCILLATOR SECTION					
Frequency (C_T = 0.01 μF, R_T = 12 kΩ, T_A = 25°C) $T_A = T_{low}$ to T_{high} – MC34060A – MC33060A (C_T = 0.001 μF, R_T = 47 kΩ)	f_{osc}	 9.7 9.5 9.0 –	 10.5 – – 25	 11.3 11.5 11.5 –	kHz
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 47 kΩ)	σf_{osc}	–	1.5	–	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V)	$\Delta f_{osc}(\Delta V)$	–	0.5	2.0	%
Frequency Change with Temperature ($\Delta T_A = T_{low}$ to T_{high}) (C_T = 0.01 μF, R_T = 12 kΩ)	$\Delta f_{osc}(\Delta T)$	 – –	 4.0 –	 – –	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn–On Threshold (V_{CC} increasing, I_{ref} = 1.0 mA)	V_{th}	4.0	4.7	5.5	V
Hysteresis	V_H	50	150	300	mV
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, all other inputs and outputs open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 – –	 5.5 7.0	 10 15	mA
Average Supply Current ($V_{[Pin\ 4]}$ = 2.0 V, C_T = 0.001 μF, R_T = 47 kΩ). See Figure 11.	I_S	–	7.0	–	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula; $\sigma = \sqrt{\frac{\sum\limits_{n-1}^{N} (x_n - x)^2}{N-1}}$



This device contains 46 active transistors.

Figure 1. Block Diagram

Description

The MC34060A is a fixed−frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply (see Figure 1). An internal−linear sawtooth oscillator is frequency−programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.2}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control−signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

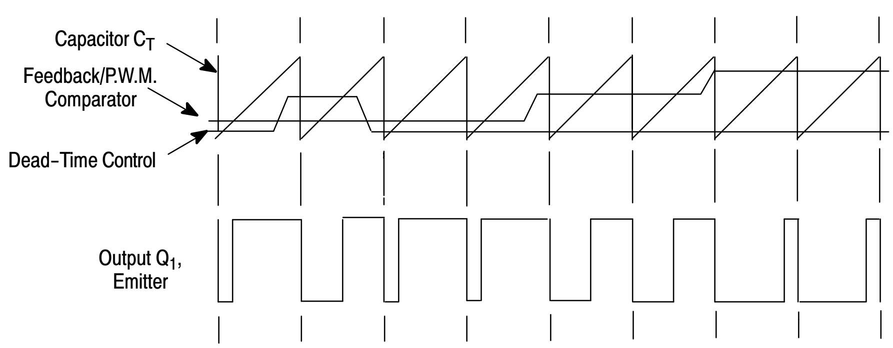


Figure 2. Timing Diagram

APPLICATIONS INFORMATION

The control signals are external inputs that can be fed into the dead−time control, the error amplifier inputs, or the feed−back input. The dead−time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth−cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time−control input to a fixed voltage, ranging between 0 V to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on−time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from −0.3 V to (V_{CC} −2.0 V), and may be used to sense power supply output voltage and current. The error−amplifier outputs are active high and are ORed together at the noninverting input of the pulse−width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC34060A has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of ±5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to +70°C.

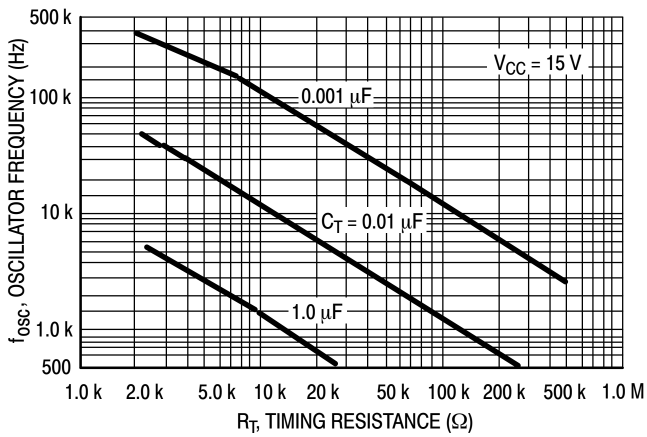


Figure 3. Oscillator Frequency versus Timing Resistance

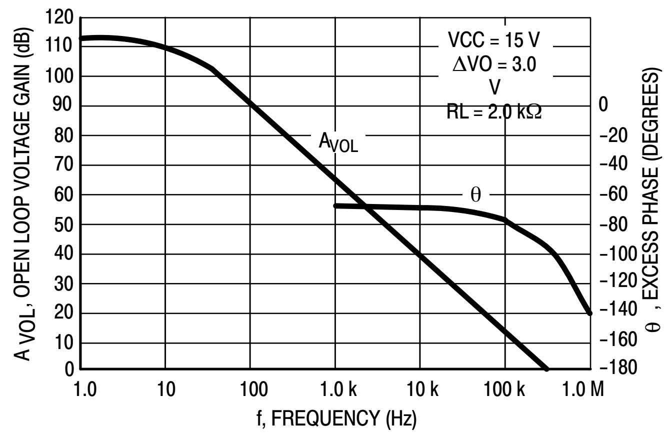


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

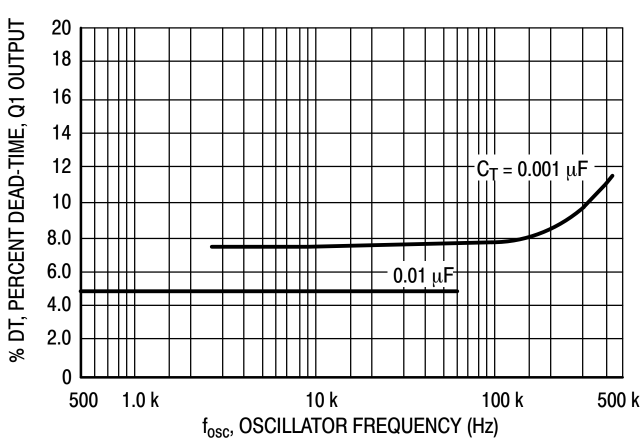


Figure 5. Percent Deadtime versus Oscillator Frequency

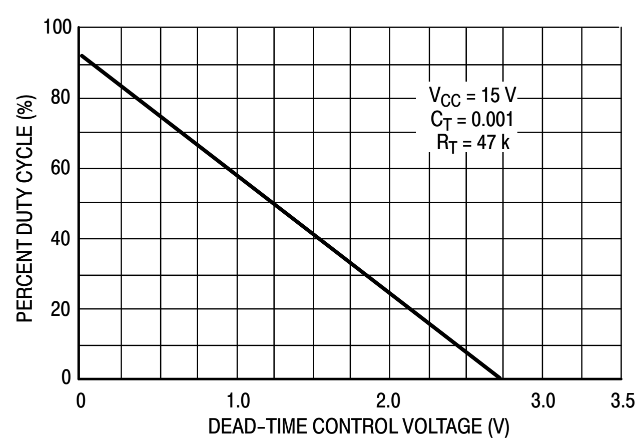


Figure 6. Percent Duty Cycle versus Dead−Time Control Voltage

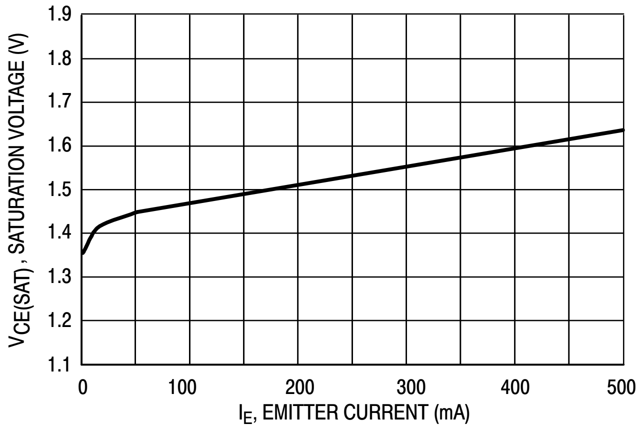


Figure 7. Emitter−Follower Configuration Output Saturation Voltage versus Emitter Current

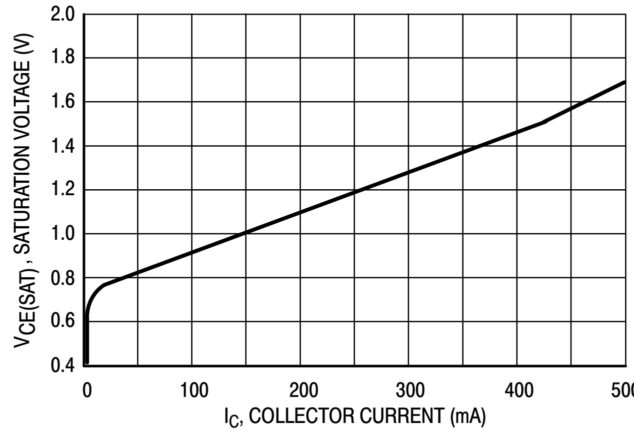


Figure 8. Common−Emitter Configuration Output Saturation Voltage versus Collector Current

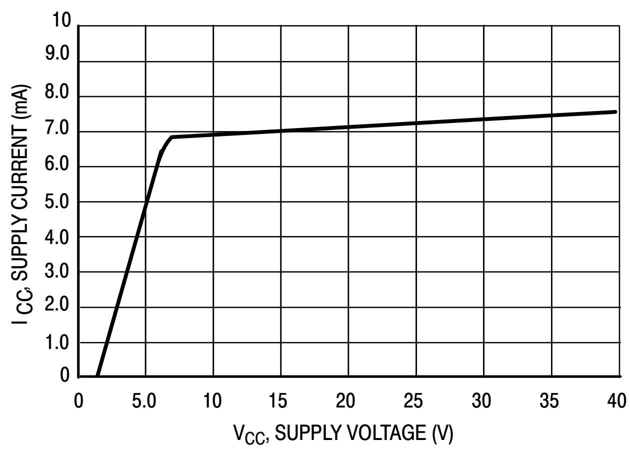


Figure 9. Standby Supply Current versus Supply Voltage

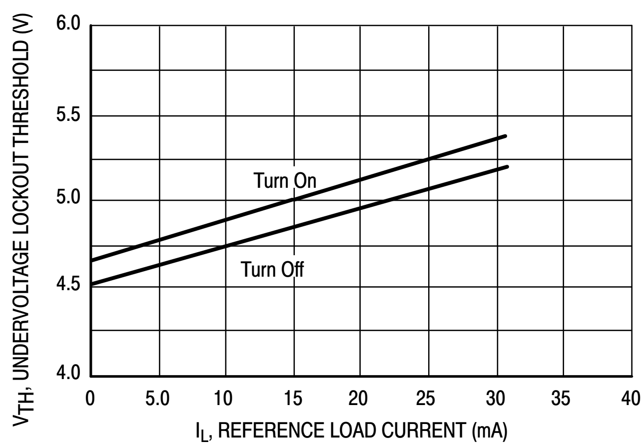


Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current

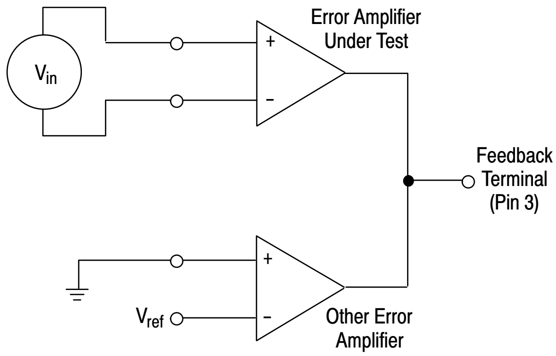


Figure 11. Error Amplifier Characteristics

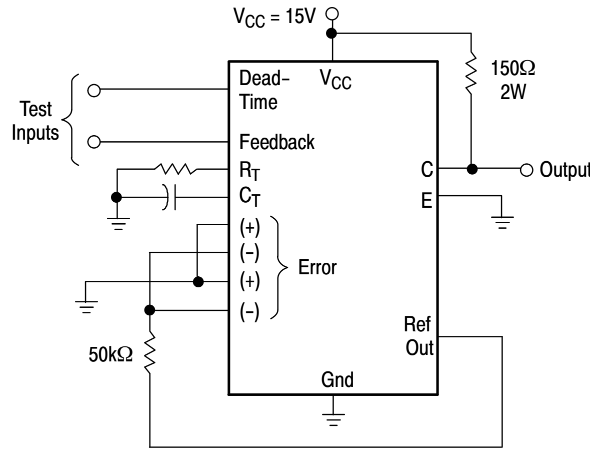


Figure 12. Deadtime and Feedback Control

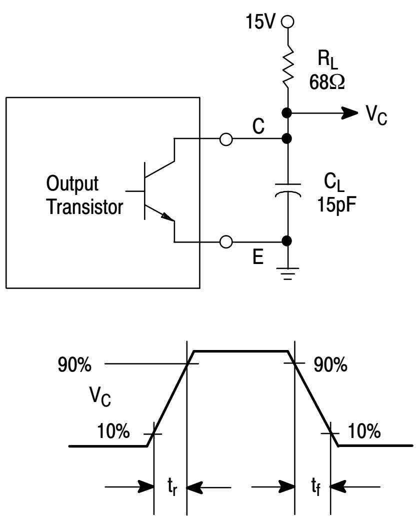


Figure 13. Common−Emitter Configuration and Waveform

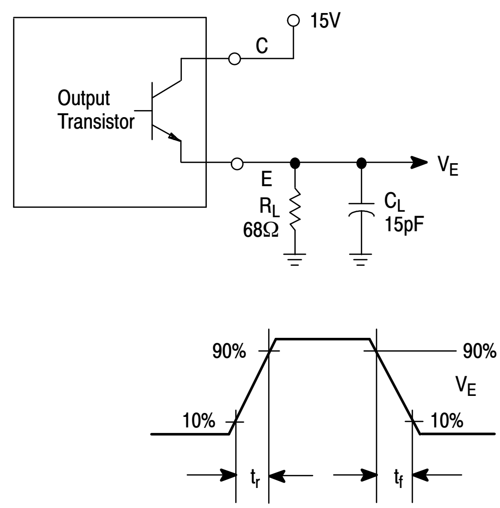


Figure 14. Emitter−Follower Configuration and Waveform

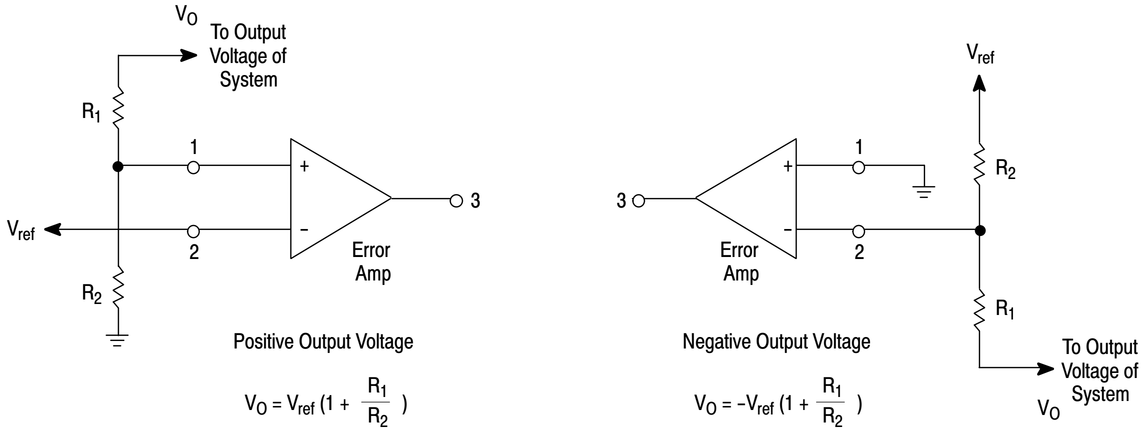


Figure 15. Error Amplifier Sensing Techniques

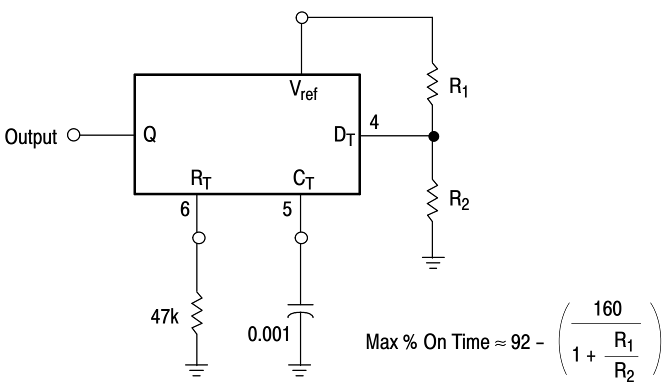


Figure 16. Deadtime Control Circuit

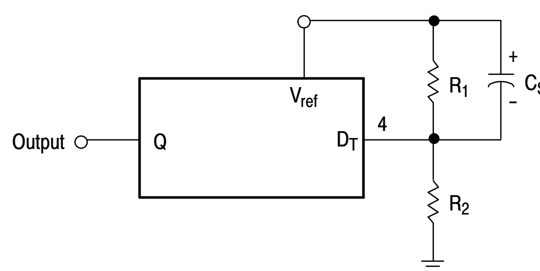


Figure 17. Soft−Start Circuit

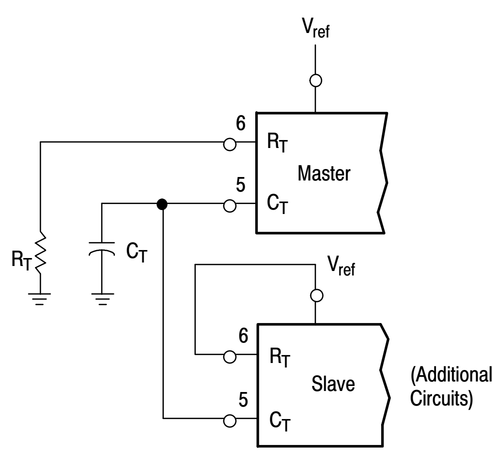
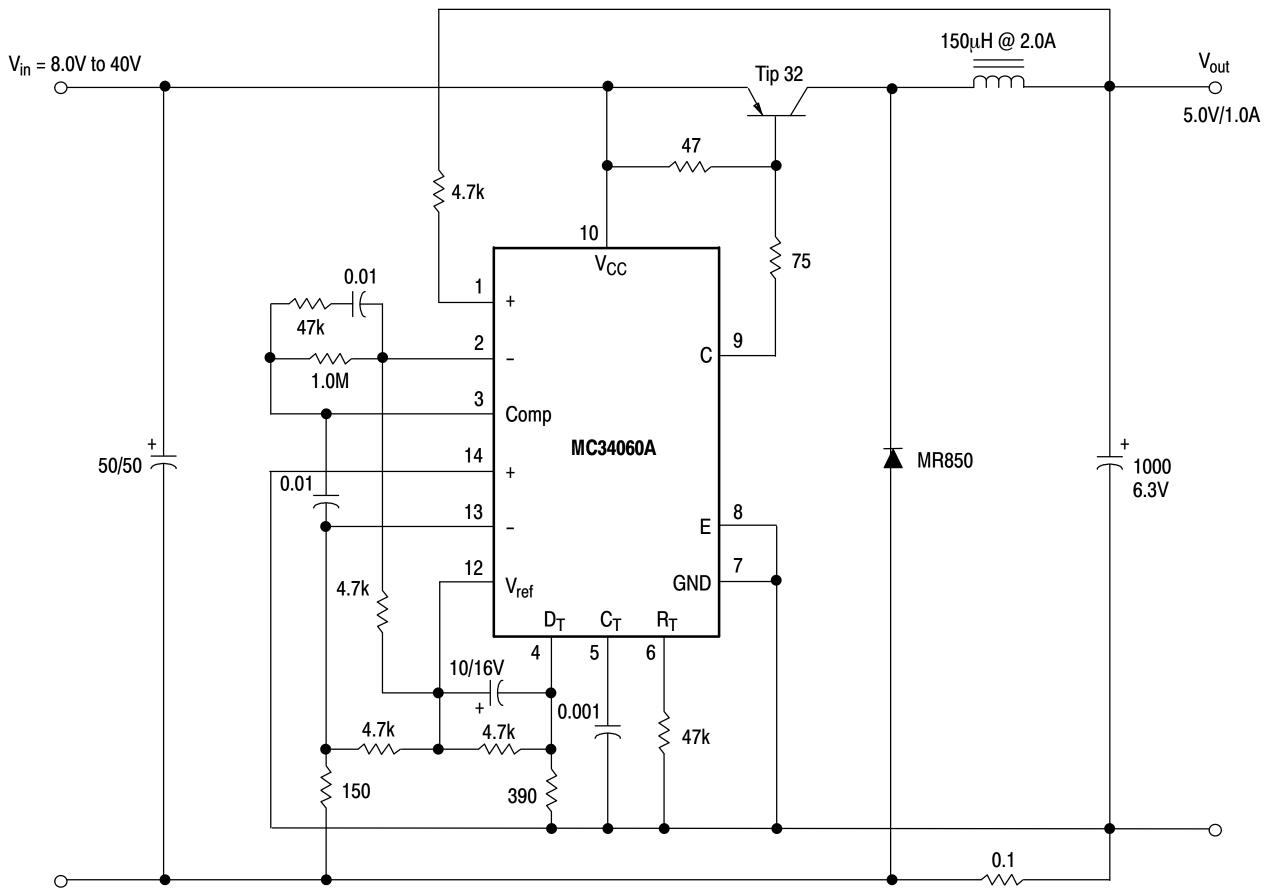
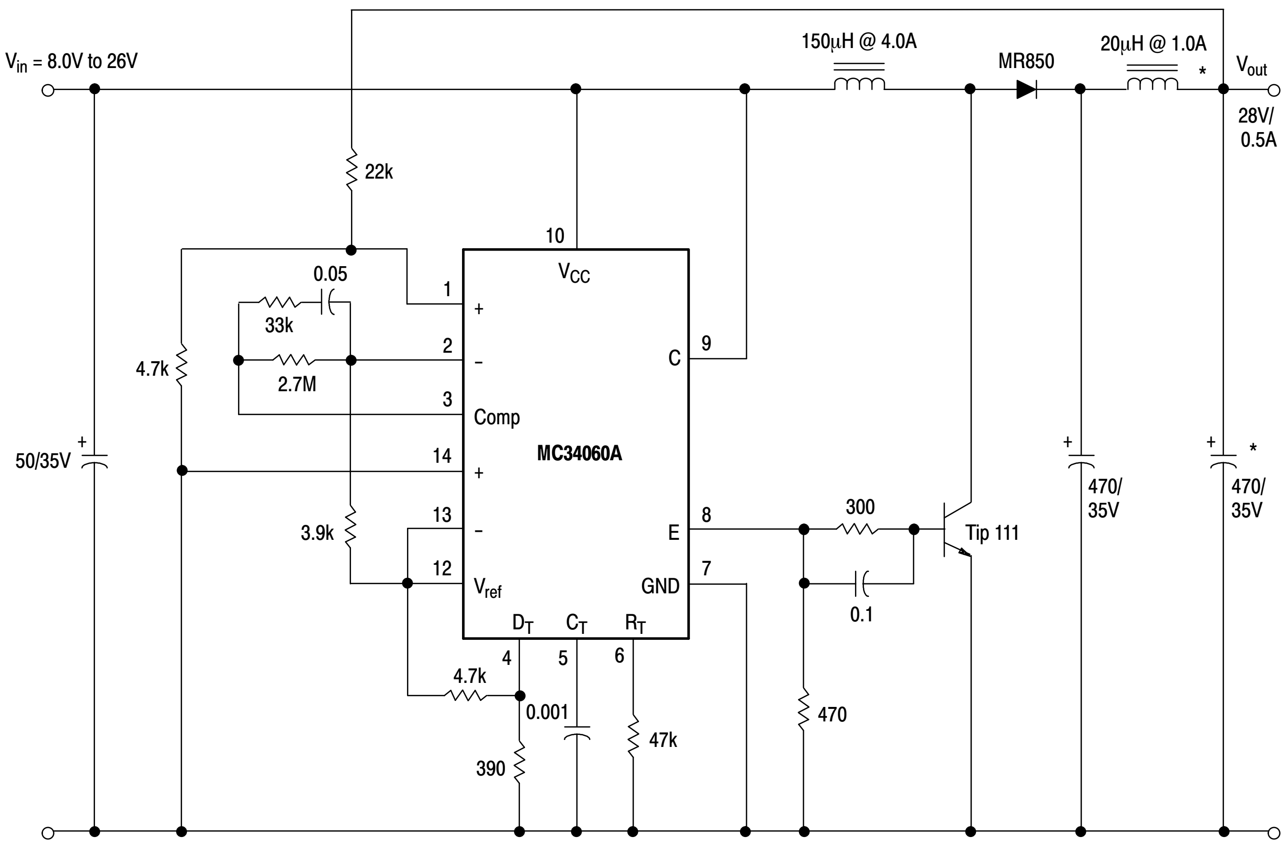


Figure 18. Slaving Two or More Control Circuits



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 1.0 A	25 mV 0.5%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	75 mV p−p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	73%

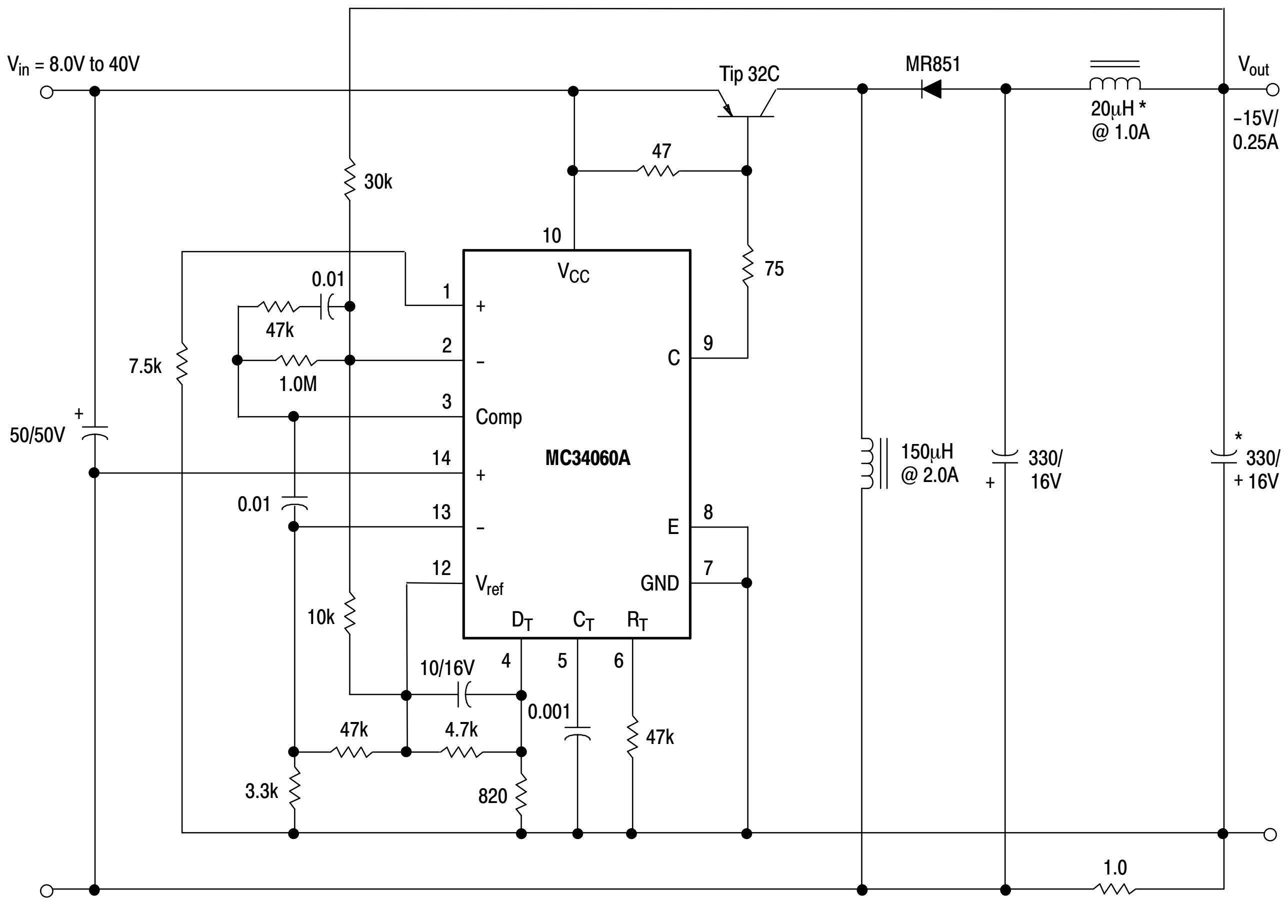
Figure 19. Step−Down Converter with Soft−Start and Output Current Limiting



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 26 V, I_O = 0.5 A	40 mV 0.14%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 0.5 A	5.0 mV 0.18%
Output Ripple	V_{in} = 12 V, I_O = 0.5 A	24 mV p−p P.A.R.D.
Efficiency	V_{in} = 12 V, I_O = 0.5 A	75%

*Optional circuit to minimize output ripple

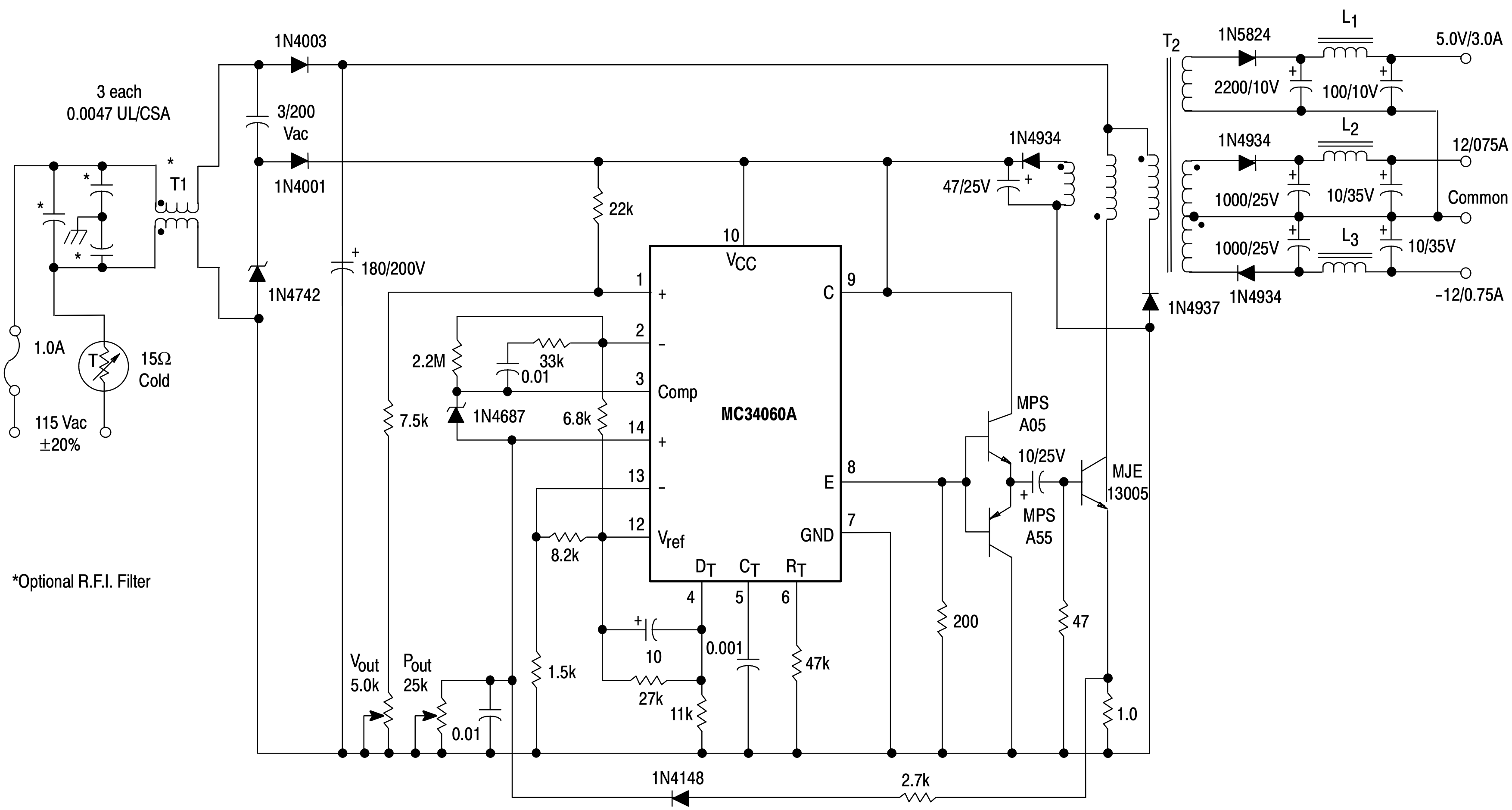
Figure 20. Step−Up Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 250 mA	52 mV 0.35%
Load Regulation	V_{in} = 12 V, I_O = 1.0 to 250 mA	47 mV 0.32%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	10 mV p−p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	330 mA
Efficiency	V_{in} = 12 V, I_O = 250 mA	86%

*Optional circuit to minimize output ripple

Figure 21. Step−Up/Down Voltage Inverting Converter with Soft−Start and Current Limiting



Test	Conditions	Results
Line Regulation 5.0 V	V_{in} = 95 Vac to 135 Vac, I_O = 3.0 A	20 mV 0.40%
Line Regulation ±12 V	V_{in} = 95 Vac to 135 Vac, I_O = ±0.75 A	52 mV 0.26%
Load Regulation 5.0 V	V_{in} = 115 Vac, I_O = 1.0 A to 4.0 A	476 mV 9.5%
Load Regulation ±12 V	V_{in} = 115 Vac, I_O = ±0.4 A to ±0.9 A	300 mV 2.5%
Output Ripple 5.0 V	V_{in} = 115 Vac, I_O = 3.0 A	45 mV p−p P.A.R.D.
Output Ripple ±12 V	V_{in} = 115 Vac, I_O = ±0.75 A	75 mV p−p P.A.R.D.
Efficiency	V_{in} = 115 Vac, I_O 5.0 V = 3.0 A I_O ±12 V = ±0.75 A	74%

T1 − Coilcraft W2961
T2 − Core: Coilcraft 11−464−16,
  0.025″ gap in each leg.
Bobbin: Coilcraft 37−573
Windings:
  Primary, 2 each, 75 turns #25 Awg Bifilar wound
  Feedback: 15 turns #26 Awg
  Secondary, 5.0 V, 6 turns @33 Awg Bifilar wound
  Secondary, 2 each, 14 turns #24 Awg Bifilar wound
L1 − Coilcraft Z7156, 15 µH @ 5.0 A
L2, L3 − Coilcraft Z7157, 25 µH @ 1.0 A

Figure 22. 33 W Off−Line Flyback Converter with Soft−Start and Primary Power Limiting

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
MC34060ADG	T_A= 0° to +70°C	SOIC−14 (Pb−Free)	55 Units / Rail
MC34060ADR2G		SOIC−14 (Pb−Free)	2500 / Tape & Reel
MC34060APG		PDIP−14 (Pb−Free)	25 Units / Rail
MC33060ADG	T_A= −40° to +85°C	SOIC−14 (Pb−Free)	55 Units / Rail
MC33060ADR2G		SOIC−14 (Pb−Free)	2500 / Tape & Reel
MC33060APG		PDIP−14 (Pb−Free)	25 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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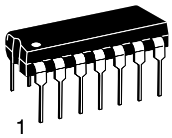

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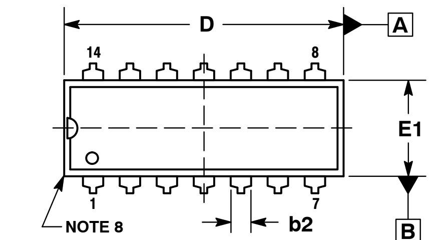
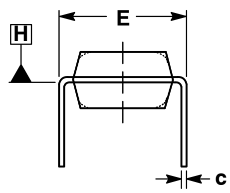
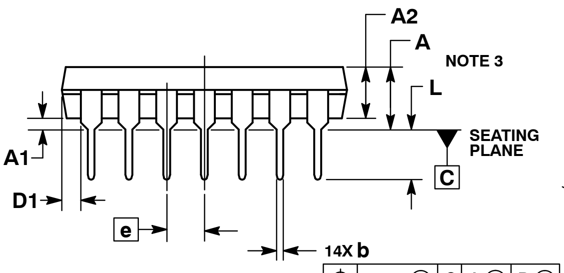


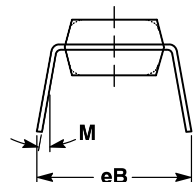
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



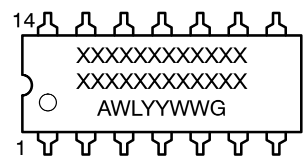
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLES ON PAGE 2

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	PDIP−14	PAGE 1 OF 2

PDIP−14
CASE 646−06
ISSUE S

DATE 22 APR 2015

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. NO CONNECTION
5. GATE
6. SOURCE
7. DRAIN
8. DRAIN
9. SOURCE
10. GATE
11. NO CONNECTION
12. GATE
13. SOURCE
14. DRAIN

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. NO CONNECTION
5. SOURCE
6. DRAIN
7. GATE
8. GATE
9. DRAIN
10. SOURCE
11. NO CONNECTION
12. SOURCE
13. DRAIN
14. GATE

STYLE 6:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 7:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 8:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 9:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

STYLE 10:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 12:
PIN 1. COMMON CATHODE
2. COMMON ANODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. COMMON ANODE
7. COMMON CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. ANODE/CATHODE
14. ANODE/CATHODE

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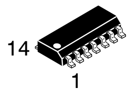
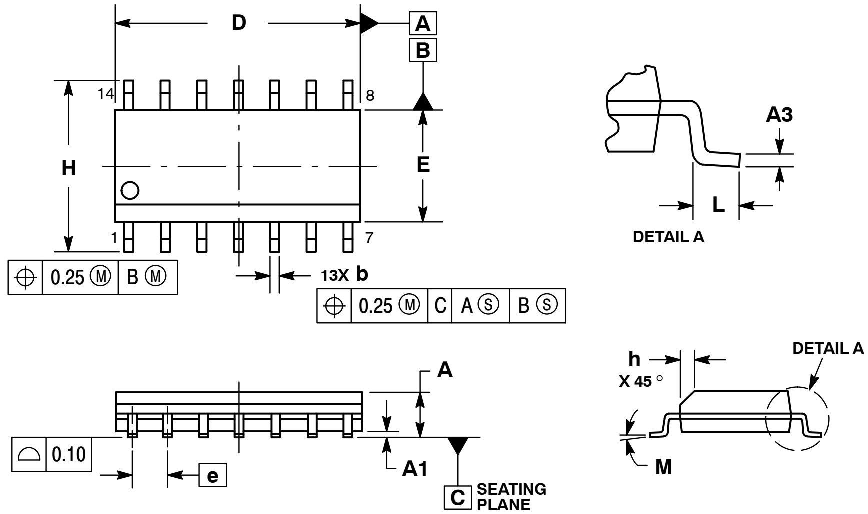
DESCRIPTION:	PDIP−14	PAGE 2 OF 2



SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

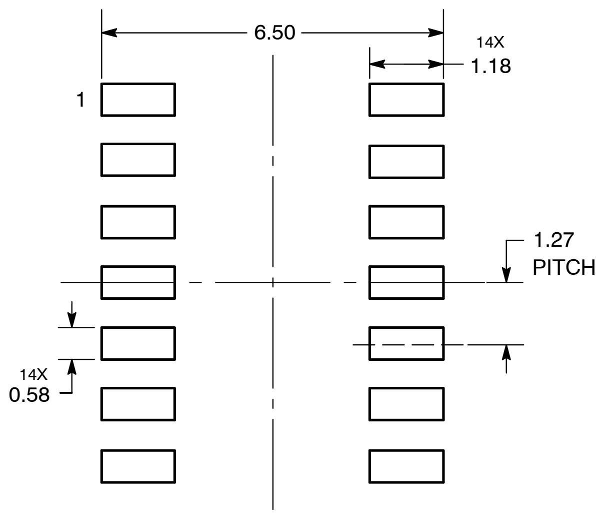
DATE 03 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

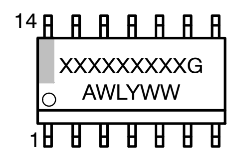
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42565B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOIC−14 NB**	**PAGE 1 OF 2**

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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