

# MC74AC273, MC74ACT273

## Octal D Flip-Flop

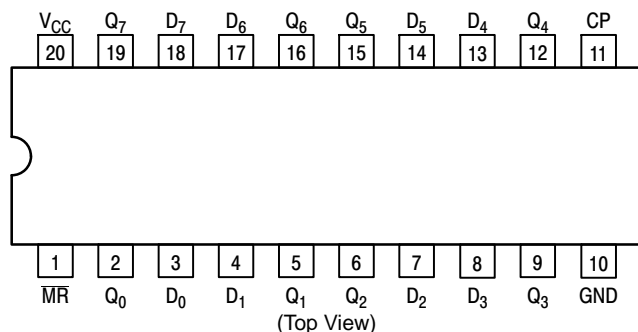
The MC74AC273/74ACT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ( $\overline{MR}$ ) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the  $\overline{MR}$  input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

### Features

- Ideal Buffer for MOS Microprocessor or Memory
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Buffered, Asynchronous Master Reset
- See MC74AC377 for Clock Enable Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC374 for 3-State Version
- Outputs Source/Sink 24 mA
- 'ACT273 Has TTL Compatible Inputs
- These are Pb-Free Devices



Pinout: 20-Lead Packages Conductors

### MODE SELECT-FUNCTION TABLE

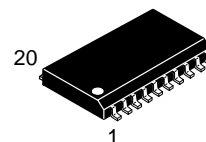
Operating Mode	Inputs			Outputs
	MR	CP	D <sub>n</sub>	Q <sub>n</sub>
Reset (Clear)	L	X	X	L
Load '1'	H	⌋	H	H
Load '0'	H	⌋	L	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ⌋ = LOW-to-HIGH Clock Transition

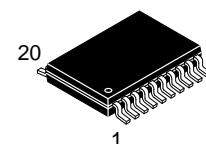


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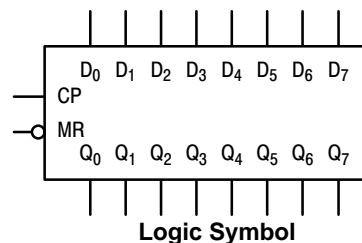
SOIC-20WB  
 SUFFIX DW  
 CASE 751D



TSSOP-20  
 SUFFIX DT  
 CASE 948E

### PIN ASSIGNMENT

PIN	FUNCTION
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q <sub>0</sub> -Q <sub>7</sub>	Data Outputs



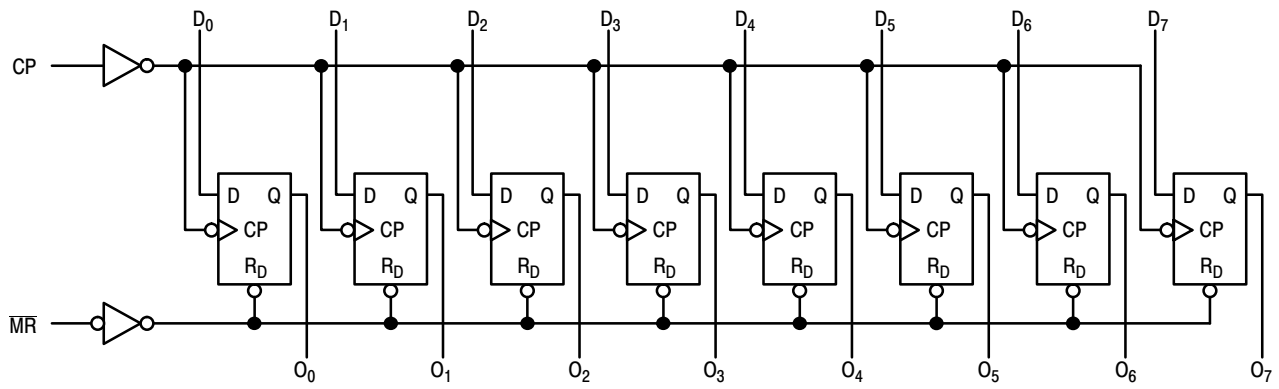
### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 6 of this data sheet.

# MC74AC273, MC74ACT273



NOTE: That this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Figure 1. Logic Diagram**

# MC74AC273, MC74ACT273

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND) (Note 1)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	DC Input Diode Current	±20	mA
I <sub>OK</sub>	DC Output Diode Current	±50	mA
I <sub>OUT</sub>	DC Output Sink/Source Current	±50	mA
I <sub>CC</sub>	DC Supply Current, per Output Pin	±50	mA
I <sub>GND</sub>	DC Ground Current, per Output Pin	±100	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead temperature, 1 mm from Case for 10 Seconds	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	140	°C
θ <sub>JA</sub>	Thermal Resistance (Note 2)	SOIC TSSOP 65.8 110.7	°C/W
MSL	Moisture Sensitivity	SOIC TSSOP Level 3 Level 1	
F <sub>R</sub>	Flammability Rating	Oxygen Index: 30% – 35%	UL 94 V-0 @ 0.125 in
V <sub>ESD</sub>	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	> 2000 > 200 > 1000 V
I <sub>Latchup</sub>	Latchup Performance	Above V <sub>CC</sub> and Below GND at 85°C (Note 6)	±100 mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I<sub>OUT</sub> absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V <sub>CC</sub>	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Ref. to GND)	0	-	V <sub>CC</sub>	V	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Note 7) 'AC Devices except Schmitt Inputs	V <sub>CC</sub> @ 3.0 V	-	150	-	ns/V
		V <sub>CC</sub> @ 4.5 V	-	40	-	
		V <sub>CC</sub> @ 5.5 V	-	25	-	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Note 8) 'ACT Devices except Schmitt Inputs	V <sub>CC</sub> @ 4.5 V	-	10	-	ns/V
		V <sub>CC</sub> @ 5.5 V	-	8.0	-	
T <sub>A</sub>	Operating Ambient Temperature Range	-40	25	85	°C	
I <sub>OH</sub>	Output Current – High	-	-	-24	mA	
I <sub>OL</sub>	Output Current – Low	-	-	24	mA	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. V<sub>IN</sub> from 30% to 70% V<sub>CC</sub>; see individual Data Sheets for devices that differ from the typical input rise and fall times.
8. V<sub>IN</sub> from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

# MC74AC273, MC74ACT273

## DC CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	74AC		74AC		Unit	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I <sub>OUT</sub> = -50 μA
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	-	2.56	2.46		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -12 mA -24 mA -24 mA
		4.5	-	3.86	3.76			
		5.5	-	4.86	4.76			
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I <sub>OUT</sub> = 50 μA
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	-	0.36	0.44		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA 24 mA 24 mA
		4.5	-	0.36	0.44			
		5.5	-	0.36	0.44			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	-	±0.1	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>OLD</sub> I <sub>OHD</sub>	†Minimum Dynamic Output Current	5.5	-	-	75		mA	V <sub>OLD</sub> = 1.65 V Max V <sub>OHD</sub> = 3.85 V Min
		5.5	-	-	-75			
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	-	8.0	80		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V<sub>CC</sub>.

## AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V <sub>CC</sub> * (V)	74AC			74AC		Unit	Figure No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	3.3 5.0	90 140	125 175	- -	75 125	- -	Mhz	3-3
t <sub>PLH</sub>	Propagation Delay Clock to Output	3.3 5.0	4.0 3.0	7.0 5.5	12.5 9.0	3.0 2.5	14.0 10.0	ns	3-6
t <sub>PHL</sub>	Propagation Delay Clock to Output	3.3 5.0	4.0 3.0	7.0 5.0	13.0 10.0	3.5 2.5	14.5 11.0	ns	3-6
t <sub>PHL</sub>	Propagation Delay MR to Output	3.3 5.0	4.0 3.0	7.0 5.0	13.0 10.0	3.5 2.5	14.0 10.5	ns	3-6

\*Voltage Range 3.3 V is 3.3 V ±0.3 V. Voltage Range 5.0 V is 5.0 V ±0.5 V.

## AC OPERATING REQUIREMENTS

Symbol	Parameter	V <sub>CC</sub> * (V)	74AC		74AC		Unit	Figure No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Typ	Guaranteed Minimum				
t <sub>s</sub>	Setup Time, HIGH or LOW Data to CP	3.3 5.0	3.5 2.5	5.5 4.0	6.0 4.5		ns	3-9
t <sub>h</sub>	Hold Time, HIGH or LOW Data to CP	3.3 5.0	-2.0 -1.0	0 1.0	0 1.0		ns	3-9
t <sub>w</sub>	Clock Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5	5.5 4.0	6.0 4.5		ns	3-6
t <sub>w</sub>	MR Pulse Width HIGH or LOW	3.3 5.0	2.0 1.5	5.5 4.0	6.0 4.5		ns	3-6
t <sub>rec</sub>	Recovery Time MR to CP	3.3 5.0	1.5 1.0	3.5 2.0	4.5 3.0		ns	3-9

\*Voltage Range 3.3 V is 3.3 V ±0.3 V. Voltage Range 5.0 V is 5.0 V ±0.5 V.

# MC74AC273, MC74ACT273

## DC CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	74ACT		74ACT		Unit	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0		V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8		V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4		V	I <sub>OUT</sub> = -50 μA
		4.5 5.5	- -	3.86 4.86	3.76 4.76		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA -24 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1		V	I <sub>OUT</sub> = 50 μA
		4.5 5.5	- -	0.36 0.36	0.44 0.44		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA 24 mA
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	-	±0.1	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND
ΔI <sub>CCT</sub>	Additional Max. I <sub>CC</sub> /Input	5.5	0.6	-	1.5		mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V
I <sub>OLD</sub> I <sub>OHD</sub>	†Minimum Dynamic Output Current	5.5 5.5	- -	- -	75 -75		mA	V <sub>OLD</sub> = 1.65 V Max V <sub>OHD</sub> = 3.85 V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	-	8.0	80		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

## AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT			74ACT		Unit	Figure No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	5.0	125	200	-	125	-	MHz	3-3
t <sub>PHL</sub>	Propagation Delay Clock to Output	5.0	3.0	6.0	10	2.5	11.0	ns	3-6
t <sub>PLH</sub>	Propagation Delay Clock to Output	5.0	3.0	6.5	11	2.5	12.0	ns	3-6
t <sub>PHL</sub>	Propagation Delay $\overline{MR}$ to Output	5.0	3.0	7.0	11	2.5	11.5	ns	3-6

\*Voltage Range 5.0 V is 5.0 V ±0.5 V.

## AC OPERATING REQUIREMENTS

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT		74ACT		Unit	Figure No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Typ	Guaranteed Minimum				
t <sub>s</sub>	Setup Time, HIGH or LOW – Data to CP	5.0	3.0	4.5	5.0		ns	3-9
t <sub>h</sub>	Hold Time, HIGH or LOW – Data to CP	5.0	-2.5	2.0	2.0		ns	3-9
t <sub>w</sub>	Clock Pulse Width – HIGH or LOW	5.0	2.5	4.0	4.5		ns	3-6
t <sub>w</sub>	$\overline{MR}$ Pulse Width – HIGH or LOW	5.0	2.5	4.0	4.5		ns	3-6
t <sub>rec</sub>	Recovery Time – $\overline{MR}$ to CP	5.0	-1.0	2.0	3.0		ns	3-6

\*Voltage Range 5.0 V is 5.0 V ±0.5 V.

## CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0 V
C <sub>PD</sub>	Power Dissipation Capacitance	50	pF	V <sub>CC</sub> = 5.0 V

# MC74AC273, MC74ACT273

## ORDERING INFORMATION

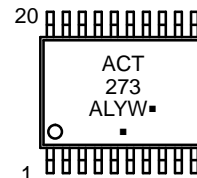
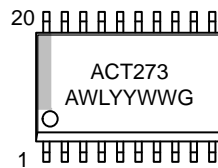
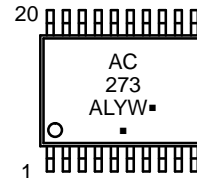
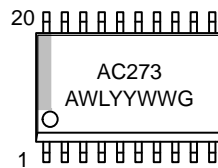
Device	Package	Shipping†
MC74AC273DWG	SOIC-20WB (Pb-Free)	38 Units / Rail
MC74AC273DWR2G	SOIC-20WB (Pb-Free)	1000 / Tape & Reel
MC74AC273DTR2G	TSSOP-20 (Pb-Free)	2500 / Tape & Reel
MC74ACT273DWG	SOIC-20WB (Pb-Free)	38 Units / Rail
MC74ACT273DWR2G	SOIC-20WB (Pb-Free)	1000 / Tape & Reel
MC74ACT273DTR2G	TSSOP-20 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MARKING DIAGRAMS

**SOIC-20WB**

**TSSOP-20**



- A = Assembly Location
  - WL, L = Wafer Lot
  - YY, Y = Year
  - WW, W = Work Week
  - G or ■ = Pb-Free Package
- (Note: Microdot may be in either location)

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015

SCALE 1:1



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

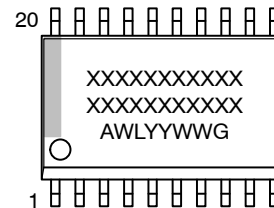
### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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<b>DESCRIPTION:</b>	<b>SOIC-20 WB</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

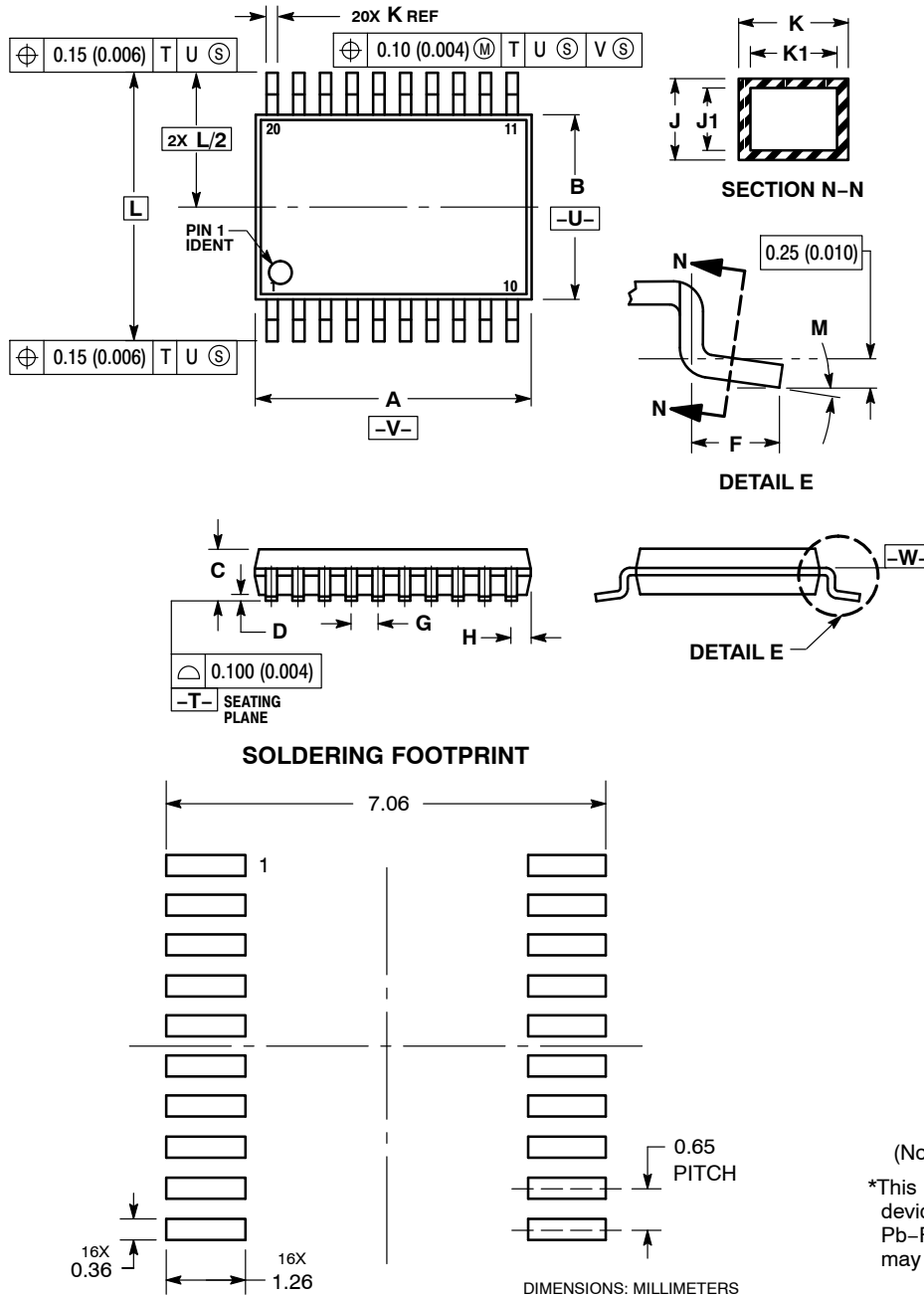
ON Semiconductor®



TSSOP-20 WB  
CASE 948E  
ISSUE D

DATE 17 FEB 2016

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -V-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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