

# MC74HCT20A

## Dual 4-Input NAND Gate with LSTTL-Compatible Inputs

### High-Performance Silicon-Gate CMOS

The MC74HCT20A is identical in pinout to the LS20. The device inputs are compatible with standard CMOS LSTTL outputs.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 V to 5.5 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- These are Pb-Free Devices

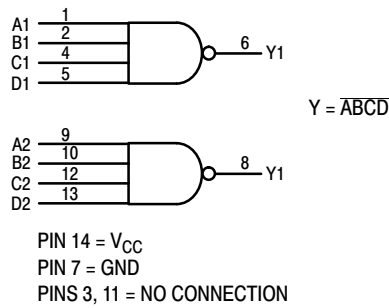


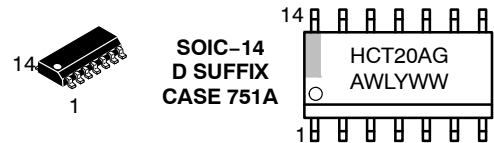
Figure 1. Logic Diagram



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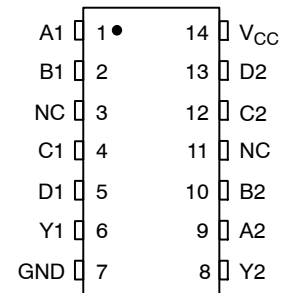
#### MARKING DIAGRAMS



A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs				Output
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

# MC74HCT20A

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V	
$V_{in}$	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V	
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V	
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA	
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA	
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA	
$P_D$	Power Dissipation in Still Air	SOIC Package TSSOP Package	500 450	mW
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature Range, All Package Types	-55	+125	$^{\circ}C$
$t_r, t_f$	Input Rise/Fall Time (Figure 1)	0	500	ns

## DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	$V_{CC}$ V	Guaranteed Limit			Unit
				-55 to 25 $^{\circ}C$	$\leq 85^{\circ}C$	$\leq 125^{\circ}C$	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1V$ $ I_{out}  \leq 20\mu A$	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.1V$ $ I_{out}  \leq 20\mu A$	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \leq 20\mu A$	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out}  \leq 20\mu A$	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	4.5	0.26	0.33	0.40	$\mu A$
			5.5	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\mu A$	4.5	1	10	40	$\mu A$
			5.5				
$\Delta I_{CC}$	Additional Quiescent Supply Current	$V_{in} = 2.4V$ , Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0\mu A$	5.5	$\geq -55^{\circ}C$	25 to 125 $^{\circ}C$		mA
					2.9	2.4	

- Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
- Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

# MC74HCT20A

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ , $V_{CC} = 5.0 \text{ V}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		- 55 to 25°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 2 and 3)	28	35	42	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 2 and 3)	15	19	22	ns
$C_{in}$	Maximum Input Capacitance	10	10	10	pF

$C_{PD}$	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$		pF
		26		

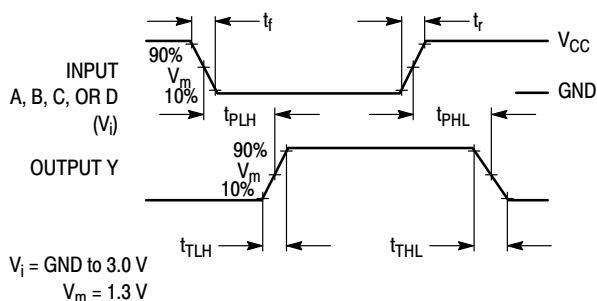
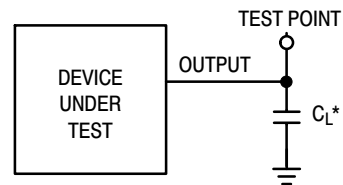


Figure 2. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 3. Test Circuit

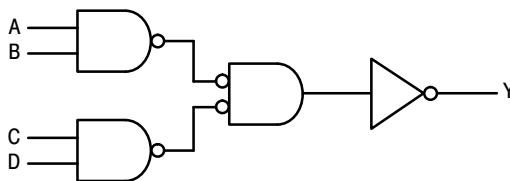


Figure 4. Expanded Logic Diagram  
(1/2 of the Device)

## ORDERING INFORMATION

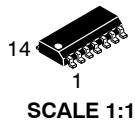
Device	Package	Shipping†
MC74HCT20ADG	SOIC-14 (Pb-Free)	55 Units/Rail
MC74HCT20ADR2G	SOIC-14 (Pb-Free)	2500/Tape & Reel
MC74HCT20ADTR2G	TSSOP-14*	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

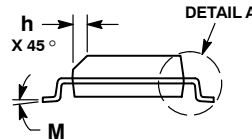
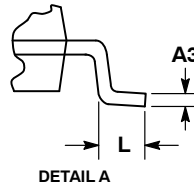
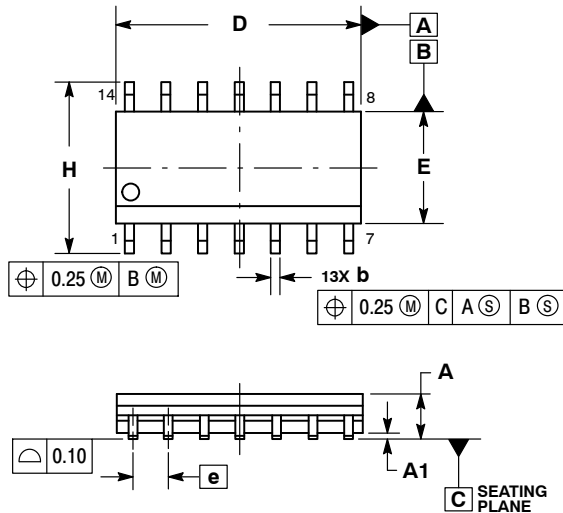
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SOIC-14 NB  
CASE 751A-03  
ISSUE L

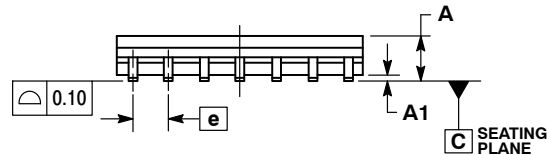
DATE 03 FEB 2016



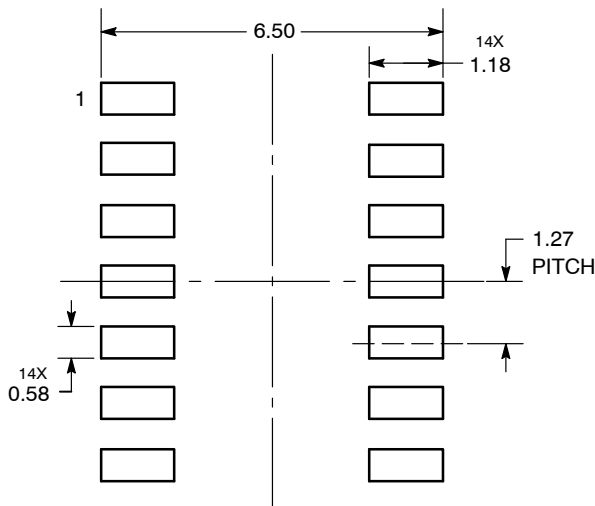
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°



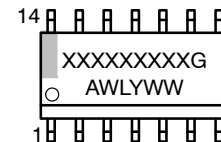
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE


STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
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 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

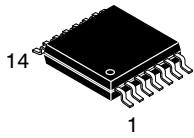
STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
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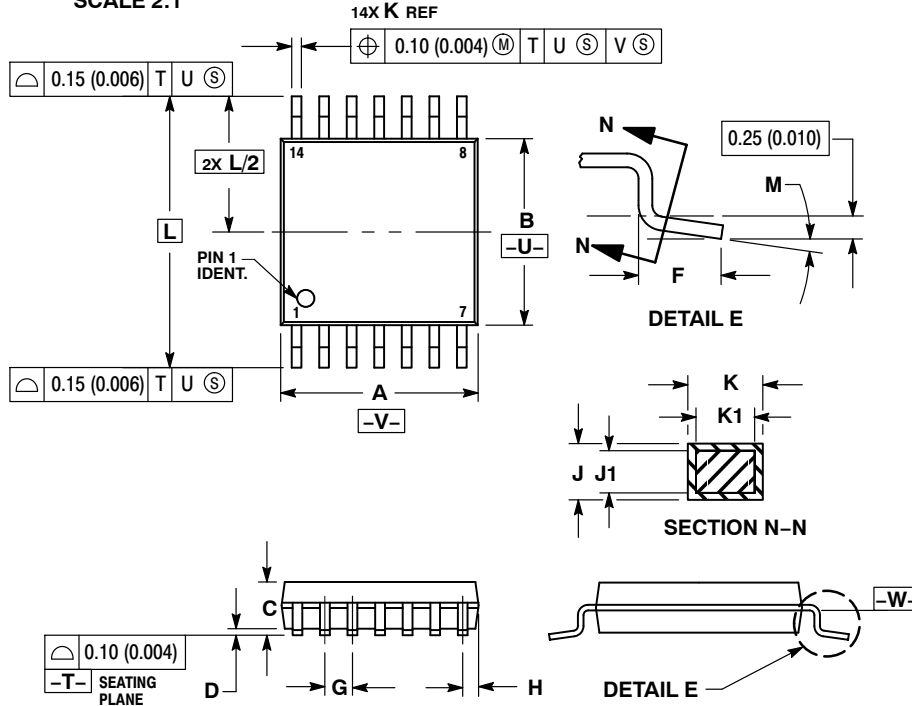
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**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

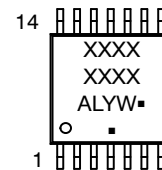


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

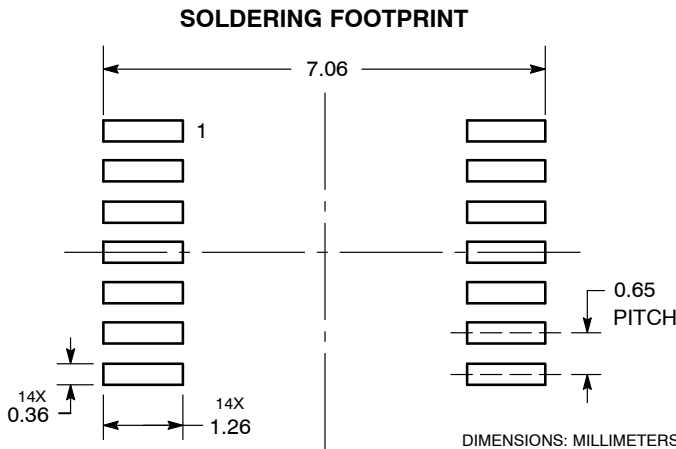
**GENERIC MARKING DIAGRAM\***



- A = Assembly Location
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- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.



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[NLX1G11AMUTCG](#) [NLX1G97MUTCG](#) [74LS38](#) [74LVC32ADTR2G](#) [MC74HCT20ADTR2G](#) [NLV17SZ00DFT2G](#) [NLV17SZ02DFT2G](#)

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[NLX1G99DMUTWG](#) [NLVVHC1G00DFT2G](#) [NLVHC1G08DFT2G](#) [NLV7SZ57DFT2G](#) [NLV74VHC04DTR2G](#) [NLV27WZ86USG](#)

[NLV27WZ00USG](#) [NLU1G86CMUTCG](#) [NLU1G08CMUTCG](#) [NL17SZ32P5T5G](#) [NL17SZ00P5T5G](#) [NL17SH02P5T5G](#) [74AUP2G00RA3-7](#)

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