MC74LVX139

Dual 2-to-4 Decoder/ Demultiplexer

The MC74LVX139 is an advanced high speed CMOS 2–to–4 decoder/demultiplexer fabricated with silicon gate CMOS technology.

When the device is enabled ($\overline{E}$ = low), it can be used for gating or as a data input for demultiplexing operations. When the enable input is held high, all four outputs are fixed high, independent of other inputs.

The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: t_{PD} = 6.0 ns (Typ) at V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 3.6 V Operating Range
- Low Noise: V_{OLP} = 0.5 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- ESD Performance:
  Human Body Model > 2000 V;
  Machine Model > 200 V
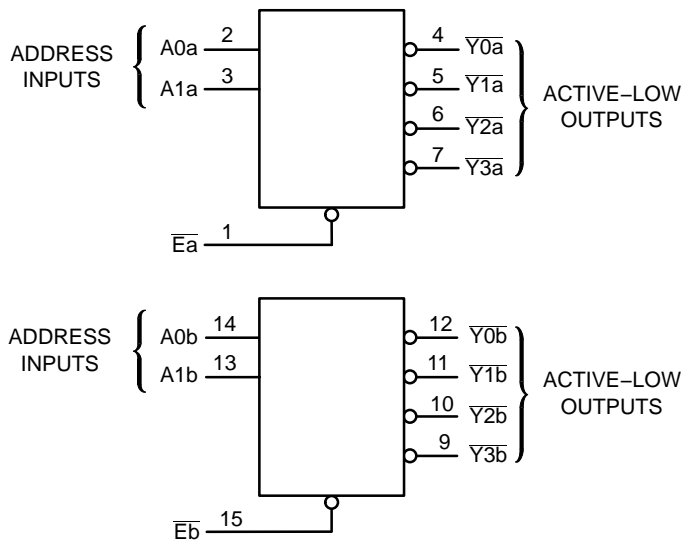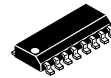- These Devices are Pb−Free and are RoHS Compliant

ON Semiconductor®

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SOIC−16
D SUFFIX
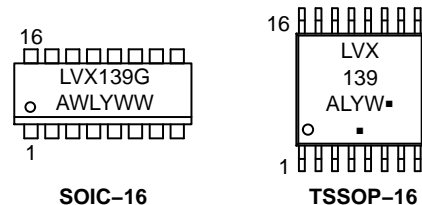**CASE 751B**

TSSOP−16
DT SUFFIX
CASE 948F

PIN ASSIGNMENT

MARKING DIAGRAMS

SOIC−16 **TSSOP−16**

LVX139 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package
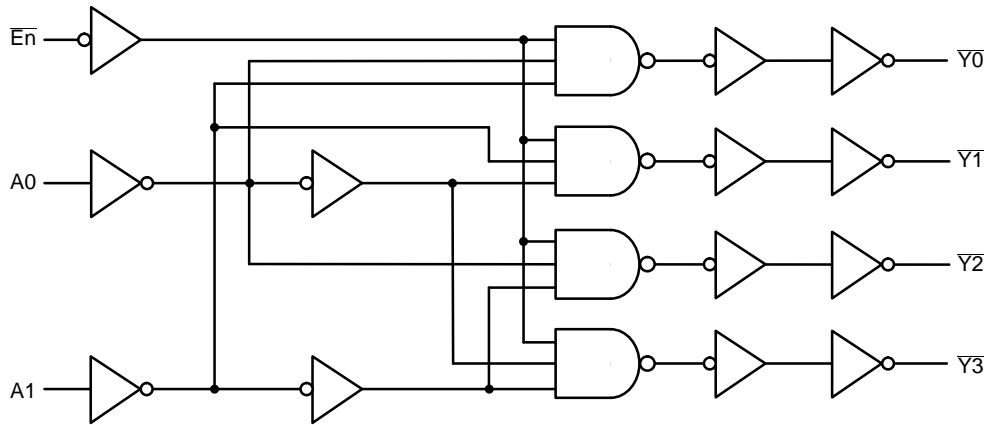
(Note: Microdot may be in either location)

FUNCTION TABLE

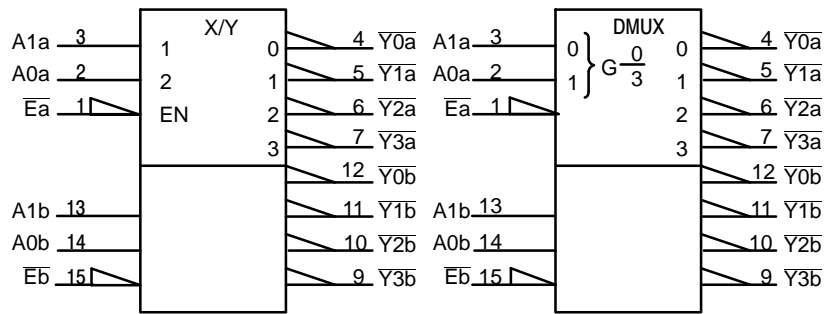| Inputs			Outputs			
$\overline{E}$	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

ORDERING INFORMATION

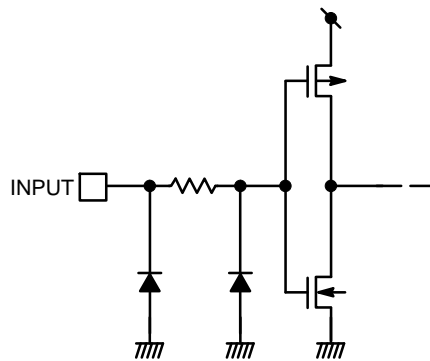See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Figure 1. Logic Diagram

August, 2014 – Rev. 4

1

Figure 2. Expanded Logic Diagram
(1/2 of Device)

Figure 3. IEC Logic Diagram

Figure 4. Input Equivalent Circuit

MC74LVX139

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	Digital Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
P_D	Power Dissipation in Still Air	SOIC Package TSSOP	200 180	mW
T_{STG}	Storage Temperature Range		−65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 200 > 2000	V
$I_{LATCHUP}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 4)	±300	mA
θ_{JA}	Thermal Resistance, Junction−to−Ambient	SOIC Package TSSOP	143 164	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Tested to EIA/JESD22−A114−A
2. Tested to EIA/JESD22−A115−A
3. Tested to JESD22−C101−A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	3.6	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage	Output in 3−State High or Low State	0	V_{CC}	V
T_A	Operating Temperature Range, all Package Types		−40	85	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 5.0 V ± 0.5 V	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MC74LVX139

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_CC (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	−40°C ≤ T_A ≤ 85°C Min	−40°C ≤ T_A ≤ 85°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 3.6	0.75 V_CC 0.7 V_CC 0.7 V_CC	– – –	– – –	0.75 V_CC 0.7 V_CC 0.7 V_CC	– – –	V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 3.6	– – –	– – –	0.25 V_CC 0.3 V_CC 0.3 V_CC	– – –	0.25 V_CC 0.3 V_CC 0.3 V_CC	V
V_{OH}	High–Level Output Voltage	I_{OH} = –50 µA I_{OH} = –50 µA I_{OH} = –4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 3.0	– – –	1.9 2.9 2.48	– – –	V
V_{OL}	Low–Level Output Voltage	I_{OL} = 50 µA I_{OH} = 50 µA I_{OH} = 4 mA	2.0 3.0 3.0	– – –	0.0	0.1 0.1 0.36	– – –	0.1 0.1 0.44	V
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 3.6	–	–	±0.1	–	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per package)	V_{IN} = V_CC or GND	3.6	1.0	1.0	2.0	–	–	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS Input $t_r = t_f$ = 3.0 ns

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	−40°C ≤ T_A ≤ 85°C Min	−40°C ≤ T_A ≤ 85°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	V_{CC} = 2.7 V	C_L = 15 pF C_L = 50 pF	– –	8.5 11.0	15.0 16.5	1.0 1.0	17.8 18.0	ns
		V_{CC} = 3.3 V ± 0.3 V	C_L = 15 pF C_L = 50 pF	– –	6.0 8.5	10.0 13.0	1.0 1.0	12.0 15.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{E}$ to Y	V_{CC} = 2.7 V	C_L = 15 pF C_L = 50 pF	– –	8.0 10.0	13.0 16.5	1.0 1.0	15.5 18.0	ns
		V_{CC} = 3.3 V ± 0.3 V	C_L = 15 pF C_L = 50 pF	– –	5.5 7.5	8.2 13.0	1.0 1.0	10.0 15.0	
C_{IN}	Maximum Input Capacitance			–	4	10	–	10	pF

Symbol	Parameter	Typical @ 25°C, V_CC = 3.3 V	Unit
C_{PD}	Power Dissipation Capacitance (Note 5)	26	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/2$ (per decoder). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.
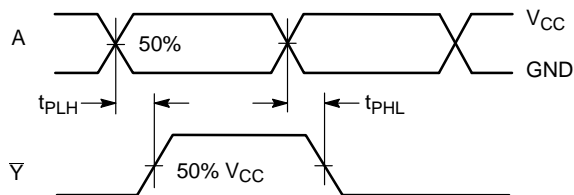
Figure 5. Switching Waveform
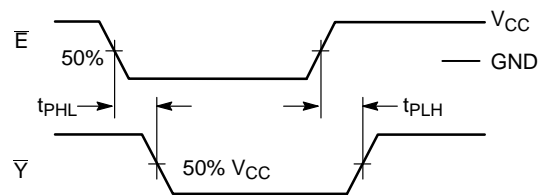
Figure 6. Switching Waveform

MC74LVX139

DEVICE UNDER TEST

OUTPUT

TEST POINT

C_L*
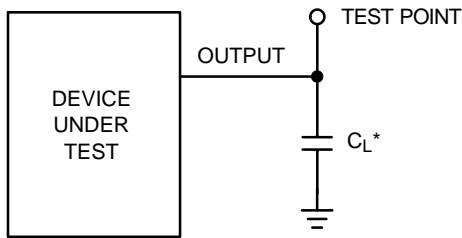
*Includes all probe and jig capacitance

Figure 7. Test Circuit

ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX139DR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74LVX139DTR2G	TSSOP−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

EMBOSSED CARRIER DIMENSIONS (See Notes 6 and 7)

Tape Size	B₁ Max	D	D₁	E	F	K	P	P₀	P₂	R	T	W
8 mm	4.35 mm (0.179")	1.5 mm + 0.1 −0.0 (0.059" +0.004 −0.0)	1.0 mm Min (0.179")	1.75 mm ±0.1 (0.069 ±0.004")	3.5 mm ±0.5 (1.38 ±0.002")	2.4 mm Max (0.094")	4.0 mm ±0.10 (0.157 ±0.004")	4.0 mm ±0.1 (0.157 ±0.004")	2.0 mm ±0.1 (0.079 ±0.004")	25 mm (0.98")	0.6 mm (0.024")	8.3 mm (0.327")
12 mm	8.2 mm (0.323")		1.5 mm Min (0.060)		5.5 mm ±0.5 (0.217 ±0.002")	6.4 mm Max (0.252")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004")			30 mm (1.18")		12.0 mm ±0.3 (0.470 ±0.012")
16 mm	12.1 mm (0.476")				7.5 mm ±0.10 (0.295 ±0.004")	7.9 mm Max (0.311")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004") 12.0 mm ±0.10 (0.472 ±0.004")					16.3 mm (0.642")
24 mm	20.1 mm (0.791")				11.5 mm ±0.10 (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 mm ±0.10 (0.63 ±0.004")					24.3 mm (0.957")

6. Metric Dimensions Govern−English are in parentheses for reference only.
7. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SOIC−16
CASE 751B−05
ISSUE K

DATE 29 DEC 2006

SCALE 1:1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

P 8 PL

⊕ | 0.25 (0.010) Ⓜ | B Ⓢ

D 16 PL

⊕ | 0.25 (0.010) Ⓜ | T | B Ⓢ | A Ⓢ

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT

8X
6.40

16X 1.12

16X
0.58

1.27
PITCH

DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−16		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TSSOP−16
CASE 948F−01
ISSUE B

DATE 19 OCT 2006

SCALE 2:1

16

1

16X K REF

$\oplus$ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

0.15 (0.006) | T | U Ⓢ

2X L/2

L

PIN 1 IDENT.

0.15 (0.006) | T | U Ⓢ

A

−V−

16   9

16   9
B
−U−

1   8

K

K1

J1

J

SECTION N−N

N

0.25 (0.010)

N

M

F

DETAIL E

C

0.10 (0.004)

−T− SEATING PLANE

D

G

H

−W−

DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

16

XXXX
XXXX
ALYW

1

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

DOCUMENT NUMBER:	98ASH70247A	
DESCRIPTION:	**TSSOP−16**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

◊

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NTE4028B NTE4514B NTE4515B NTE4543B NTE4547B NTE74LS249 NLV74HC4851AMNTWG MC74LVX257DG
M74HCT4851ADWR2G AP4373AW5-7-01 NL7SZ19DBVT1G MC74LVX257DTR2G 74VHC4066AFT(BJ) 74VHCT138AFT(BJ)
74HC158D.652 74HC4052D(BJ) 74VHC138MTC COMX-CAR-P1 JM38510/65852BEA 74VHC138MTCX 74HC138D(BJ)
NL7SZ19DFT2G 74AHCT138T16-13 74LCX138FT(AJ) 74LCX157FT(AJ) NL7SZ18MUR2G PCA9540BD,118 QS3VH16233PAG8
SNJ54HC251J SN54LS139AJ SN74CBTLV3257PWG4 SN74ALS156DR SN74AHCT139PWR 74HC251D.652 74HC257D.652