MC74LVX86

Quad 2-Input XOR Gate

With 5 V−Tolerant Inputs

The MC74LVX86 is an advanced high speed CMOS 2−input Exclusive−OR gate. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: t_{PD} = 5.8 ns (Typ) at V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
    Human Body Model > 2000 V;
    Machine Model > 200 V
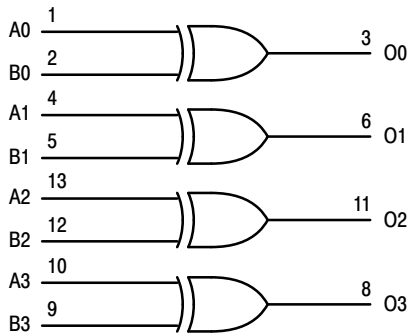- These Devices are Pb−Free and are RoHS Compliant

Figure 1. Logic Diagram

PIN NAMES

Pins	Function
An, Bn	Data Inputs
On	Outputs

FUNCTION TABLE

Inputs		Outputs
An	**Bn**	**On**
L	L	L
L	H	H
H	L	H
H	H	L

ON Semiconductor®

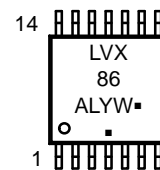| SOIC−14 NB	TSSOP−14
D SUFFIX	DT SUFFIX
CASE 751A	CASE 948G

PIN ASSIGNMENT
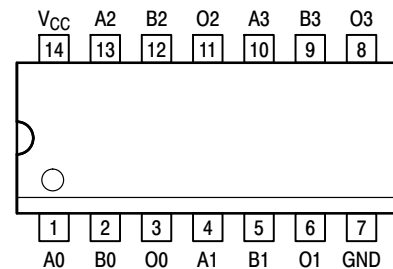
14−Lead (Top View)

MARKING DIAGRAMS
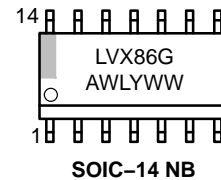
SOIC−14 NB

TSSOP−14

LVX86 = Specific Device Code
A   = Assembly Location
WL, L = Wafer Lot
Y   = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to +7.0	V
V_{in}	DC Input Voltage	−0.5 to +7.0	V
V_{out}	DC Output Voltage	−0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	−20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	−40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = −40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low−Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High−Level Output Voltage ($V_{in} = V_{IH}$ or V_{IL})	$I_{OH} = -50\mu A$ $I_{OH} = -50\mu A$ $I_{OH} = -4mA$	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low−Level Output Voltage ($V_{in} = V_{IH}$ or V_{IL})	$I_{OL} = 50\mu A$ $I_{OL} = 50\mu A$ $I_{OL} = 4mA$	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	3.6			2.0		20.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = −40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, Input to Output	V_{CC} = 2.7V	C_L = 15pF C_L = 50pF		7.5 10.0	14.5 18.0	1.0 1.0	17.5 21.0	ns
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		5.8 8.3	9.3 12.8	1.0 1.0	11.0 14.5	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1)	V_{CC} = 2.7V V_{CC} = 3.3 ± 0.3V	C_L = 50pF C_L = 50pF			1.5 1.5		1.5 1.5	ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter		T_A = 25°C			T_A = −40 to 85°C	Unit
		Min	Typ	Max	Min	Max	
Cin	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2)		18				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 3.3V, Measured in SOIC Package)

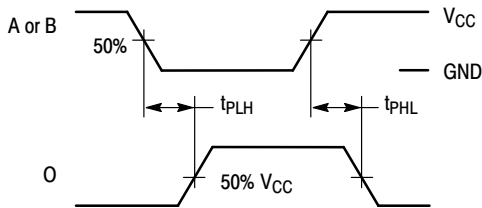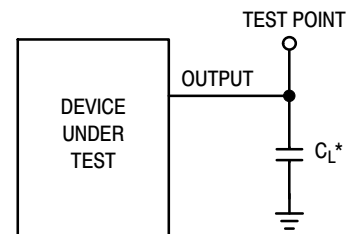| Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.3	−0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

Figure 2. Switching Waveforms

*Includes all probe and jig capacitance

Figure 3. Test Circuit

ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX86DR2G	SOIC–14 NB (Pb–Free)	2500 Tape & Reel
MC74LVX86DTR2G	TSSOP–14 (Pb–Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
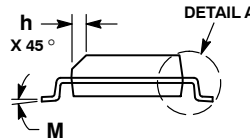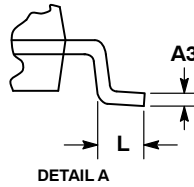
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®
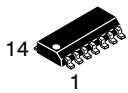
SOIC−14 NB
CASE 751A−03
ISSUE L

SCALE 1:1

DATE 03 FEB 2016

14

1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DETAIL A

SEATING PLANE

X 45°

DETAIL A

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT*

6.50

14X
1.18

1.27 PITCH

14X
0.58

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

14

XXXXXXXXXG
AWLYWW

1

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	
DESCRIPTION:	SOIC−14 NB	PAGE 1 OF 2

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 2 OF 2

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

14

SCALE 2:1

1

14X **K** REF

⊕ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

⌂ | 0.15 (0.006) | T | U Ⓢ

2X **L/2**

L

14   8

B
−U−

PIN 1
IDENT.

1   7

⌂ | 0.15 (0.006) | T | U Ⓢ

A

−V−

N

0.25 (0.010)

M

N

F

DETAIL E

K
K1

J J1

SECTION N−N

⌂ | 0.10 (0.004)

−T− SEATING
PLANE

C

D ◄ **G** ► ◄ **H** ►

DETAIL E

−W−

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

**GENERIC
MARKING DIAGRAM***

14

XXXX
XXXX
ALYW▪

1
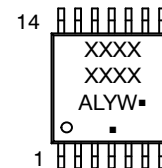
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

SOLDERING FOOTPRINT

7.06

1

0.65
PITCH

14X
0.36

14X
1.26

DIMENSIONS: MILLIMETERS
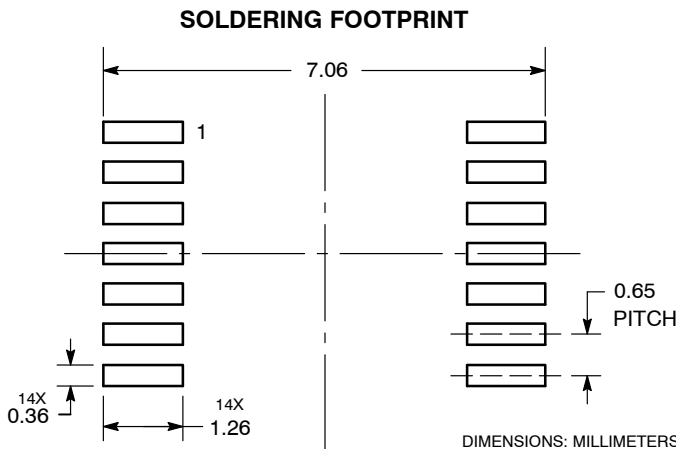
DOCUMENT NUMBER:	98ASH70246A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	TSSOP−14 WB		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

◊

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Logic Gates *category:*

Click to view products by ON Semiconductor *manufacturer:*

Other Similar products are found below :

74HC85N NLU1G32AMUTCG NLV7SZ58DFT2G CD4068BE NL17SG32P5T5G NL17SG86DFT2G NLV14001UBDR2G

NLX1G11AMUTCG NLX1G97MUTCG 74LS38 74LVC32ADTR2G MC74HCT20ADTR2G NLV17SZ00DFT2G NLV17SZ02DFT2G

NLV74HC02ADR2G 74HC32S14-13 74LS133 74LVC1G32Z-7 M38510/30402BDA 74LVC1G86Z-7 74LVC2G08RA3-7

NLV74HC08ADTR2G NLV74HC14ADR2G NLV74HC20ADR2G NLX2G86MUTCG 5962-8973601DA 74LVC2G02HD4-7

NLU1G00AMUTCG 74LVC2G32RA3-7 74LVC2G00HD4-7 NL17SG02P5T5G 74LVC2G00HK3-7 74LVC2G86HK3-7

NLX1G99DMUTWG NLVVHC1G00DFT2G NLVHC1G08DFT2G NLV7SZ57DFT2G NLV74VHC04DTR2G NLV27WZ86USG

NLV27WZ00USG NLU1G86CMUTCG NLU1G08CMUTCG NL17SZ32P5T5G NL17SZ00P5T5G NL17SH02P5T5G 74AUP2G00RA3-7

NLV74HC02ADTR2G NLX1G332CMUTCG NL17SG86P5T5G NL17SZ05P5T5G