MC74VHC1G09E

2-Input AND Gate with Open Drain Output

The MC74VHC1G09E is an advanced high speed CMOS 2−input AND gate with open drain output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including an open drain output which provides the capability to set output switching level. This allows the MC74VHC1G09E to be used to interface 5 V circuits to circuits of any voltage between V_{CC} and 5.5 V using an external resistor and power supply.

The MC74VHC1G09E input structure provides protection when voltages up to 5.5 V are applied, regardless of the supply voltage.

Features

- High Speed: t_{PD} = 4.3 ns (Typ) at V_{CC} = 5 V
- Low Internal Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 62; Equivalent Gates = 16
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

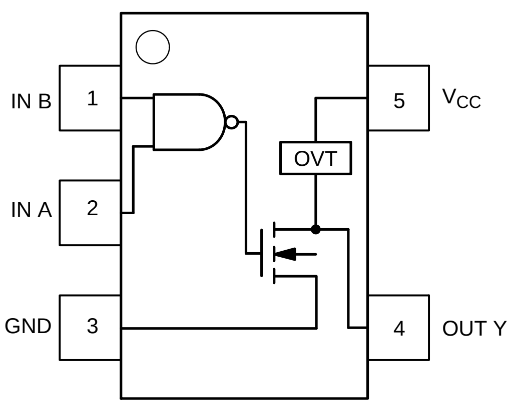

Figure 1. Pinout (Top View)

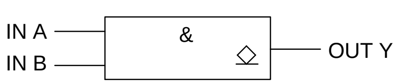

Figure 2. Logic Symbol

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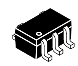
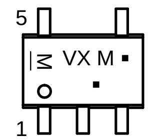
MARKING DIAGRAMS



SC−88A / SOT−353 / SC−70
DF SUFFIX
CASE 419A



VX = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT Y
5	V_{CC}

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage		−0.5 to +6.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current		+20	mA
I_{OUT}	DC Output Current, per Pin		+25	mA
I_{CC}	DC Supply Current, V_{CC} and GND		+50	mA
P_D	Power dissipation in still air		200	mW
θ_{JA}	Thermal resistance		333	°C/W
T_L	Lead temperature, 1 mm from case for 10 s		260	°C
T_J	Junction temperature under bias		+150	°C
T_{stg}	Storage temperature		−65 to +150	°C
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Charged Device Model (Note 2)	4000 1000	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 3)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22−A114−A
2. Tested to JESD22−C101−A
3. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		0.0	5.5	V
V_{OUT}	DC Output Voltage		0.0	7.0	V
T_A	Operating Temperature Range		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25°C$			$T_A \le 85°C$		$-55 \le T_A \le 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low−Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OL}	Maximum Low−Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\ \mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4$ mA $I_{OL} = 8$ mA	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5$ V or GND	0 to 5.5			±0.1		±1.0		±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			1.0		20		40	µA
I_{OFF}	Power Off−Output Leakage Current	$V_{OUT} = 5.5$ V $V_{IN} = 5.5$ V	0			0.25		2.5		5	µA

AC ELECTRICAL CHARACTERISTICS Input $t_r = t_f = 3.0$ ns

Symbol	Parameter	Test Conditions	$T_A = 25°C$			$T_A \le 85°C$		$-55 \le T_A \le 125°C$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PZL}	Maximum Output Enable Time, Input A or B to Y	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $R_L = 1000\ \Omega$ $C_L = 50$ pF		6.2 8.7	8.8 12.3		10.5 14.0		12.5 16.5	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $R_L = 1000\ \Omega$ $C_L = 50$ pF		4.3 5.8	5.9 7.9		7.0 9.0		9.0 11.0	
t_{PLZ}	Maximum Output Disable Time	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$ pF $R_L = 1000\ \Omega$		8.7	12.3		14.0		16.5	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF $R_L = 1000\ \Omega$		5.8	7.9		9.0		11.0	
C_{IN}	Maximum Input Capacitance			6.0	10		10		10	pF

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Note 4)	18	pF

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}{}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

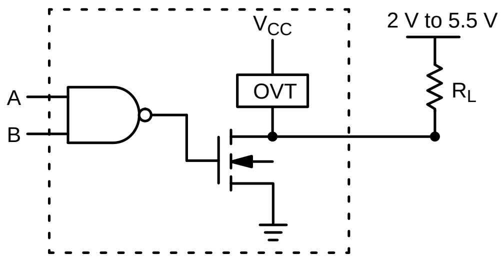


Figure 3. Output Voltage Mismatch Application

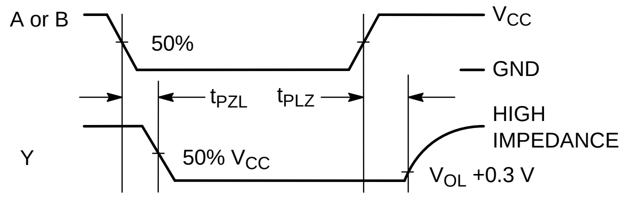
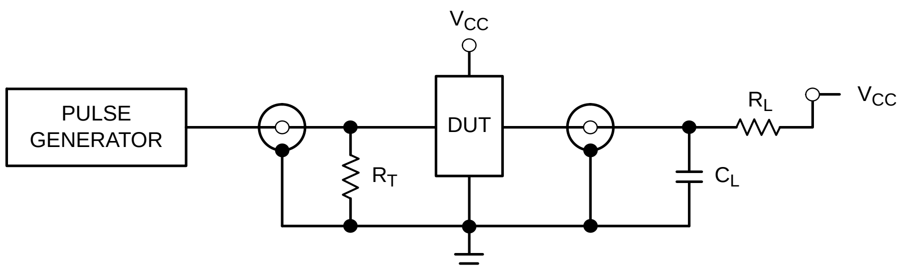


Figure 4. Switching Waveforms



C_L = 50 pF equivalent (Includes jig and probe capacitance)
R_L = 1000 Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 5. Test Circuit

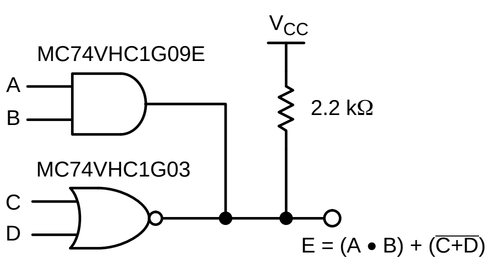


Figure 6. Complex Boolean Functions

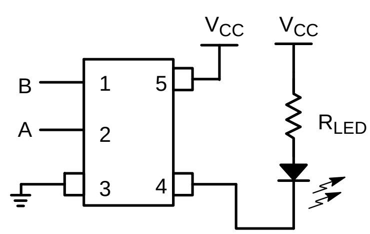


Figure 7. LED Driver

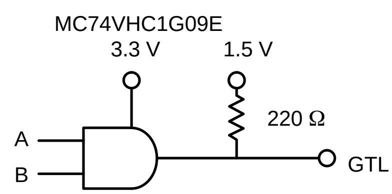


Figure 8. GTL Driver

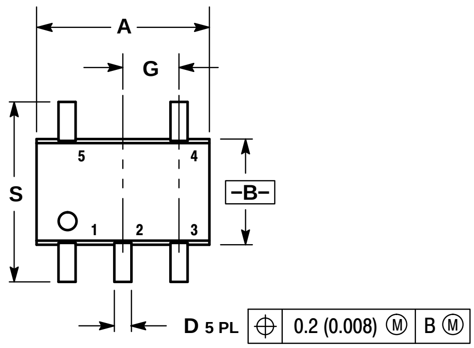
ORDERING INFORMATION

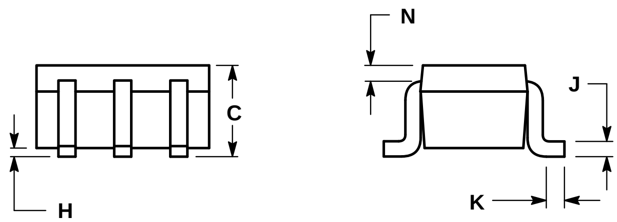
Device	Package	Shipping†
MC74VHC1G09EDFT2G	SC70−5 / SC−88A / SOT−353 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L

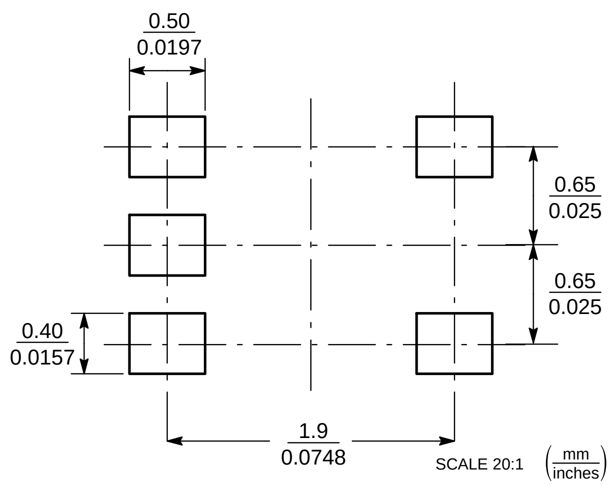




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDERING FOOTPRINT*



SCALE 20:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
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