Noninverting 3-State Buffer

MC74VHC1G125, MC74VHC1GT125

The MC74VHC1G125 / MC74VHC1GT125 is a single non−inverting 3−state buffer in tiny footprint packages. The MC74VHC1G125 has CMOS−level input thresholds while the MC74VHC1GT125 has TTL−level input thresholds.

The internal circuit is composed of three stages, including a buffered 3−state output which provides high noise immunity and stable output.

The input structures provide protection when voltages up to 5.5 V are applied, regardless of the supply voltage. This allows the device to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when V_{CC} = 0 V and when the output voltage exceeds V_{CC}. These input and output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- Designed for 2.0 V to 5.5 V V_{CC} Operation
- 3.5 ns t_{PD} at 5 V (typ)
- Inputs/Outputs Over−Voltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 8 mA at 3.0 V
- Available in SC−88A, SC−74A, TSOP−5, SOT−953 and UDFN6 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

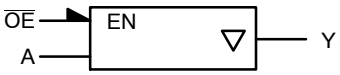
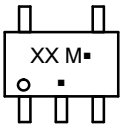


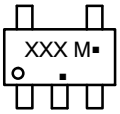
Figure 1. Logic Symbol

MARKING DIAGRAMS

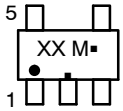
SC−88A
DF SUFFIX
CASE 419A



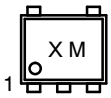
SC−74A
DBV SUFFIX
CASE 318BQ



TSOP−5
DT SUFFIX
CASE 483



SOT−953
P5 SUFFIX
CASE 527AE



UDFN6
1.45 x 1.0
CASE 517AQ

UDFN6
1.2 x 1.0
CASE 517AA

UDFN6
1.0 x 1.0
CASE 517BX

XX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 8 of this data sheet.

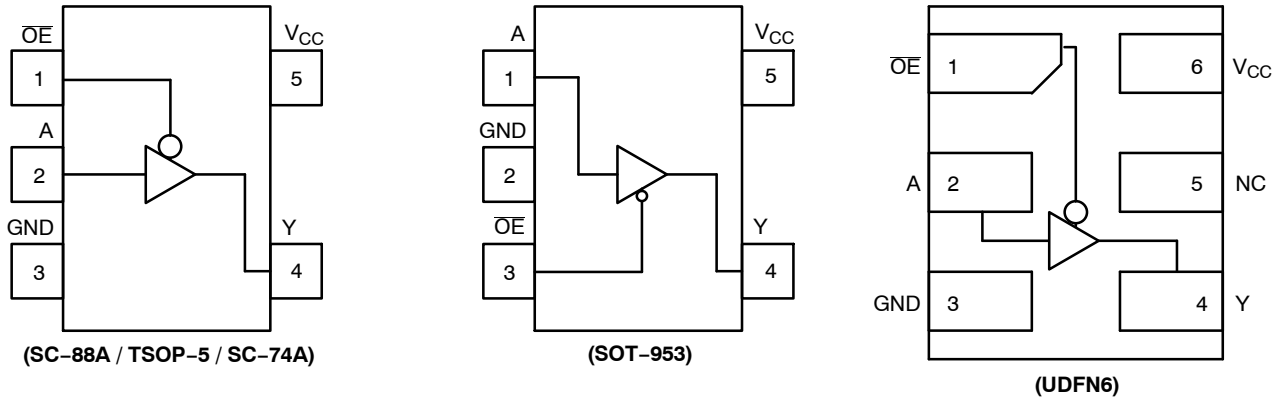


Figure 2. Pinout (Top View)

PIN ASSIGNMENT
(SC−88A / TSOP−5 / SC−74A)

Pin	Function
1	$\overline{OE}$
2	A
3	GND
4	Y
5	V_{CC}

PIN ASSIGNMENT (SOT−953)

Pin	Function
1	A
2	GND
3	$\overline{OE}$
4	Y
5	V_{CC}

PIN ASSIGNMENT (UDFN)

Pin	Function
1	$\overline{OE}$
2	A
3	GND
4	Y
5	NC
6	V_{CC}

FUNCTION TABLE

Input		Output
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

X = Don’t Care

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage	TSOP−5, SC−88A (NLV) SC−74A, SC−88A, UDFN6, SOT−953	−0.5 to +7.0 −0.5 to +6.5	V
V_{IN}	DC Input Voltage	TSOP−5, SC−88A (NLV) SC−74A, SC−88A, UDFN6, SOT−953	−0.5 to +7.0 −0.5 to +6.5	V
V_{OUT}	DC Output Voltage TSOP−5, SC−88A (NLV)	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +7.0 −0.5 to +7.0	V
	DC Output Voltage SC−74A, SC−88A, UDFN6, SOT−953	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +6.5 −0.5 to +6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−20	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−20	mA
I_{OUT}	DC Output Source/Sink Current		±25	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SC−88A SC−74A SOT−953 UDFN6	377 320 254 154	°C/W
P_D	Power Dissipation in Still Air	SC−88A SC−74A SOT−953 UDFN6	332 390 491 812	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm−by−1inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to ANSI/ESDA/JEDEC JS−001−2017. CDM tested to EIA/JESD22−C101−F. JEDEC recommends that ESD qualification to EIA/JESD22−A115−A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage	TSOP−5, SC−88A (NLV)	0	V_{CC}	V
	DC Output Voltage	SC−74A, SC−88A, UDFN6, SOT−953 Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	 0 0 0	 V_{CC} 5.5 5.5	
T_A	Operating Temperature Range		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	TSOP−5, SC−88A (NLV) V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 5.5 V	 0 0	 100 20	ns/V
	Input Rise and Fall Time	SC−74A, SC−88A, UDFN6, SOT−953 V_{CC} = 2.0 V V_{CC} = 2.3 V to 2.7 V V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 5.5 V	 0 0 0 0	 20 20 10 5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (MC74VHC1G125)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		−55°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High−Level Input Voltage		2.0	1.5	–	–	1.5	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	2.1	–	
			4.5	3.15	–	–	3.15	–	3.15	–	
			5.5	3.85	–	–	3.85	–	3.85	–	
V_{IL}	Low−Level Input Voltage		2.0	–	–	0.5	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	–	0.9	
			4.5	–	–	1.35	–	1.35	–	1.35	
			5.5	–	–	1.65	–	1.65	–	1.65	
V_{OH}	High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA I_{OH} = −8 mA	 2.0 3.0 4.5 3.0 4.5	 1.9 2.9 4.4 2.58 3.94	 2.0 3.0 4.5 – –	 – – – – –	 1.9 2.9 4.4 2.48 3.80	 – – – – –	 1.9 2.9 4.4 2.34 3.66	 – – – – –	V
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA I_{OL} = 8 mA	 2.0 3.0 4.5 3.0 4.5	 – – – – –	 0.0 0.0 0.0 – –	 0.1 0.1 0.1 0.36 0.36	 – – – – –	 0.1 0.1 0.1 0.44 0.44	 – – – – –	 0.1 0.1 0.1 0.52 0.52	V
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	2.0 to 5.5	–	–	±0.1	–	±1.0	–	±1.0	μA
I_{OZ}	3−State Output Leakage Current	V_{OUT} = 0 V to 5.5 V	5.5	–	–	±0.25	–	±2.5	–	±2.5	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 5.5 V or V_{OUT} = 5.5 V	0	–	–	1.0	–	10	–	10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5	–	–	1.0	–	20	–	40	μA

DC ELECTRICAL CHARACTERISTICS (MC74VHC1GT125)

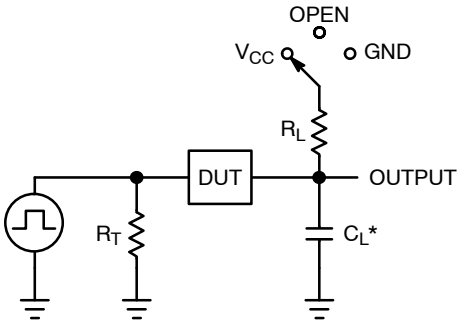
Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		−55°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High−Level Input Voltage		2.0	1.0	–	–	1.0	–	1.0	–	V
			3.0	1.4	–	–	1.4	–	1.4	–	
			4.5	2.0	–	–	2.0	–	2.0	–	
			5.5	2.0	–	–	2.0	–	2.0	–	
V_{IL}	Low−Level Input Voltage		2.0	–	–	0.28	–	0.28	–	0.28	V
			3.0	–	–	0.45	–	0.45	–	0.45	
			4.5	–	–	0.8	–	0.8	–	0.8	
			5.5	–	–	0.8	–	0.8	–	0.8	
V_{OH}	High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}									V
		I_{OH} = −50 μA	2.0	1.9	2.0	–	1.9	–	1.9	–	
		I_{OH} = −50 μA	3.0	2.9	3.0	–	2.9	–	2.9	–	
		I_{OH} = −50 μA	4.5	4.4	4.5	–	4.4	–	4.4	–	
		I_{OH} = −4 mA	3.0	2.58	–	–	2.48	–	2.34	–	
		I_{OH} = −8 mA	4.5	3.94	–	–	3.80	–	3.66	–	
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}									V
		I_{OL} = 50 μA	2.0	–	0.0	0.1	–	0.1	–	0.1	
		I_{OL} = 50 μA	3.0	–	0.0	0.1	–	0.1	–	0.1	
		I_{OL} = 50 μA	4.5	–	0.0	0.1	–	0.1	–	0.1	
		I_{OL} = 4 mA	3.0	–	–	0.36	–	0.44	–	0.52	
		I_{OL} = 8 mA	4.5	–	–	0.36	–	0.44	–	0.52	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	2.0 to 5.5	–	–	±0.1	–	±1.0	–	±1.0	μA
I_{OZ}	3−State Output Leakage Current	V_{OUT} = 0 V to 5.5 V	5.5	–	–	±0.25	–	±2.5	–	±2.5	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 5.5 V or V_{OUT} = 5.5 V	0	–	–	1.0	–	10	–	10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5	–	–	1.0	–	20	–	40	μA
I_{CCT}	Increase in Quiescent Supply Current per Input Pin	One Input: V_{IN} = 3.4 V; Other Input at V_{CC} or GND	5.5	–	–	1.35	–	1.5	–	1.65	mA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		−55°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, A to Y (Figures 3 and 4)	C_L = 15 pF	3.0 to 3.6	–	4.5	8.0	–	9.5	–	12.0	ns
		C_L = 50 pF		–	6.4	11.5	–	13.0	–	16.0	
		C_L = 15 pF	4.5 to 5.5	–	3.5	5.5	–	6.5	–	8.5	
		C_L = 50 pF		–	4.5	7.5	–	8.5	–	10.5	
t_{PZL}, t_{PZH}	Output Enable Time, $\overline{OE}$ to Y (Figures 3 and 4)	C_L = 15 pF	3.0 to 3.6	–	4.5	8.0	–	9.5	–	11.5	ns
		C_L = 50 pF		–	6.4	11.5	–	13.0	–	15.0	
		C_L = 15 pF	4.5 to 5.5	–	3.5	5.1	–	6.0	–	8.5	
		C_L = 50 pF		–	4.5	7.1	–	8.0	–	10.5	
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OE}$ to Y (Figures 3 and 4)	C_L = 15 pF	3.0 to 3.6	–	6.5	9.7	–	11.5	–	14.5	ns
		C_L = 50 pF		–	8.0	13.2	–	15.0	–	18.0	
		C_L = 15 pF	4.5 to 5.5	–	4.8	6.8	–	8.0	–	10.0	
		C_L = 50 pF		–	7.0	8.8	–	10.0	–	12.0	
C_{IN}	Input Capacitance			–	4.0	10	–	10	–	10	pF
C_{OUT}	Output Capacitance	Output in High Impedance State		–	6.0	–	–	–	–	–	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 5)	8.0	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.



C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Test	Switch Position	C_L, pF	R_L, Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	X
t_{PLZ} / t_{PZL}	V_{CC}		1 k
t_{PHZ} / t_{PZH}	GND		1 k

X = Don't Care

Figure 3. Test Circuit

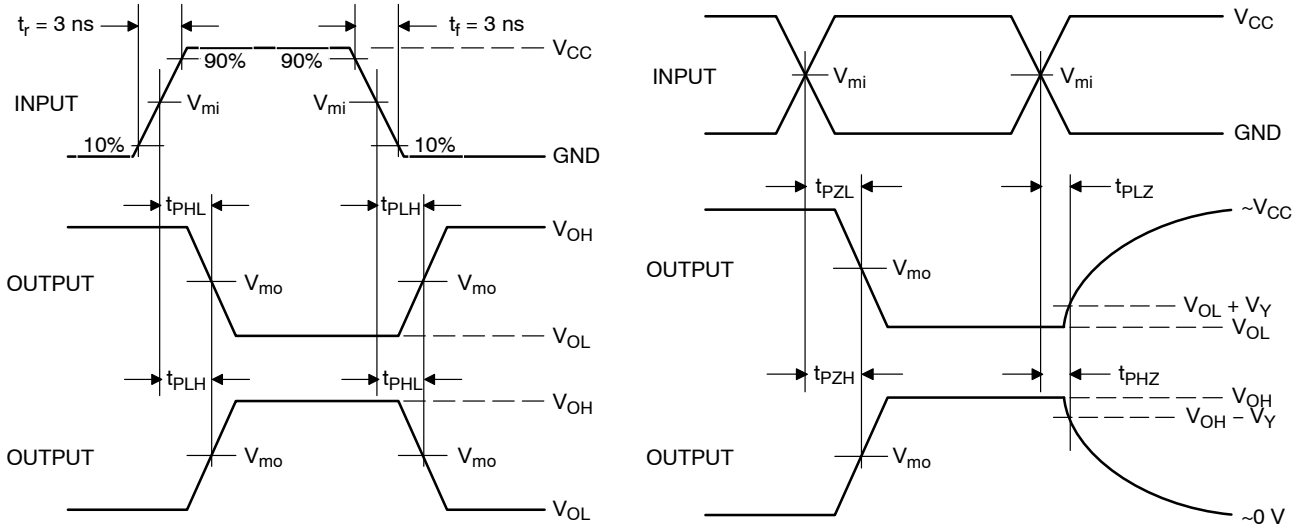


Figure 4. Switching Waveforms

V_{CC}, V	V_{mi}, V	V_{mo}, V		V_Y, V
		t_{PLH}, t_{PHL}	t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}	
3.0 to 3.6	V_{CC}/2	V_{CC}/2	V_{CC}/2	0.3
4.5 to 5.5	V_{CC}/2	V_{CC}/2	V_{CC}/2	0.3

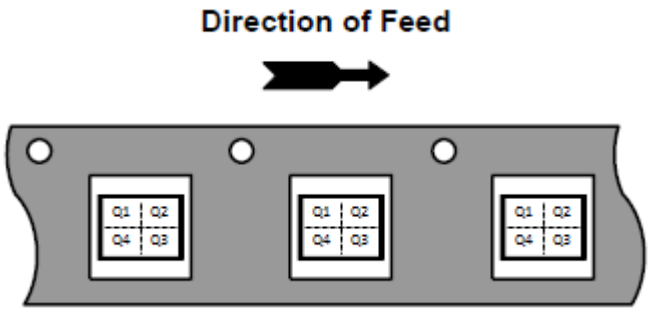
ORDERING INFORMATION

Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping†
M74VHC1G125DFT1G	SC−88A	W0	Q2	3000 / Tape & Reel
M74VHC1G125DFT2G	SC−88A	W0	Q4	3000 / Tape & Reel
NLVVHC1G125DFT1G*	SC−88A	W0	Q2	3000 / Tape & Reel
M74VHC1GT125DF1G	SC−88A	W1	Q2	3000 / Tape & Reel
M74VHC1GT125DF2G	SC−88A	W1	Q4	3000 / Tape & Reel
NLVVHC1GT125DF1G*	SC−88A	W1	Q2	3000 / Tape & Reel
NLVVHC1GT125DF2G*	SC−88A	W1	Q4	3000 / Tape & Reel
MC74VHC1G125DBVT1G	SC−74A	W0	Q4	3000 / Tape & Reel
MC74VHC1GT125DBVT1G	SC−74A	W1	Q4	3000 / Tape & Reel
M74VHC1G125DTT1G	TSOP−5	W0	Q4	3000 / Tape & Reel
M74VHC1GT125DT1G	TSOP−5	W1	Q4	3000 / Tape & Reel
NLVVHC1GT125DT1G*	TSOP−5	W1R	Q4	3000 / Tape & Reel
MC74VHC1G125P5T5G	SOT−953	T	Q2	8000 / Tape & Reel
MC74VHC1GT125P5T5G (In Development)	SOT−953	TBD	Q2	8000 / Tape & Reel
MC74VHC1G125MU1TCG (In Development)	UDFN6, 1.45 x 1.0, 0.5P	TBD	Q4	3000 / Tape & Reel
MC74VHC1GT125MU1TCG	UDFN6, 1.45 x 1.0, 0.5P	D	Q4	3000 / Tape & Reel
MC74VHC1GT125MU2TCG	UDFN6, 1.2 x 1.0, 0.4P	7	Q4	3000 / Tape & Reel
MC74VHC1G125MU3TCG (In Development)	UDFN6, 1.0 x 1.0, 0.35P	TBD	Q4	3000 / Tape & Reel
MC74VHC1GT125MU3TCG	UDFN6, 1.0 x 1.0, 0.35P	L	Q4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

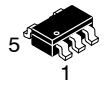
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel



MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

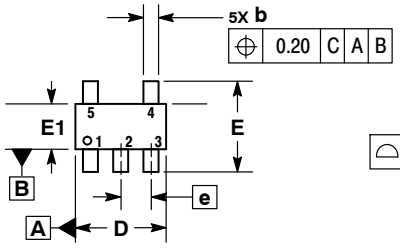
ON Semiconductor®

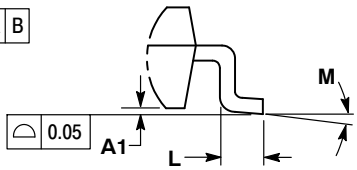


SCALE 2:1

SC−74A
CASE 318BQ
ISSUE B

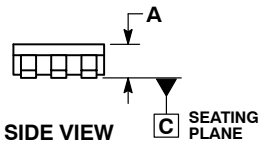
DATE 18 JAN 2018

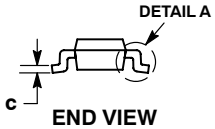




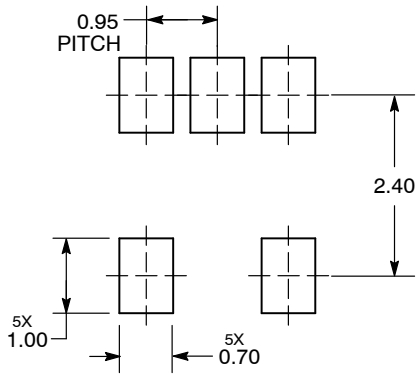
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.10
A1	0.01	0.10
b	0.25	0.50
c	0.10	0.26
D	2.85	3.15
E	2.50	3.00
E1	1.35	1.65
e	0.95 BSC	
L	0.20	0.60
M	0 °	10 °





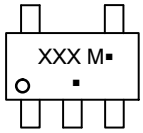
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON66279G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	SC−74A		PAGE 1 OF 1

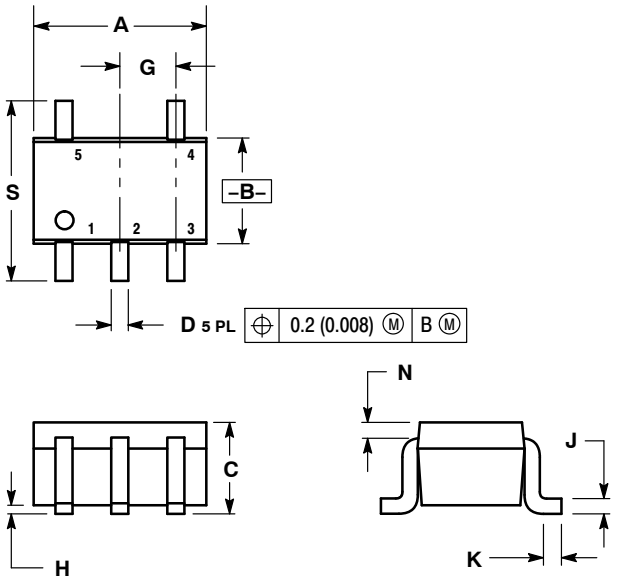
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L

SCALE 2:1

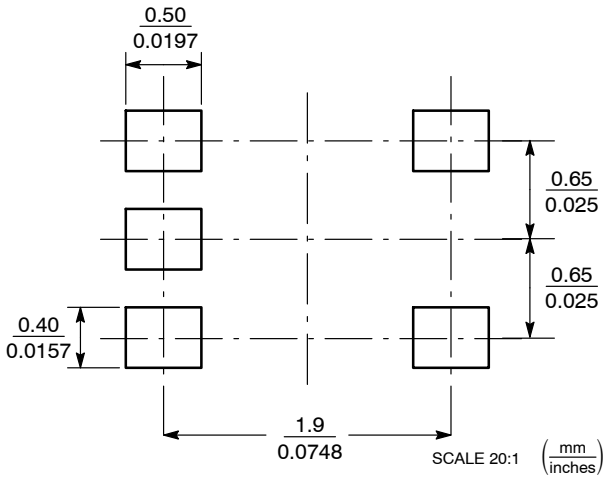
DATE 17 JAN 2013



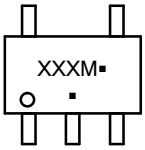
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

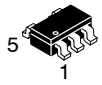
STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

DOCUMENT NUMBER:	98ASB42984B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

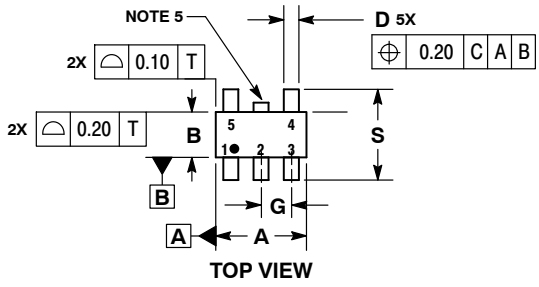
ON Semiconductor®



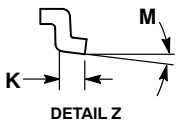
SCALE 2:1

TSOP−5
CASE 483
ISSUE N

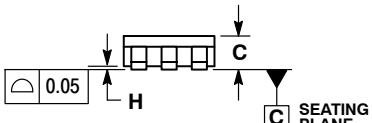
DATE 12 AUG 2020



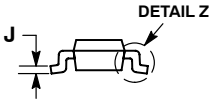
TOP VIEW



DETAIL Z



SIDE VIEW

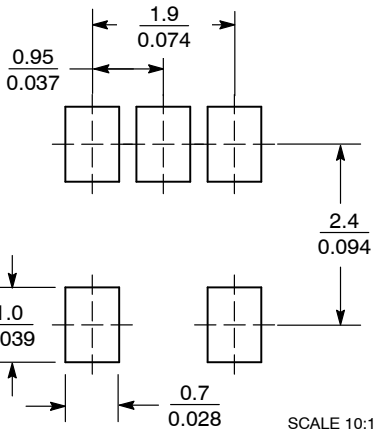


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

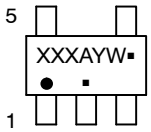
SOLDERING FOOTPRINT*



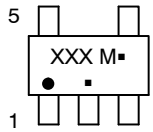
SCALE 10:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

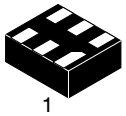
DOCUMENT NUMBER:	98ARB18753C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TSOP−5	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

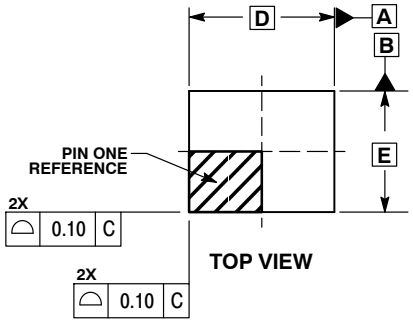
ON Semiconductor®

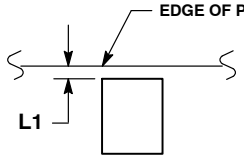
UDFN6, 1.2x1.0, 0.4P
CASE 517AA−01
ISSUE D

DATE 03 SEP 2010

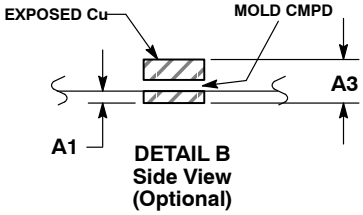


SCALE 8:1

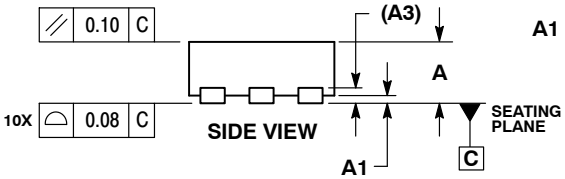


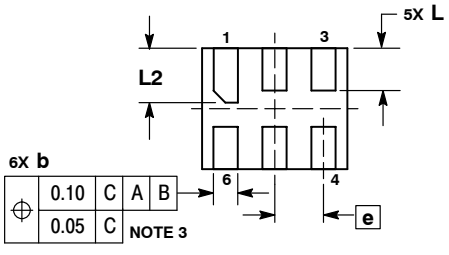


DETAIL A
Bottom View
(Optional)



DETAIL B
Side View
(Optional)





BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

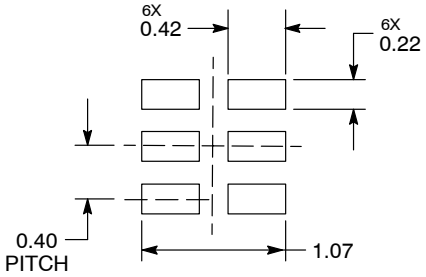
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.30	0.40
L1	0.00	0.15
L2	0.40	0.50

GENERIC MARKING DIAGRAM*

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

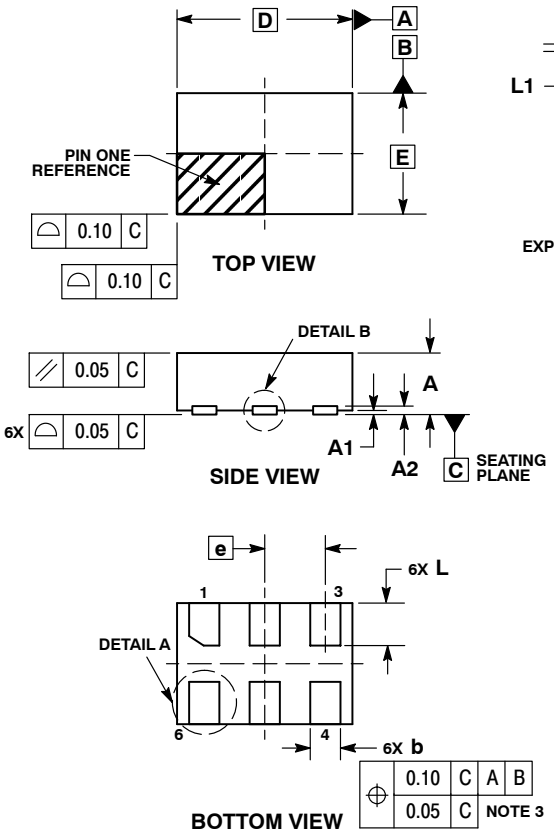
DOCUMENT NUMBER:	98AON22068D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	6 PIN UDFN, 1.2X1.0, 0.4P	PAGE 1 OF 1

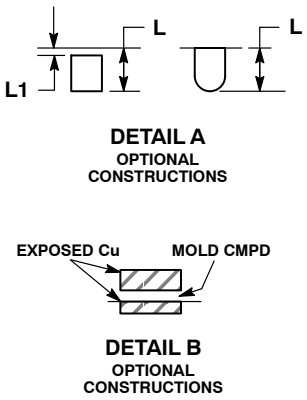
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

UDFN6, 1.45x1.0, 0.5P
CASE 517AQ
ISSUE O

SCALE 4:1

DATE 15 MAY 2008

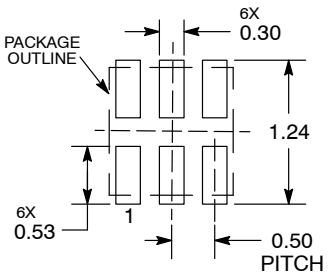




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	---	0.15

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

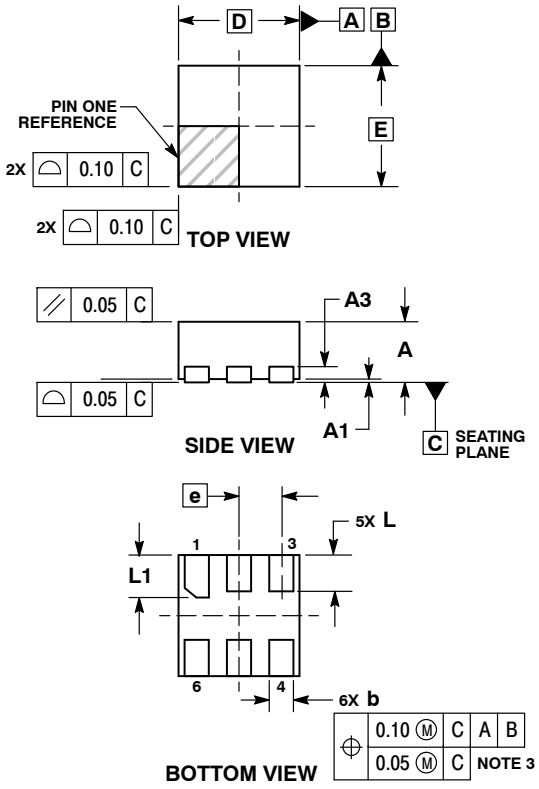
DOCUMENT NUMBER:	**98AON30313E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**UDFN6, 1.45x1.0, 0.5P**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

UDFN6, 1x1, 0.35P
CASE 517BX
ISSUE O

SCALE 4:1

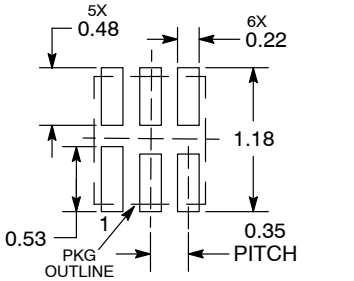
DATE 18 MAY 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

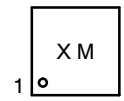
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON56787E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**UDFN6, 1x1, 0.35P**	**PAGE 1 OF 1**

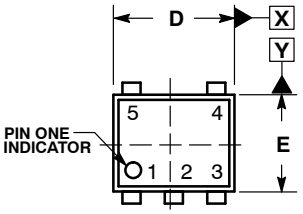
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

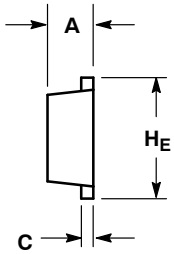
SOT−953
CASE 527AE
ISSUE E

DATE 02 AUG 2011

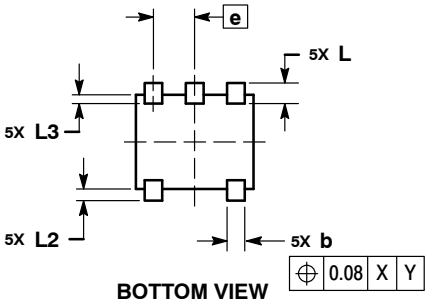
SCALE 4:1



TOP VIEW



SIDE VIEW

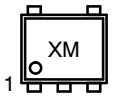


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H_E	0.95	1.00	1.05
L	0.175 REF		
L2	0.05	0.10	0.15
L3	−−−	−−−	0.15

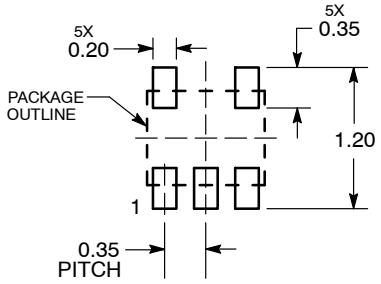
GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON26457D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT−953**	**PAGE 1 OF 1**

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