MC74VHC4316

Quad Analog Switch/ Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies

High−Performance Silicon−Gate CMOS

The MC74VHC4316 utilizes silicon−gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF−channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full analog power−supply range (from V_{CC} to V_{EE}).

The VHC4316 is similar in function to the metal−gate CMOS MC14016 and MC14066, and to the High−Speed CMOS HC4066A. Each device has four independent switches. The device control and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal−gate CMOS analog switches. Logic−level translators are provided so that the On/Off Control and Enable logic−level voltages need only be V_{CC} and GND, while the switch is passing signals ranging between V_{CC} and V_{EE}. When the Enable pin (active−low) is high, all four analog switches are turned off.

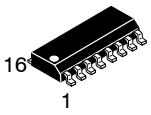
Features

- Logic−Level Translator for On/Off Control and Enable Inputs
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Diode Protection on All Inputs/Outputs
- Analog Power−Supply Voltage Range (V_{CC} − V_{EE}) = 2.0 to 12.0 V
- Digital (Control) Power−Supply Voltage Range (V_{CC} − GND) = 2.0 V to 6.0 V, Independent of V_{EE}
- Improved Linearity of ON Resistance
- Chip Complexity: 66 FETs or 16.5 Equivalent Gates
- These Devices are Pb−Free and are RoHS Compliant

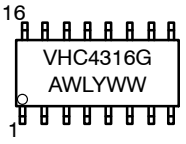
ON Semiconductor®

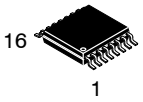
http://onsemi.com

MARKING DIAGRAMS

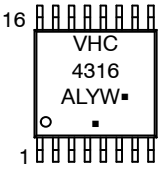


SOIC−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



A	=	Assembly Location
WL, L	=	Wafer Lot
Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
MC74VHC4316DG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74VHC4316DR2G	SOIC−16 (Pb−Free)	2500/Tape&Reel
MC74VHC4316DTG	TSSOP16 (Pb−Free)	96 Units / Rail
MC74VHC4316DTR2G	TSSOP16 (Pb−Free)	2500/Tape&Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

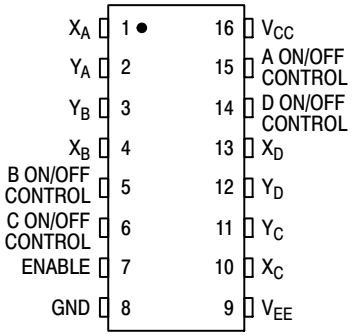


Figure 1. Pin Assignment

FUNCTION TABLE

Inputs		State of Analog Switch
Enable	**On/Off Control**	
L	H	On
L	L	Off
H	X	Off

X = Don't Care.

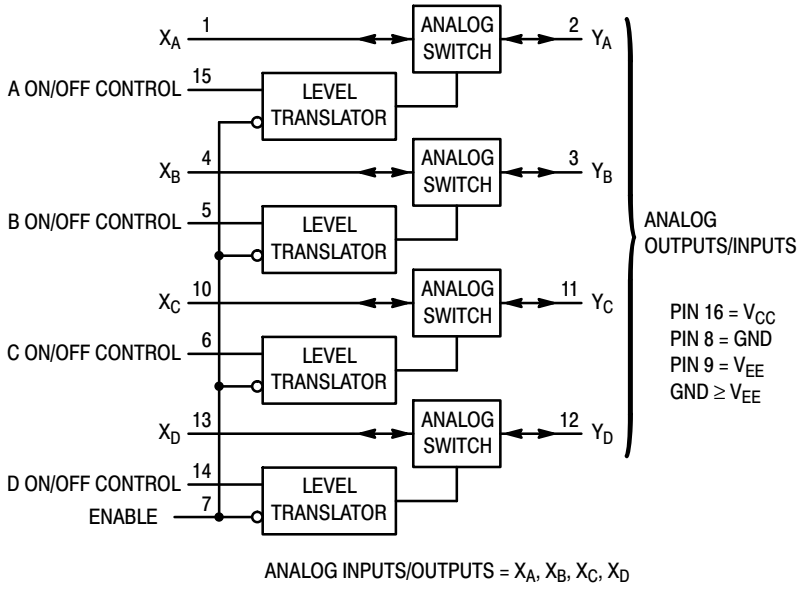


Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage	(Ref. to GND) (Ref. to V_{EE})	− 0.5 to + 7.0 − 0.5 to + 14.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)		− 7.0 to + 0.5	V
V_{IS}	Analog Input Voltage		V_{EE} − 0.5 to V_{CC} + 0.5	V
V_{in}	DC Input Voltage (Ref. to GND)		− 0.5 to V_{CC} + 0.5	V
I	DC Current Into or Out of Any Pin		± 25	mA
P_D	Power Dissipation in Still Air	SOIC Package* TSSOP Package*	500 450	mW
T_{stg}	Storage Temperature		− 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package)		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*Derating − SOIC Package: − 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND)		2.0	6.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)		− 6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Ref. to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		−	1.2	V
T_A	Operating Temperature, All Package Types		− 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Control or Enable Inputs) (Figure 10)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE} = GND Except Where Noted

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Voltage, Control or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Voltage, Control or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
I_{in}	Maximum Input Leakage Current, Control or Enable Inputs	V_{in} = V_{CC} or GND V_{EE} = – 6.0 V	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND V_{IO} = 0 V V_{EE} = GND V_{EE} = – 6.0	 6.0 6.0	 2 4	 20 40	 40 160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to V_{EE})

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum “ON” Resistance	V_{in} = V_{IH} V_{IS} = V_{CC} to V_{EE} I_S ≤ 2.0 mA	2.0* 4 5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	– 160 90 90	– 200 110 110	– 240 130 130	Ω
		V_{in} = V_{IH} V_{IS} = V_{CC} or V_{EE} (Endpoints) I_S ≤ 2.0 mA	2.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	– 90 70 70	– 115 90 90	– 140 105 105	
ΔR_{on}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V_{in} = V_{IH} V_{IS} = 1/2 (V_{CC} – V_{EE}) I_S ≤ 2.0 mA	2.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	– 20 15 15	– 25 20 20	– 30 25 25	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	V_{in} = V_{IL} V_{IO} = V_{CC} or V_{EE} Switch Off (Figure 3)	6.0	– 6.0	0.1	0.5	1.0	μA
I_{on}	Maximum On–Channel Leakage Current, Any One Channel	V_{in} = V_{IH} V_{IS} = V_{CC} or V_{EE} (Figure 4)	6.0	– 6.0	0.1	0.5	1.0	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

*At supply voltage (V_{CC} – V_{EE}) approaching 2.0 V the analog switch–on resistance becomes extremely non–linear. Therefore, for low–voltage operation, it is recommended that these devices only be used to control digital signals.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Control or Enable $t_r = t_f$ = 6 ns, V_{EE} = GND)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0 4.5 6.0	40 6 5	50 8 7	60 9 8	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0 4.5 6.0	130 40 30	160 50 40	200 60 50	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0 4.5 6.0	140 40 30	175 50 40	250 60 50	ns
C	Maximum Capacitance — ON/OFF Control and Enable Inputs	–	10	10	10	pF
	Control Input = GND Analog I/O Feedthrough	 – –	 35 1.0	 35 1.0	 35 1.0	

1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Switch) (Figure 13)*	15	pF

*Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 5)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads – 3 dB R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	150 160 160	MHz
–	Off–Channel Feedthrough Isolation (Figure 6)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 50 – 50 – 50	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 40 – 40 – 40	
–	Feedthrough Noise, Control to Switch (Figure 7)	V_{in} ≤ 1 MHz Square Wave ($t_r = t_f$ = 6 ns) Adjust R_L at Setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	60 130 200	mV_{PP}
		R_L = 10 kΩ, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	30 65 100	
–	Crosstalk Between Any Two Switches (Figure 12)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 70 – 70 – 70	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 80 – 80 – 80	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF THD = $THD_{Measured}$ – THD_{Source} V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 8.0 V_{PP} sine wave V_{IS} = 11.0 V_{PP} sine wave	 2.25 4.50 6.00	 – 2.25 – 4.50 – 6.00	 0.10 0.06 0.04	%

*Limits not tested. Determined by design and verified by qualification.

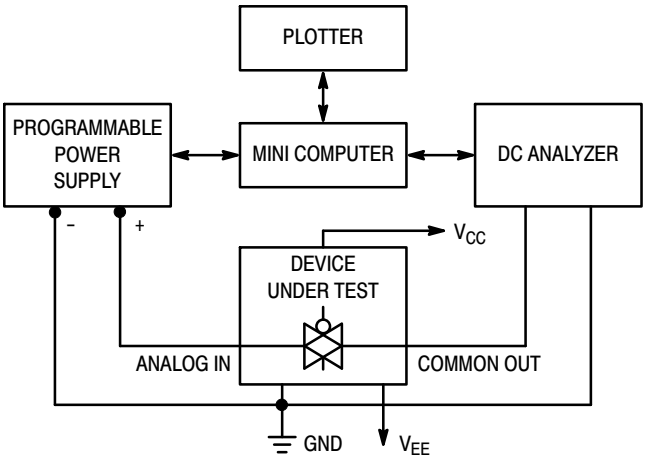


Figure 1. On Resistance Test Set–Up

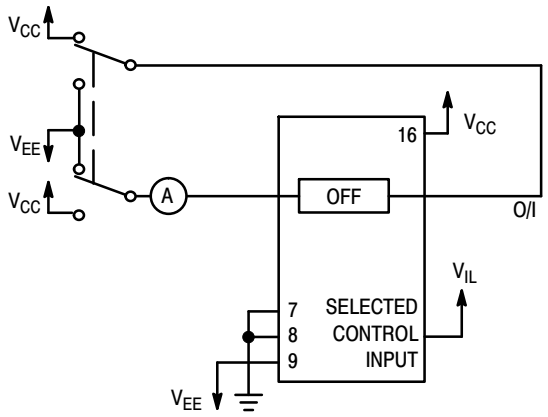


Figure 2. Maximum Off Channel Leakage Current, Any One Channel, Test Set−Up

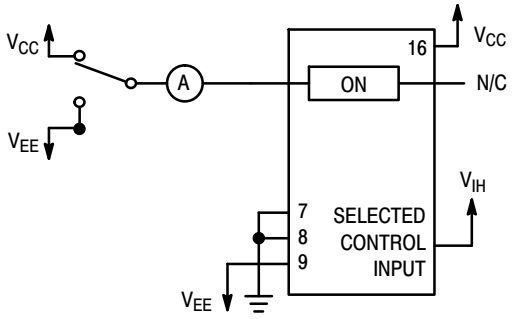
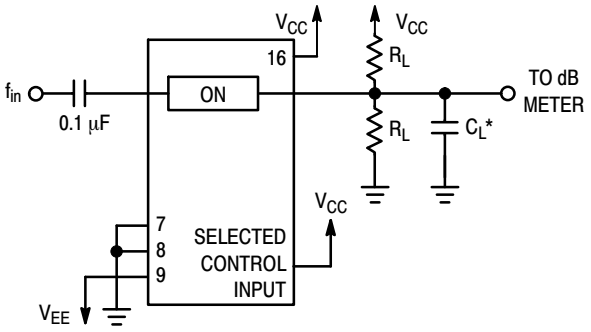
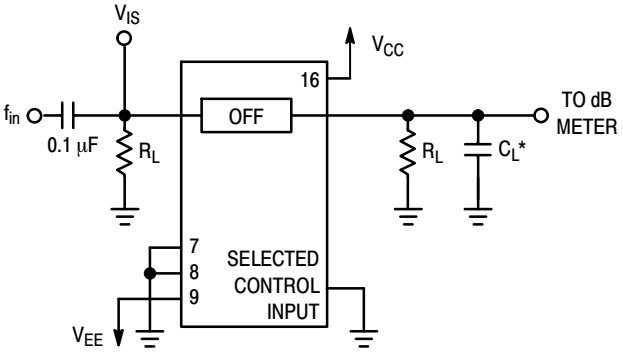


Figure 3. Maximum On Channel Leakage Current, Test Set−Up



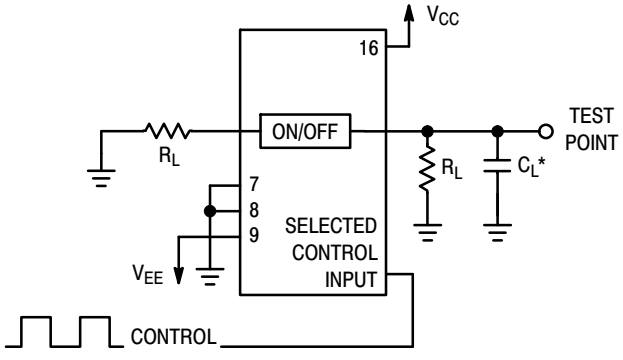
*Includes all probe and jig capacitance.

Figure 4. Maximum On−Channel Bandwidth Test Set−Up



*Includes all probe and jig capacitance.

Figure 5. Off−Channel Feedthrough Isolation, Test Set−Up



*Includes all probe and jig capacitance.

Figure 6. Feedthrough Noise, Control to Analog Out, Test Set−Up

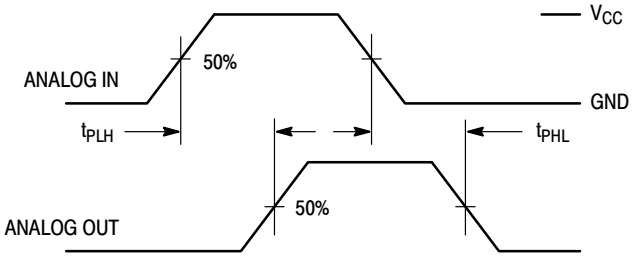
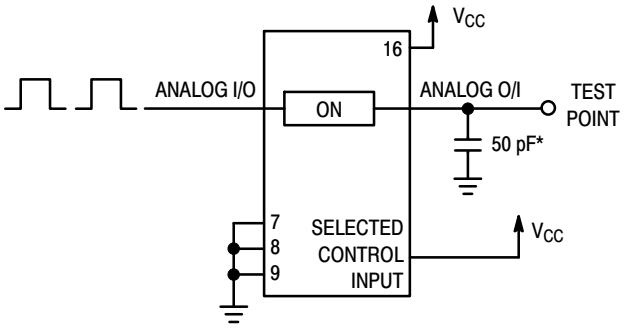


Figure 7. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 8. Propagation Delay Test Set−Up

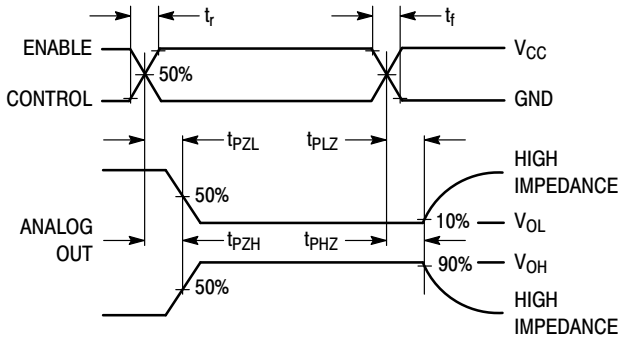
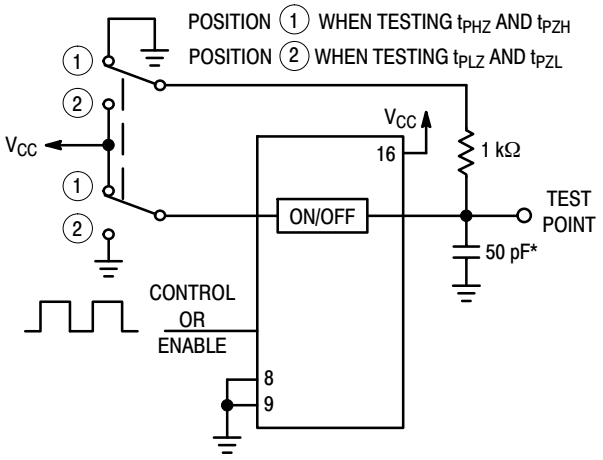
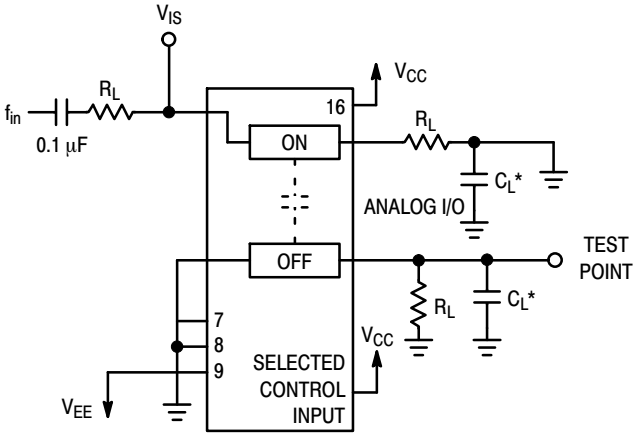


Figure 9. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 10. Propagation Delay Test Set−Up



*Includes all probe and jig capacitance.

Figure 11. Crosstalk Between Any Two Switches, Test Set−Up (Adjacent Channels Used)

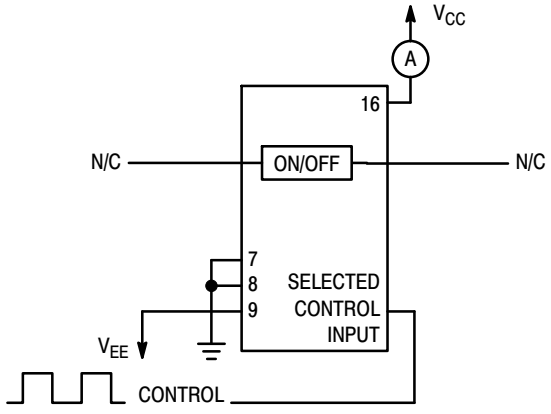
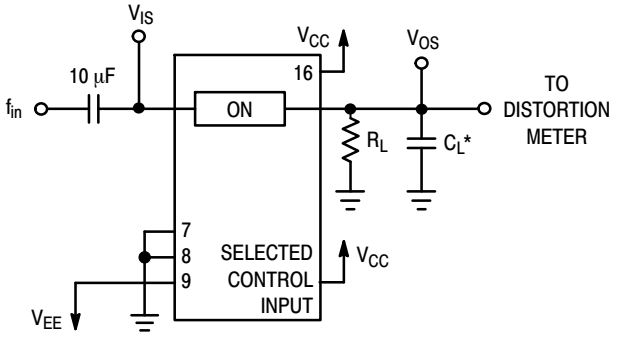


Figure 12. Power Dissipation Capacitance Test Set−Up



*Includes all probe and jig capacitance.

Figure 13. Total Harmonic Distortion, Test Set−Up

APPLICATIONS INFORMATION

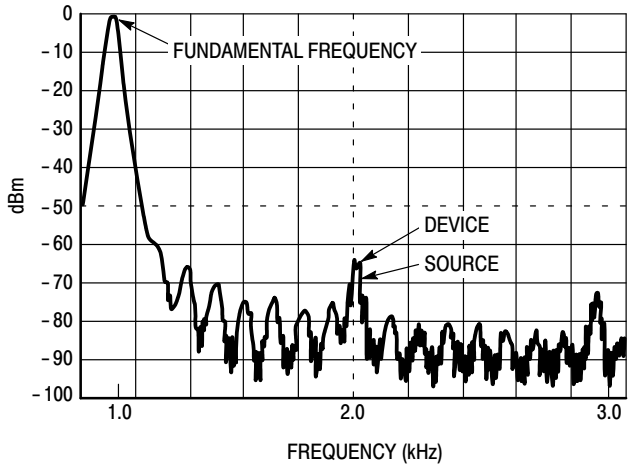


Figure 14. Plot, Harmonic Distortion

The Enable and Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or V_{EE} through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In the example below, the difference between V_{CC} and V_{EE} is 12 V. Therefore, using the configuration in Figure 15, a maximum analog signal of twelve volts peak−to−peak can be controlled.

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 16. These diodes should be small signal, fast turn−on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with MOSORBs (MOSORB™ is an acronym for high current surge protectors). MOSORBs are fast turn−on devices ideally suited for precise dc protection with no inherent wear out mechanism.

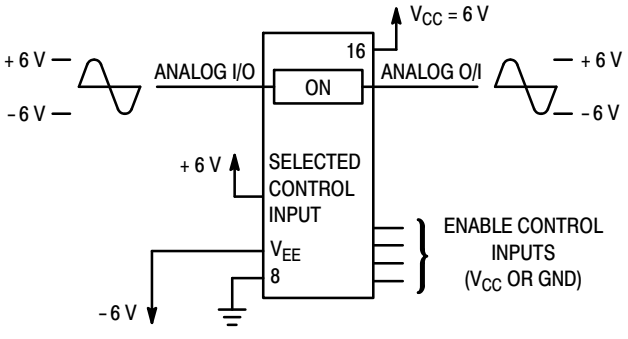


Figure 15.

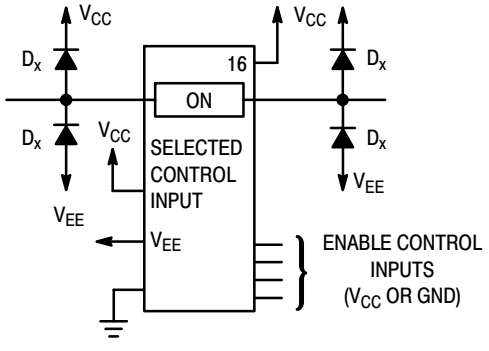
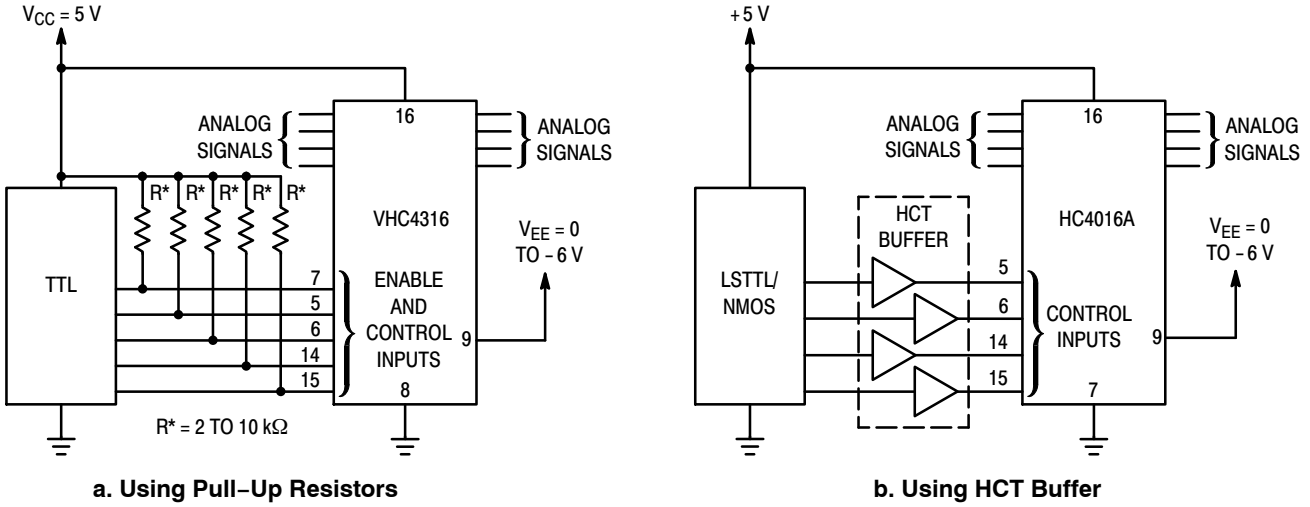


Figure 16. Transient Suppressor Application



a. Using Pull−Up Resistors **b. Using HCT Buffer**

Figure 17. LSTTL/NMOS to HCMOS Interface

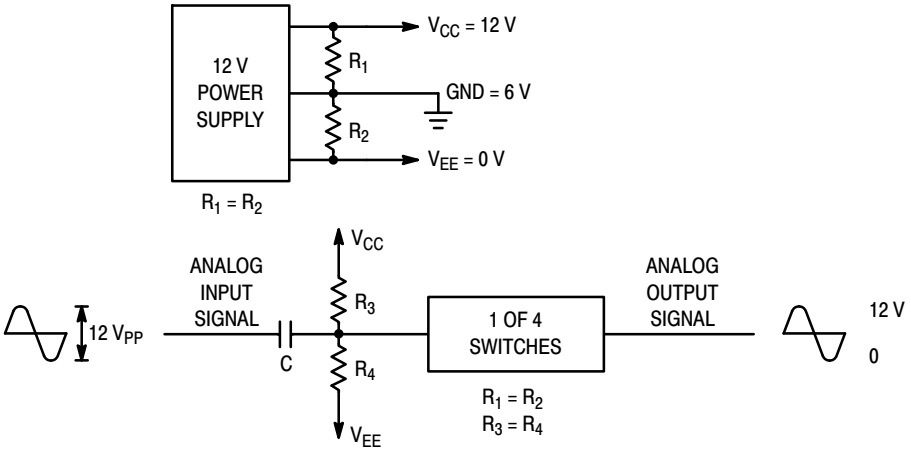


Figure 18. Switching a 0−to−12 V Signal Using a Single Power Supply (GND ≠ 0 V)

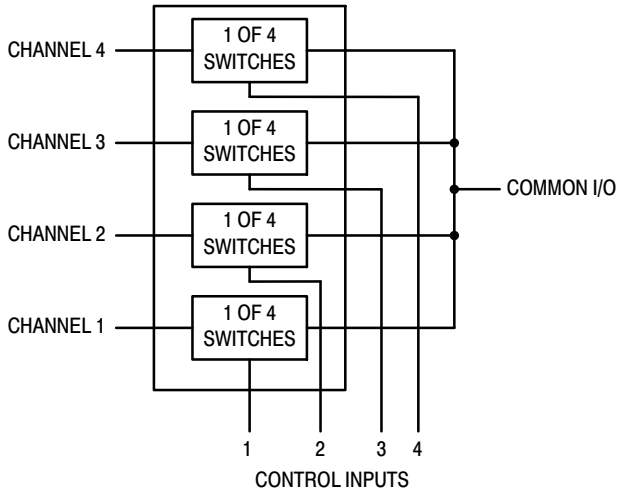


Figure 19. 4−Input Multiplexer

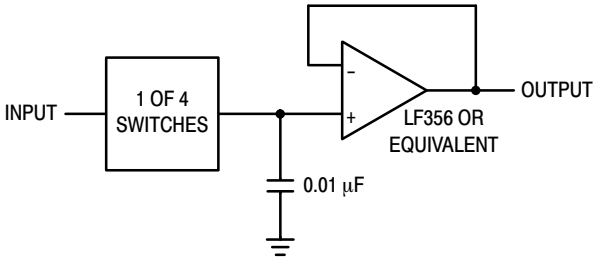


Figure 20. Sample/Hold Amplifier

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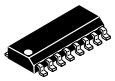
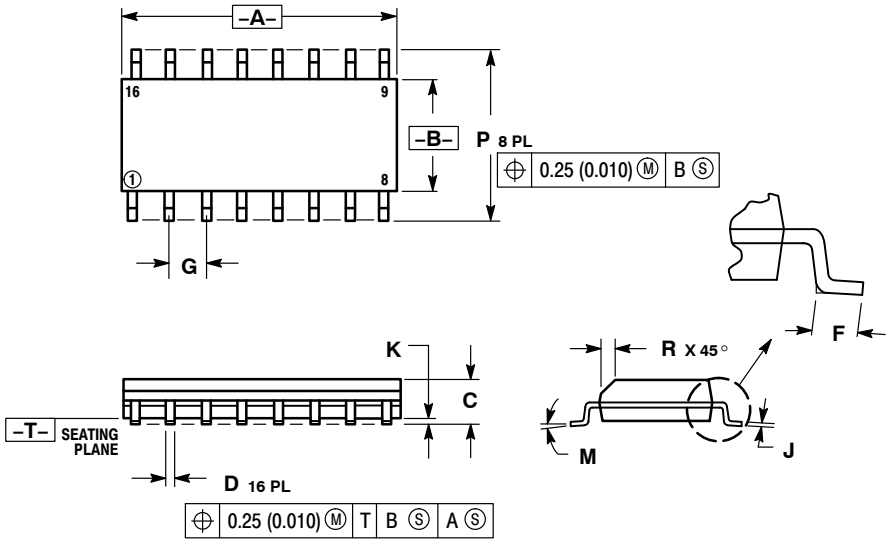
ISSUE K

DATE 29 DEC 2006



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

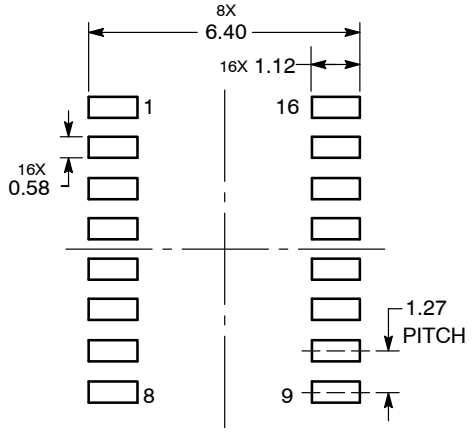
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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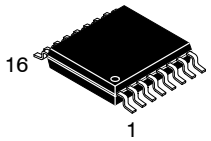
DESCRIPTION:	SOIC−16	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

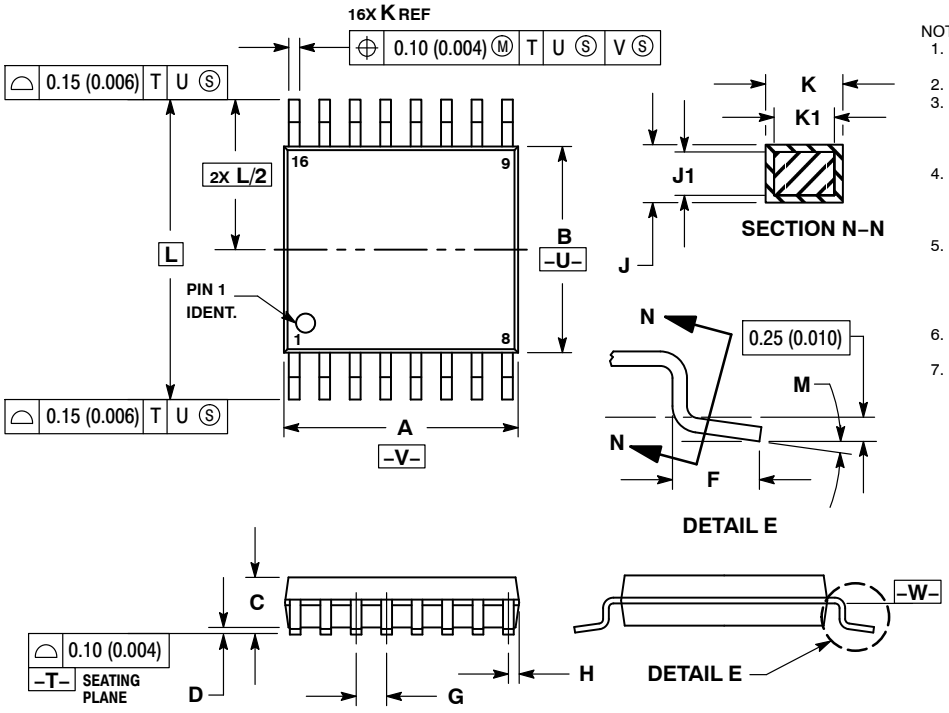
ON Semiconductor®



SCALE 2:1

TSSOP−16
CASE 948F−01
ISSUE B

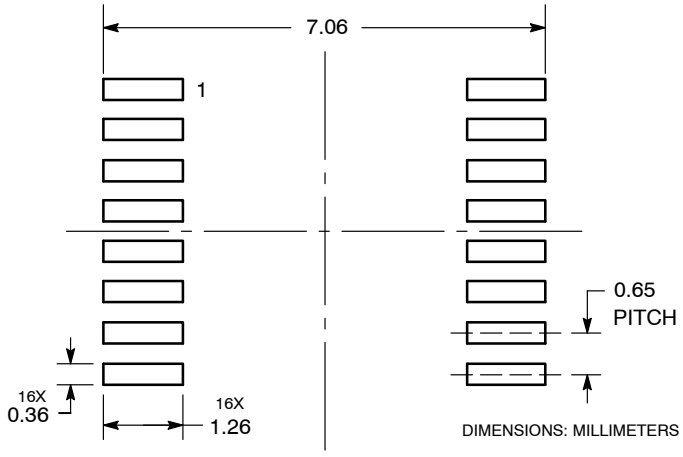
DATE 19 OCT 2006



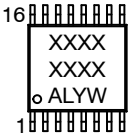
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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