MJ15022 (NPN), MJ15024 (NPN)

Silicon Power Transistors

The MJ15022 and MJ15024 are power transistors designed for high power audio, disk head positioners and other linear applications.

Features

- High Safe Operating Area
- High DC Current Gain
- These Devices are Pb-Free and are RoHS Compliant*
- Complementary to MJ15023 (PNP), MJ15025 (PNP)

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|-----------------------------------|-------------|-----------|
| Collector–Emitter Voltage MJ15022 MJ15024 | V _{CEO} | 200 250 | Vdc |
| Collector-Base Voltage MJ15022 MJ15024 | V _{CBO} | 350 400 | Vdc |
| Emitter-Base Voltage | V _{EBO} | 5 | Vdc |
| Collector-Emitter Voltage | V _{CEX} | 400 | Vdc |
| Collector Current – Continuous | Ι _C | 16 | Adc |
| Collector Current – Peak (Note 1) | I _{CM} | 30 | Adc |
| Base Current – Continuous | Ι _Β | 5 | Adc |
| Total Device Dissipation @ T _C = 25°C Derate above 25°C | PD | 250 1.43 | W W/°C |
| Operating and Storage Junction Temperature Range | T _J , T _{stg} | -65 to +200 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

THERMAL CHARACTERISTICS

| Characteristics | Symbol | Мах | Unit |
|--------------------------------------|-----------------------|------|------|
| Thermal Resistance, Junction-to-Case | $R_{	extsf{	heta}JC}$ | 0.70 | °C/W |

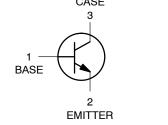


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16 AMPERES SILICON POWER TRANSISTORS 200 – 250 VOLTS, 250 WATTS

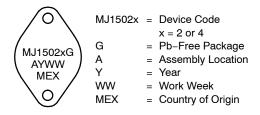
CASE







MARKING DIAGRAM



ORDERING INFORMATION

| Device | Package | Shipping |
|----------|---------------------|------------------|
| MJ15022G | TO–204 (Pb–Free) | 100 Units / Tray |
| MJ15024G | TO–204 (Pb–Free) | 100 Units / Tray |

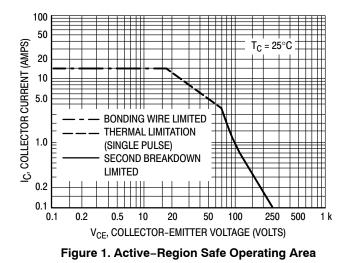
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MJ15022 (NPN), MJ15024 (NPN)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|--------------------|-----------------------|------------|------------|------|
| OFF CHARACTERISTICS | | | | | |
| Collector-Emitter Sustaining Voltage (Note 2) $(I_C = 100 \text{ mAdc}, I_B = 0)$ | MJ15022 MJ15024 | V _{CEO(sus)} | 200 250 | | _ |
| Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc) | MJ15022 MJ15024 | I _{CEX} | - | 250 250 | μAdc |
| Collector Cutoff Current ($V_{CE} = 150 \text{ Vdc}, I_B = 0$) ($V_{CE} = 200 \text{ vdc}, I_B = 0$) | MJ15022 MJ15024 | I _{CEO} | | 500 500 | μAdc |
| Emitter Cutoff Current ($V_{CE} = 5 \text{ Vdc}, I_B = 0$) | | I _{EBO} | - | 500 | μAdc |
| SECOND BREAKDOWN | | | | | |
| Second Breakdown Collector Current with Base Forward Biased (V _{CE} = 50 Vdc, t = 0.5 s (non-repetitive)) (V _{CE} = 80 Vdc, t = 0.5 s (non-repetitive)) | | I _{S/b} | 5 2 | | Adc |
| ON CHARACTERISTICS | | | | | - |
| DC Current Gain ($I_C = 8 \text{ Adc}, V_{CE} = 4 \text{ Vdc}$) ($I_C = 16 \text{ Adc}, V_{CE} = 4 \text{ Vdc}$) | | h _{FE} | 15 5 | 60 - | _ |
| Collector–Emitter Saturation Voltage ($I_C = 8 \text{ Adc}, I_B = 0.8 \text{ Adc}$) ($I_C = 16 \text{ Adc}, I_B = 3.2 \text{ Adc}$) | | V _{CE(sat)} | | 1.4 4.0 | Vdc |
| Base–Emitter On Voltage (I _C = 8 Adc, V _{CE} = 4 Vdc) | | $V_{\text{BE(on)}}$ | _ | 2.2 | Vdc |
| DYNAMIC CHARACTERISTICS | | | - | | |
| Current–Gain – Bandwidth Product (I _C = 1 Adc, V _{CE} = 10 Vdc, f _{test} = 1 MHz) | | fT | 4 | - | MHz |
| Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1 MHz) | | C _{ob} | - | 500 | pF |

2. Pulse Test: Pulse Width = 300 μ s, Duty Cycle \leq 2%.

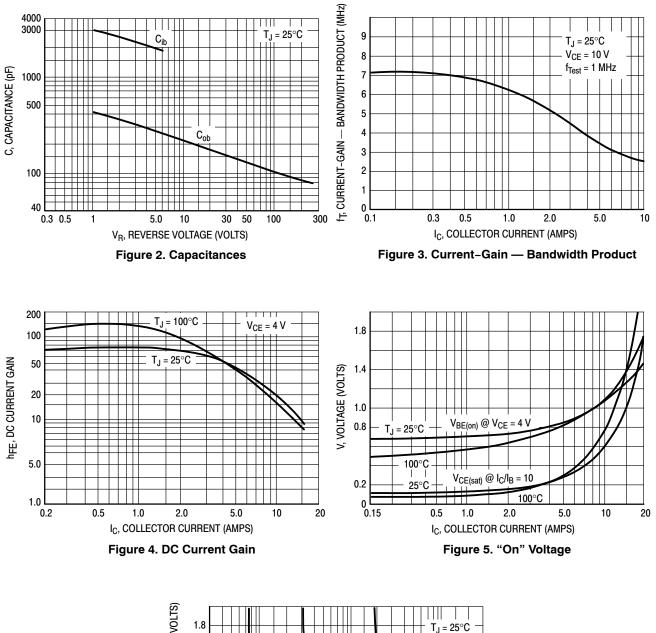


There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 200^{\circ}$ C; T_{C} is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values Ion than the limitations imposed by second breakdown.

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TYPICAL CHARACTERISTICS



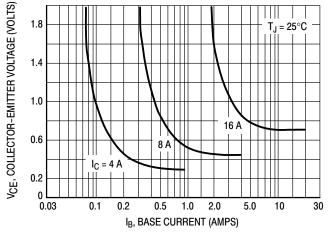


Figure 6. Collector Saturation Region

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



| DIMENSIONS | | | |
|--|---|--|--------------------|
| SCALE 1:1 | TO–204 (TO–3) CASE 1–07 ISSUE Z |) | DATE 05/18/1988 |
| $ \begin{array}{c} $ | $ \begin{array}{c} $ | NOTES: 1. DIMENSIONING AND TC Y14.5M, 1982. 2. CONTROLLING DIMENS 3. ALL RULES AND NOTES REFERENCED TO-204A MIN MAX A 1.550 REF B 1.050 C 0.250 0.335 D 0.038 0.043 E 0.055 0.070 G 0.430 BSC H 0.215 BSC K 0.440 0.480 L 0.665 BSC N 0.830 Q 0.151 0.165 U 1.187 BSC V 0.131 0.188 | ION: INCH. |
| STYLE 1: PIN 1. BASE 2. EMITTER CASE: COLLECTOR STYLE 6: PIN 1. GATE 2. EMITTER CASE: COLLECTOR | STYLE 2: STYLE 3: PIN 1. BASE PIN 1. GATE 2. COLLECTOR 2. SOURCE CASE: EMITTER CASE: DRAIN STYLE 7: STYLE 8: PIN 1. ANODE PIN 1. CATHODE #1 2. OPEN 2. CATHODE #2 CASE: CATHODE CASE: ANODE | STYLE 4: STYLE 5: PIN 1. GROUND 2. INPUT CASE: OUTPUT STYLE 9: PIN 1. ANODE #1 2. ANODE #2 CASE: CATHODE | E AL TRIP/DELAY |

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