

# MJF122, MJF127

## Complementary Power Darlington

### For Isolated Package Applications

Designed for general-purpose amplifiers and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

#### Features

- Electrically Similar to the Popular TIP122 and TIP127
- 100 V<sub>CEO(sus)</sub>
- 5.0 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High DC Current Gain – 2000 (Min) @ I<sub>C</sub> = 3 Adc
- UL Recognized, File #E69369, to 3500 V<sub>RMS</sub> Isolation
- Pb-Free Packages are Available\*

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	100	Vdc
Collector-Base Voltage	V <sub>CB</sub>	100	Vdc
Emitter-Base Voltage	V <sub>EB</sub>	5	Vdc
RMS Isolation Voltage (Note 1) (t = 0.3 sec, R.H. ≤ 30%, T <sub>A</sub> = 25°C) Per Figure 14	V <sub>ISOL</sub>	4500	V <sub>RMS</sub>
Collector Current – Continuous Peak	I <sub>C</sub>	5 8	Adc
Base Current	I <sub>B</sub>	0.12	Adc
Total Power Dissipation (Note 2) @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	30 0.24	W W/°C
Total Power Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	2 0.016	W W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-65 to +150	I <sub>C</sub>

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	°C/W
Thermal Resistance, Junction-to-Case (Note 2)	R <sub>θJC</sub>	4.1	°C/W
Lead Temperature for Soldering Purpose	T <sub>L</sub>	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

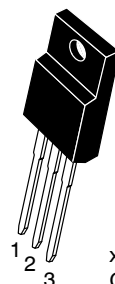
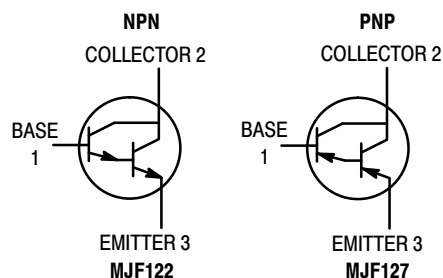
1. Proper strike and creepage distance must be provided.
2. Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.



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### COMPLEMENTARY SILICON POWER DARLINGTONS 5.0 A, 100 V, 30 W



#### MARKING DIAGRAM

TO-220  
CASE 221D-02  
STYLE 2



x = 2 or 7  
G = Pb-Free Package  
A = Assembly Location  
Y = Year  
WW = Work Week

#### ORDERING INFORMATION

Device	Package	Shipping†
MJF122	TO-220	50 Units / Rail
MJF122G	TO-220 (Pb-Free)	50 Units / Rail
MJF127	TO-220	50 Units / Rail
MJF127G	TO-220 (Pb-Free)	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MJF122, MJF127

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (Note 3) (I <sub>C</sub> = 100 mAdc, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	100	–	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 50 Vdc, I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	10	μAdc
Collector Cutoff Current (V <sub>CB</sub> = 100 Vdc, I <sub>E</sub> = 0)	I <sub>CBO</sub>	–	10	μAdc
Emitter Cutoff Current (V <sub>BE</sub> = 5 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	2	mAdc
<b>ON CHARACTERISTICS</b> (Note 3)				
DC Current Gain (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 3 Vdc) (I <sub>C</sub> = 3 Adc, V <sub>CE</sub> = 3 Vdc)	h <sub>FE</sub>	1000 2000	– –	–
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 3 Adc, I <sub>B</sub> = 12 mAdc) (I <sub>C</sub> = 5 Adc, I <sub>B</sub> = 20 mAdc)	V <sub>CE(sat)</sub>	– –	2 3.5	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 3 Adc, V <sub>CE</sub> = 3 Vdc)	V <sub>BE(on)</sub>	–	2.5	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Small–Signal Current Gain (I <sub>C</sub> = 3 Adc, V <sub>CE</sub> = 4 Vdc, f = 1 MHz)	h <sub>fe</sub>	4	–	–
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)	MJF127 MJF122 C <sub>ob</sub>	– –	300 200	pF

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

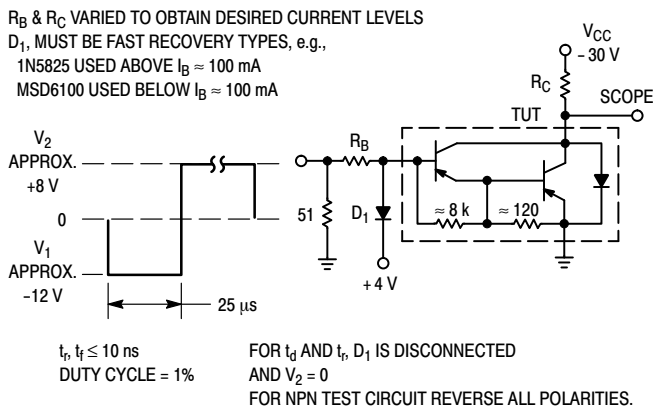


Figure 1. Switching Times Test Circuit

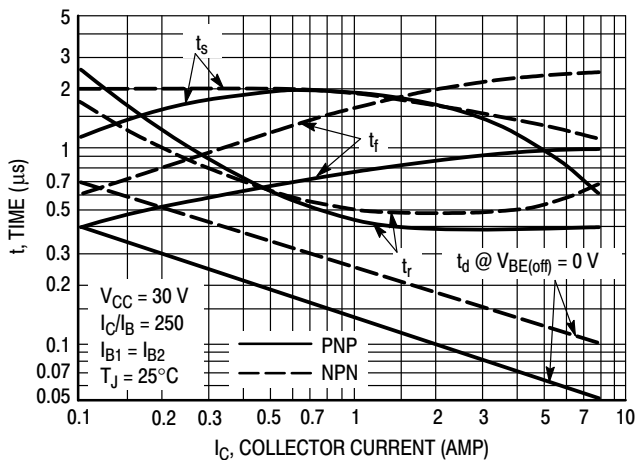


Figure 2. Typical Switching Times

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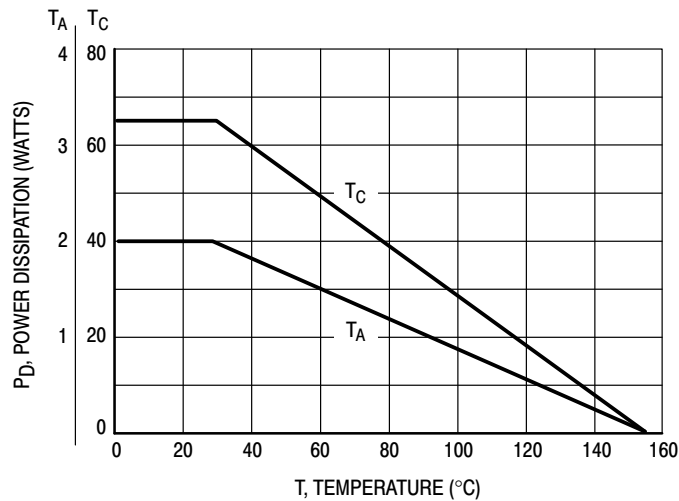


Figure 3. Maximum Power Derating

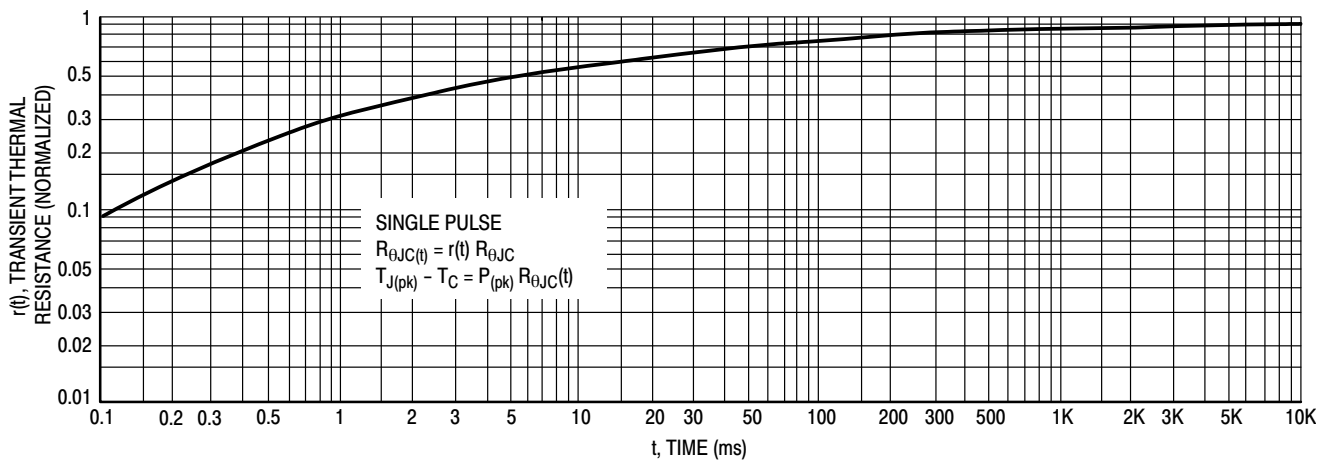


Figure 4. Thermal Response

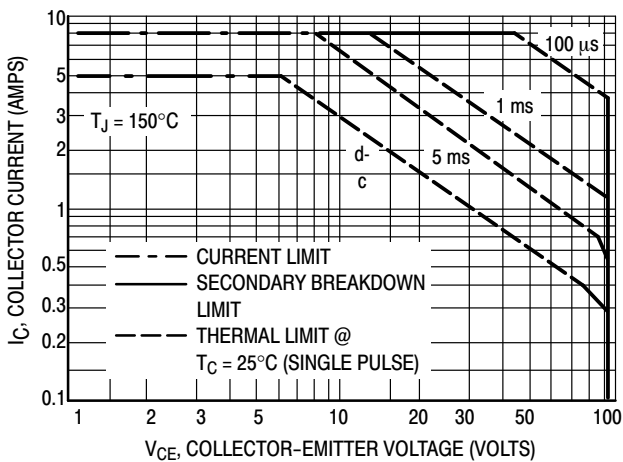


Figure 5. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

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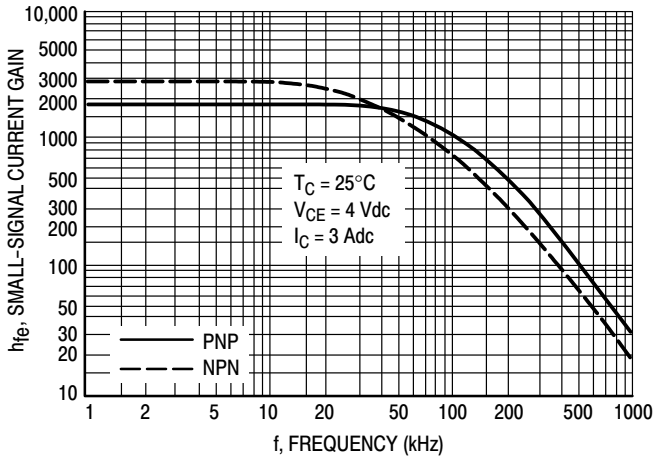


Figure 6. Typical Small-Signal Current Gain

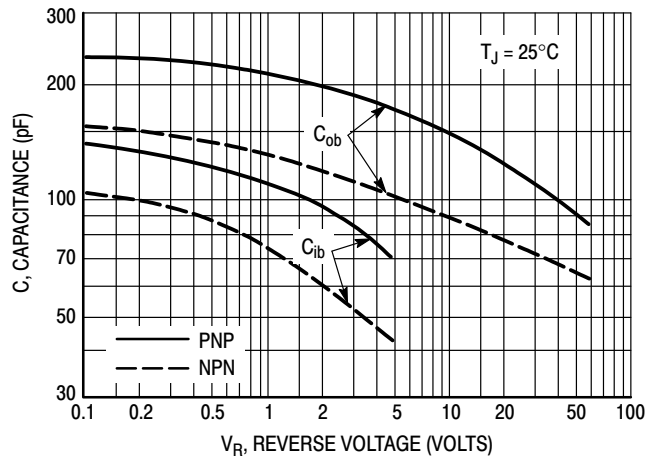


Figure 7. Typical Capacitance

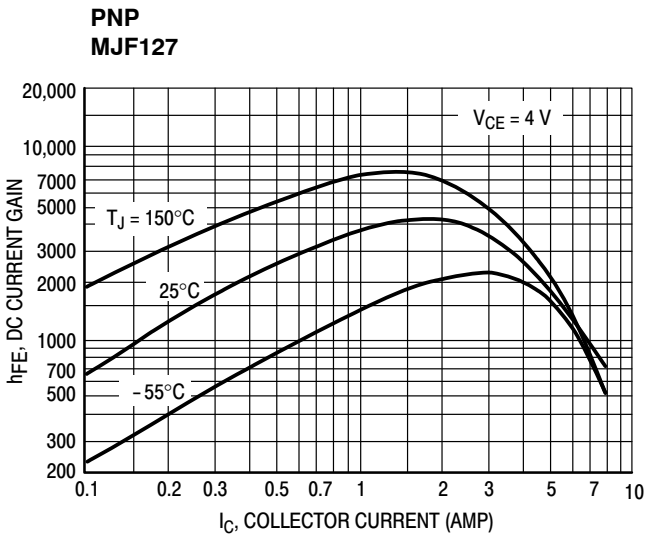
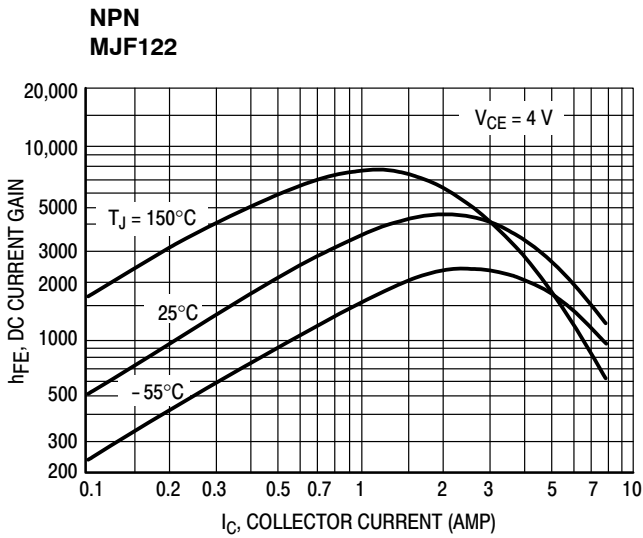


Figure 8. Typical DC Current Gain

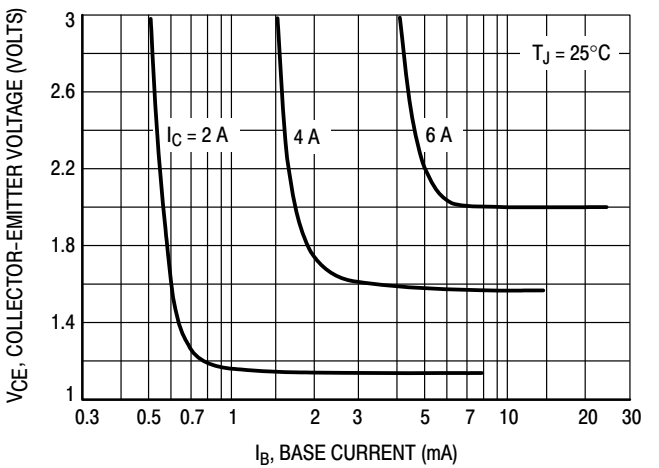
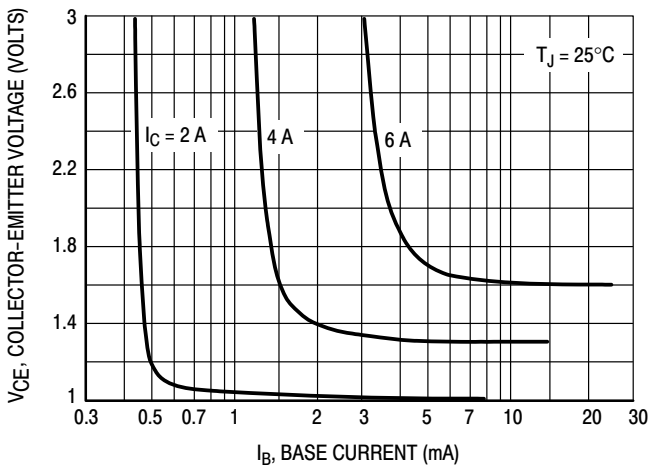
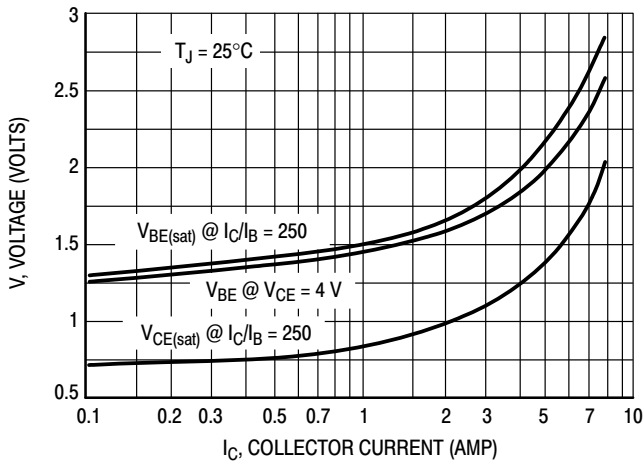


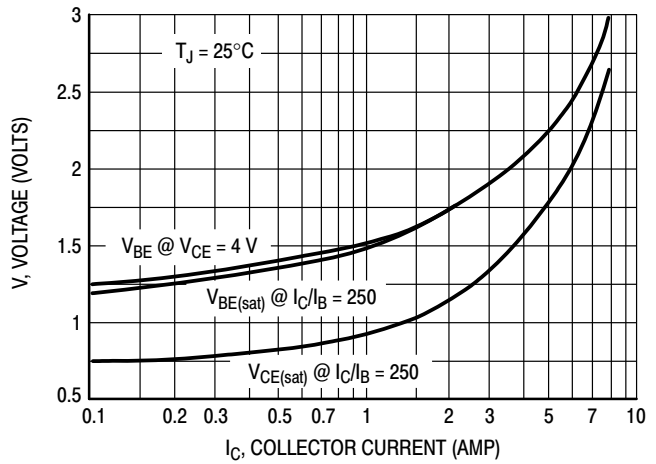
Figure 9. Typical Collector Saturation Region

# MJF122, MJF127

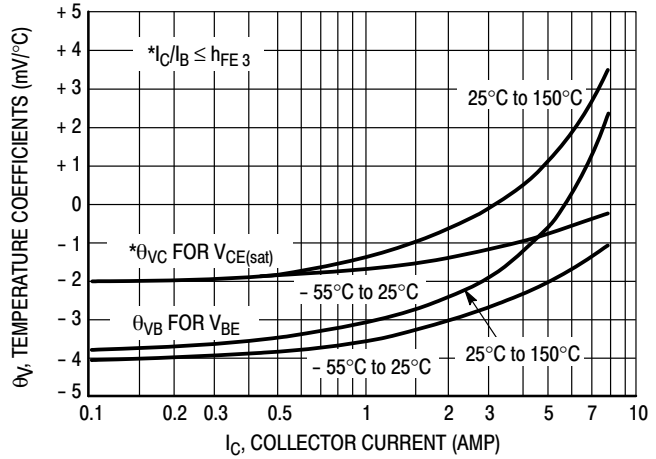
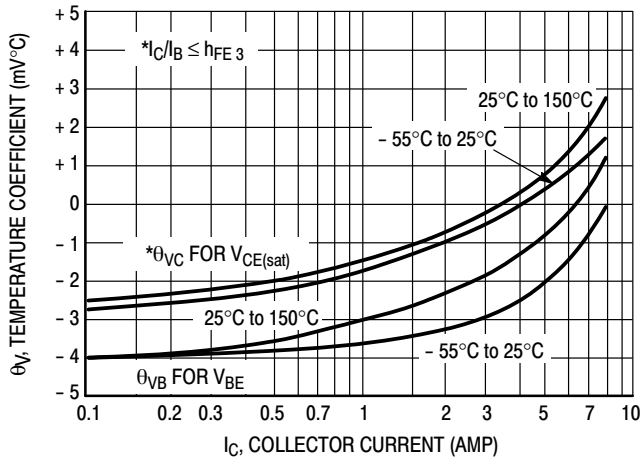
**NPN  
MJF122**



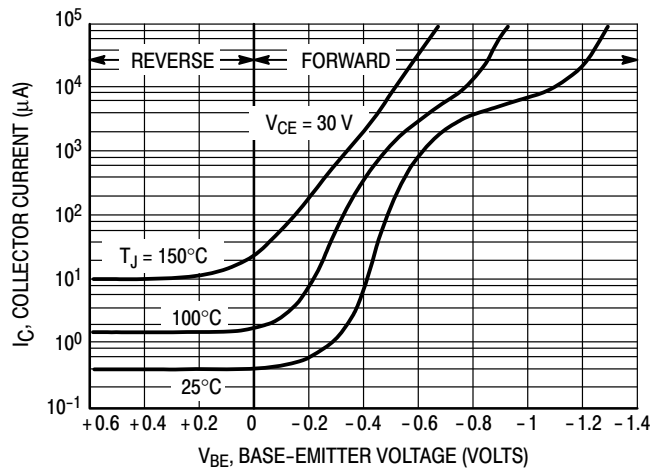
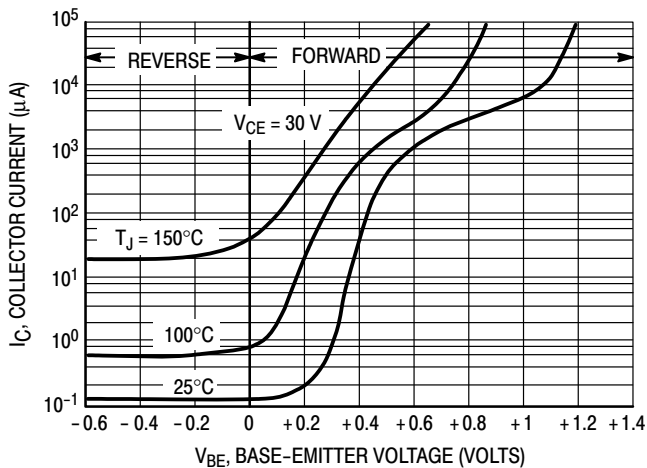
**PNP  
MJF127**



**Figure 10. Typical "On" Voltages**



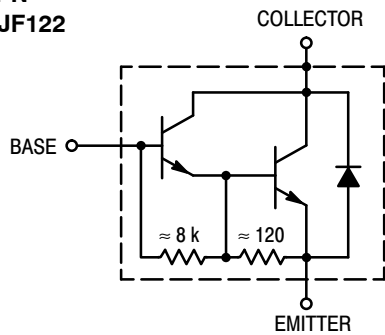
**Figure 11. Typical Temperature Coefficients**



**Figure 12. Typical Collector Cut-Off Region**

## MJF122, MJF127

NPN  
MJF122



PNP  
MJF127

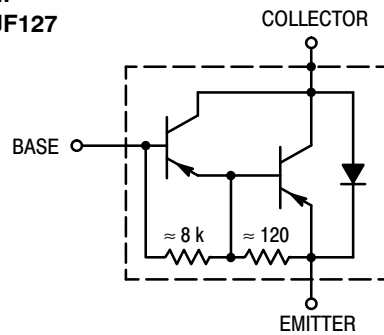


Figure 13. Darlington Schematic

### TEST CONDITIONS FOR ISOLATION TESTS\*

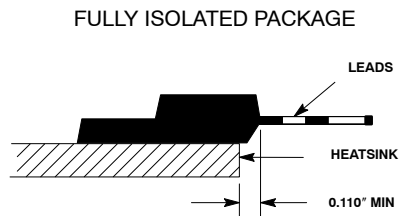


Figure 14. Mounting Position

\*Measurement made between leads and heatsink with all leads shorted together.

### MOUNTING INFORMATION

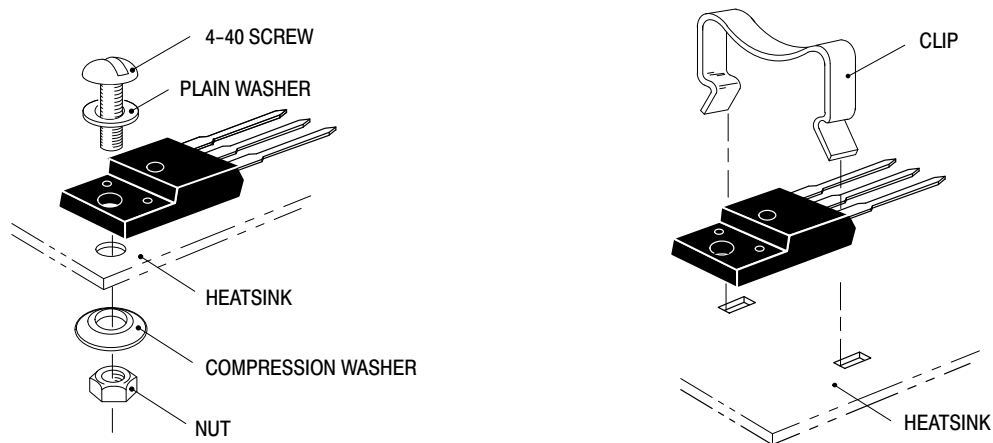


Figure 15. Typical Mounting Techniques\*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

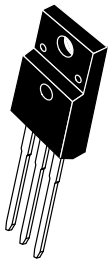
Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

\*\* For more information about mounting power semiconductors see Application Note AN1040.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

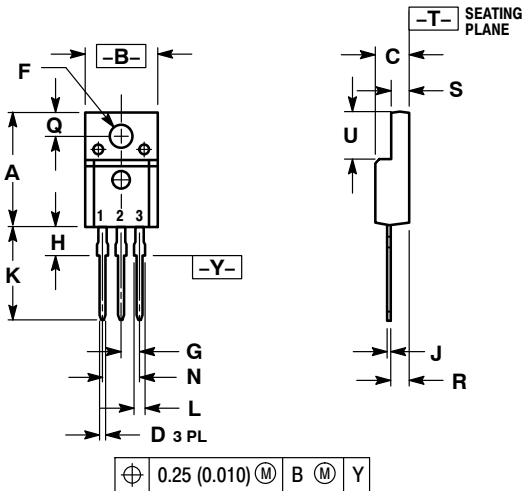
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SCALE 1:1

## TO-220 FULLPAK CASE 221D-03 ISSUE K

DATE 27 FEB 2009



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

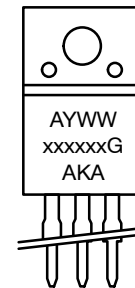
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

### MARKING DIAGRAMS

- |  |   |  |
|--|---|--|
| STYLE 1:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE     | STYLE 2:<br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER | STYLE 3:<br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE |
| STYLE 4:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE | STYLE 5:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE     | STYLE 6:<br>PIN 1. MT 1<br>2. MT 2<br>3. GATE      |



**Bipolar**



**Rectifier**

- |                               |                           |
|-------------------------------|---------------------------|
| xxxxxx = Specific Device Code | A = Assembly Location     |
| G = Pb-Free Package           | Y = Year                  |
| A = Assembly Location         | WW = Work Week            |
| Y = Year                      | xxxxxx = Device Code      |
| WW = Work Week                | G = Pb-Free Package       |
|                               | AKA = Polarity Designator |

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