FAIRCHILD SEMICONDUCTOR™

February 1984
Revised October 1999

# MM74HC4049 • MM74HC4050
# Hex Inverting Logic Level Down Converter • Hex Logic Level Down Converter

## General Description

The MM74HC4049 and the MM74HC4050 utilize advanced silicon-gate CMOS technology, and have a modified input protection structure that enables these parts to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0–15V CMOS logic can be converted to 0–5V logic when using a 5V supply. The modified input protection has no diode connected to $V_{CC}$, thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition each part can be used as a simple buffer or inverter without level translation. The MM74HC4049 is pin and functionally compatible to the CD4049BC and the MM74HC4050 is compatible to the CD4050BC

## Features

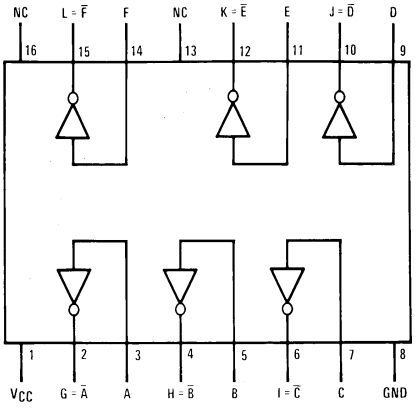
- Typical propagation delay: 8 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 20 μA maximum (74HC)
- Fanout of 10 LS-TTL loads

## Ordering Code:

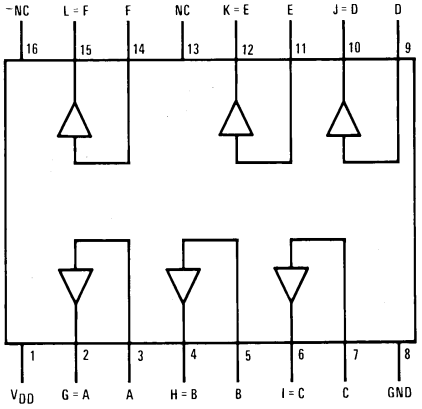
| Order Number | Package Number | Package Description |
|---|---|---|
| MM74HC4049M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow |
| MM74HC4049SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC4049MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153. 4.4mm Wide |
| MM74HC4049N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide |
| MM74HC4050M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow |
| MM74HC4050SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC4050MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153. 4.4mm Wide |
| MM74HC4050N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

## Connection Diagrams




TOP VIEW
**MM74HC4049**




TOP VIEW
**MM74HC4050**

## Absolute Maximum Ratings(Note 1)

(Note 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5 to +7.0V |
| DC Input Voltage ($V_{IN}$) | −1.5 to +18V |
| DC Output Voltage ($V_{OUT}$) | −0.5 to $V_{CC}$ +0.5V |
| Clamp Diode Current ($I_{ZK}$, $I_{OK}$) | −20 mA |
| DC Output Current, per pin ($I_{OUT}$) | ±25 mA |
| DC $V_{CC}$ or GND Current, per pin ($I_{CC}$) | ±50 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature ($T_L$) | |
| (Soldering 10 seconds) | 260°C |

## Recommended Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 2 | 6 | V |
| DC Input Voltage ($V_{IN}$) | 0 | 15 | V |
| DC Output Voltage ($V_{OUT}$) | 0 | $V_{CC}$ | V |
| Operating Temperature Range ($T_A$) | −40 | +85 | °C |
| Input Rise or Fall Times | | | |
| ($t_r$, $t_f$) $V_{CC}$ = 2.0V | | 1000 | ns |
| $V_{CC}$ = 4.5V | | 500 | ns |
| $V_{CC}$ = 6.0V | | 400 | ns |

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$ = 25°C | $T_A$ = −40°C to 85°C | $T_A$ = −55°C to 125°C | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | | 2.0V | | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5V | | 3.15 | 3.15 | 3.15 | V |
| | | | 6.0V | | 4.2 | 4.2 | 4.2 | V |
| $V_{IL}$ | Maximum LOW Level Input Voltage | | 2.0V | | 0.5 | 0.5 | 0.5 | V |
| | | | 4.5V | | 1.35 | 1.35 | 1.35 | V |
| | | | 6.0V | | 1.8 | 1.8 | 1.8 | V |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $\|I_{OUT}\| \leq 20$ µA | 2.0V | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | 4.4 | V |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | 5.9 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $\|I_{OUT}\| \leq 4.0$ mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | $\|I_{OUT}\| \leq 5.2$ mA | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | V |
| $V_{OL}$ | Maximum LOW Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $\|I_{OUT}\| \leq 20$ µA | 2.0V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $\|I_{OUT}\| \leq 4$ mA | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | $\|I_{OUT}\| \leq 5.2$ mA | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| $I_{IN}$ | Maximum Input Current | $V_{IN}$ = $V_{CC}$ or GND | 6.0V | | ±0.1 | ±1.0 | ±1.0 | µA |
| | | $V_{IN}$ = 15V | 2.0V | | ±0.5 | ±5 | ±5 | µA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND | 6.0V | | 2.0 | 20 | 40 | µA |
| | | $I_{OUT}$ = 0 µA | | | | | | |

**Note 4:** For a power supply of 5V ±10% the worst case output voltages ($V_{OH}$ and $V_{OL}$) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5V and 4.5V respectively. (The $V_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V values should be used.

## AC Electrical Characteristics

$V_{CC}$ = 5V, $T_A$ = 25°C, $C_L$ = 15 pF, $t_r$ = $t_f$ = 6 ns

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay | | 8 | 15 | ns |

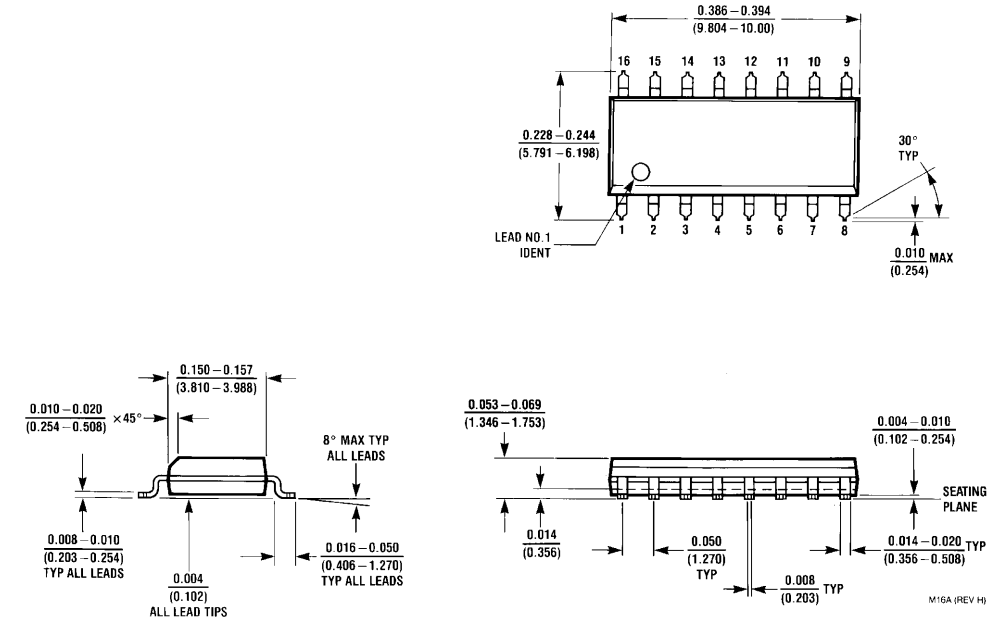
## AC Electrical Characteristics

$V_{CC}$ = 2.0V to 6.0V, $C_L$ = 50 pF, $t_r$ = $t_f$ = 6 ns (unless otherwise specified)

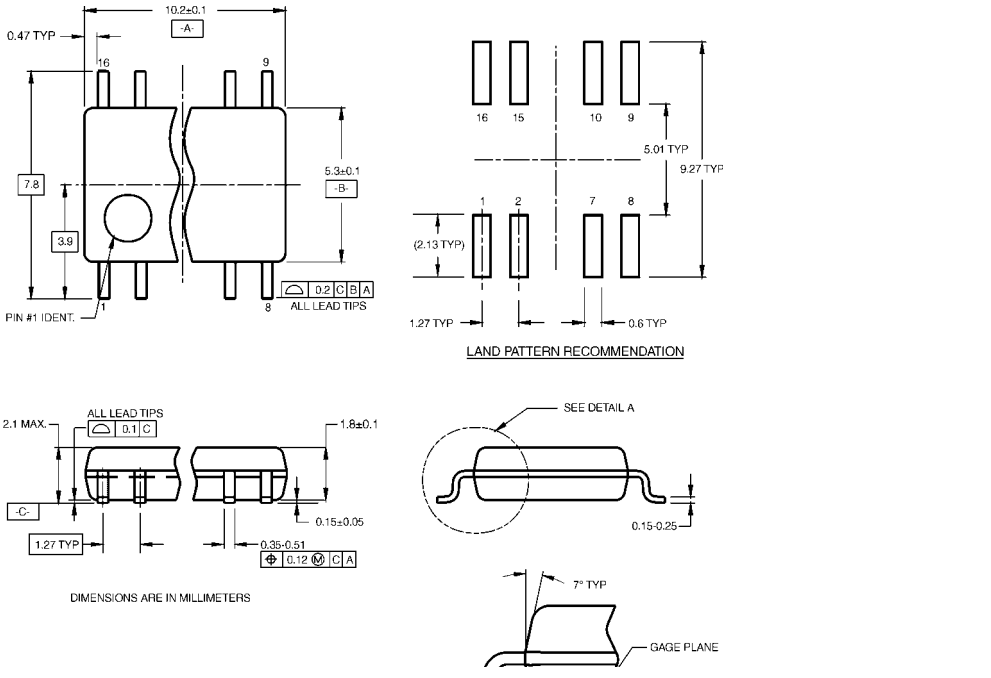
| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$ = 25°C | $T_A$ = −40° to 85°C | $T_A$ = −55° to 125°C | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | | |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay | | 2.0V | 30 | 85 | 100 | 130 | ns |
| | | | 4.5V | 10 | 17 | 20 | 26 | ns |
| | | | 6.0V | 9 | 15 | 18 | 22 | ns |
| $t_{THL}$, $t_{TLH}$ | Maximum Output Rise and Fall Time | | 2.0V | 25 | 75 | 95 | 110 | ns |
| | | | 4.5V | 7 | 15 | 19 | 22 | ns |
| | | | 6.0V | 6 | 13 | 16 | 19 | ns |
| $C_{PD}$ | Power Dissipation Capacitance (Note 5) | (per gate) | | 25 | | | | pF |
| $C_{IN}$ | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |

**Note 5:** $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

## Physical Dimensions inches (millimeters) unless otherwise noted

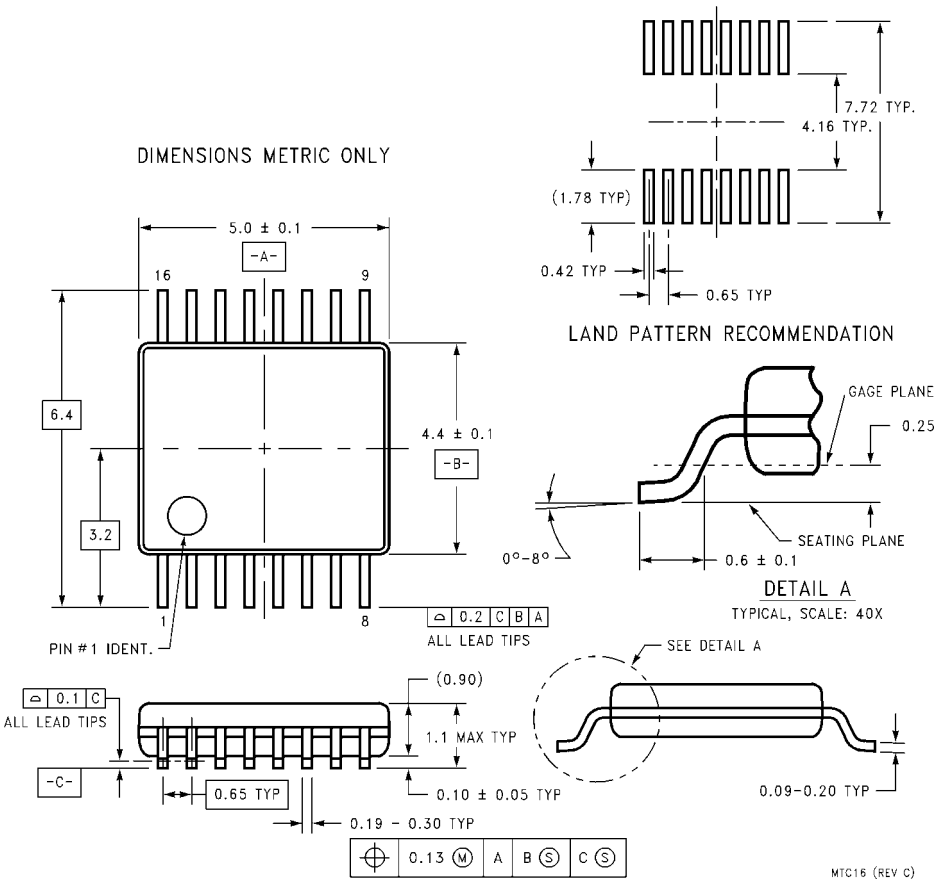



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**
**Package Number M16A**



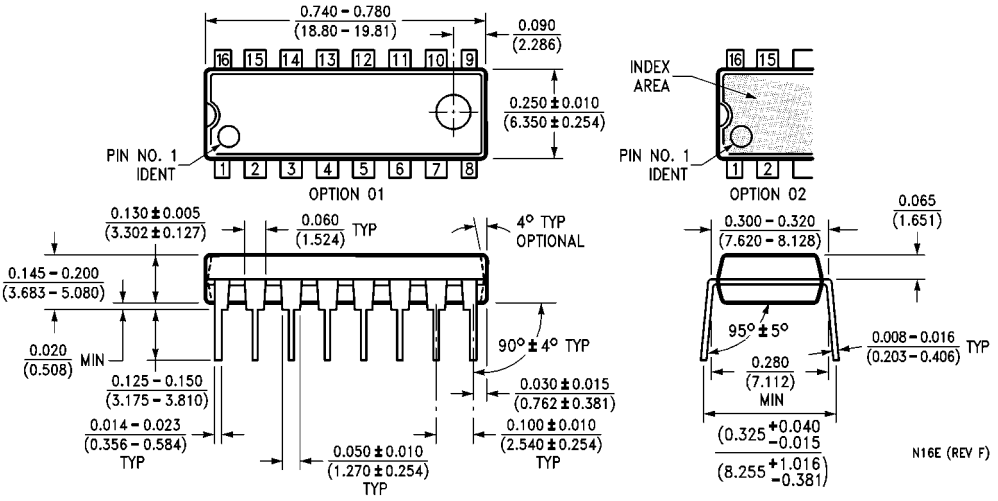

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M16D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC16**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N16E**

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