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September 1983
Revised May 2005

MM74HC540 • MM74HC541
Inverting Octal 3-STATE Buffer • Octal 3-STATE Buffer

General Description

The MM74HC540 and MM74HC541 3-STATE buffers utilize advanced silicon-gate CMOS technology. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. Both devices have a fanout of 15 LS-TTL equivalent inputs.

The MM74HC540 is an inverting buffer and the MM74HC541 is a non-inverting buffer. The 3-STATE control gate operates as a two-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are HIGH, all eight outputs are in the high-impedance state.

In order to enhance PC board layout, the MM74HC540 and MM74HC541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- 3-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Output current: 6 mA

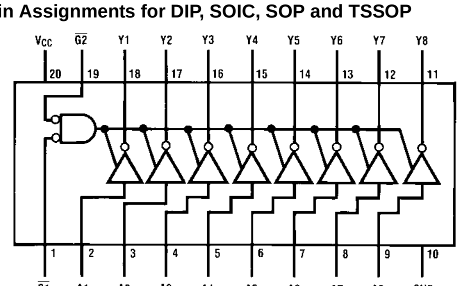
Ordering Code:

Order Number	Package Number	Package Description
MM74HC540WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC540SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC540MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC540N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HC541WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC541SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC541N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

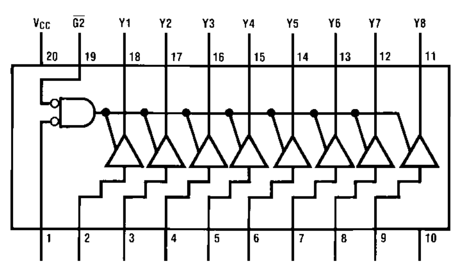
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View
MM74HC540



Top View
MM74HC541

Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C Typ	T_A = 25°C Guaranteed Limits	T_A = −40 to 85°C Guaranteed Limits	T_A = −55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3-STATE Output Leakage Current	$V_{IN} = V_{IH}$ or V_{IL}, $\overline{G} = V_{IH}$, $V_{OUT} = V_{CC}$ or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\ \mu A$	6.0V		8.0	80	160	μA

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, t_r = t_f = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay (540)	C_L = 45 pF	12	18	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay (541)	C_L = 45 pF	14	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 45 pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 5 pF	15	25	ns

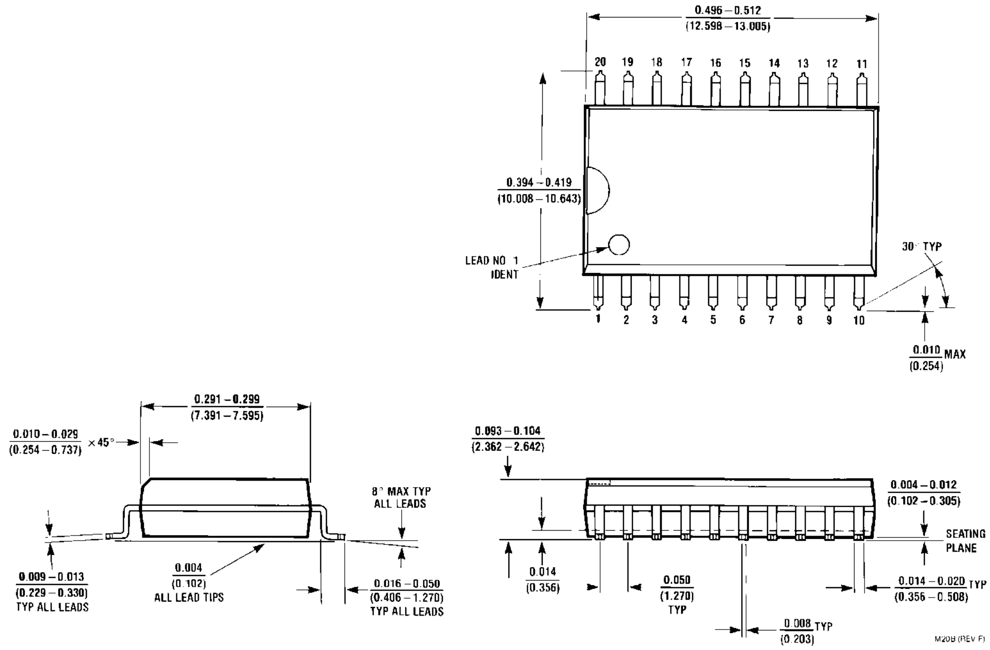
AC Electrical Characteristics

V_{CC} = 2.0V to 6.0V, C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay (540)	C_L = 50 pF	2.0V	55	100	126	149	ns
		C_L = 150 pF	2.0V	83	150	190	224	ns
		C_L = 50 pF	4.5V	12	20	25	30	ns
		C_L = 150 pF	4.5V	22	30	38	45	ns
		C_L = 50 pF	6.0V	11	17	21	25	ns
		C_L = 150 pF	6.0V	18	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay (541)	C_L = 50 pF	2.0V	58	115	145	171	ns
		C_L = 150 pF	2.0V	83	165	208	246	ns
		C_L = 50 pF	4.5V	14	23	29	34	ns
		C_L = 150 pF	4.5V	17	33	42	49	ns
		C_L = 50 pF	6.0V	11	20	25	29	ns
		C_L = 150 pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	75	150	189	224	ns
		C_L = 150 pF	2.0V	100	200	252	298	ns
		C_L = 50 pF	4.5V	15	30	38	45	ns
		C_L = 150 pF	4.5V	30	40	50	60	ns
		C_L = 50 pF	6.0V	13	26	32	38	ns
		C_L = 150 pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ	2.0V	75	150	189	224	ns
		C_L = 50 pF	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	$\overline{G}$ = V_{IH}		10				pF
		$\overline{G}$ = V_{IL}		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

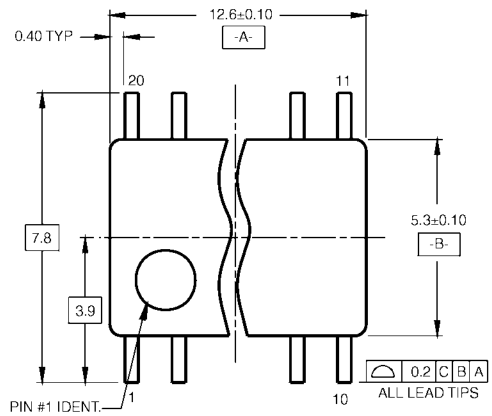
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

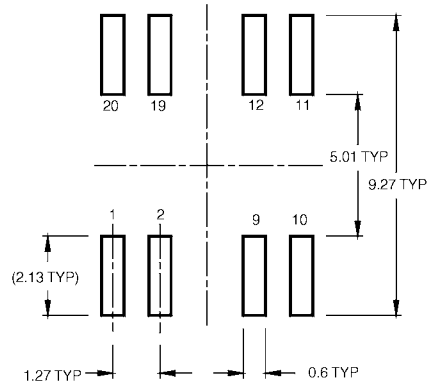
Physical Dimensions inches (millimeters) unless otherwise noted



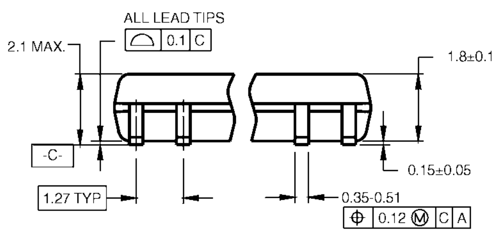
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

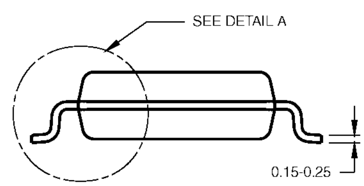




LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



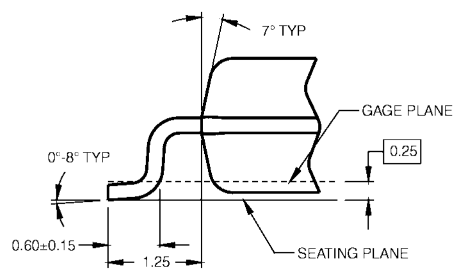
NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

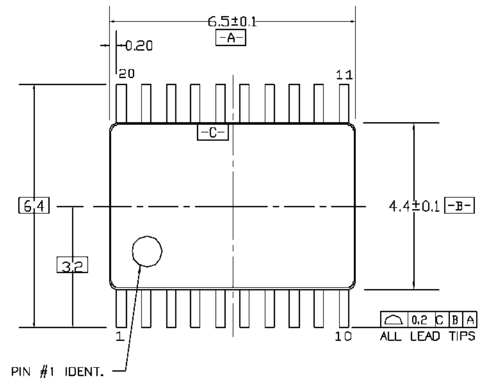
M20DRevB1

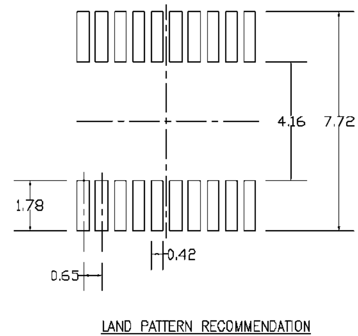


DETAIL A

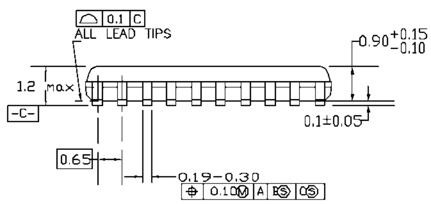
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

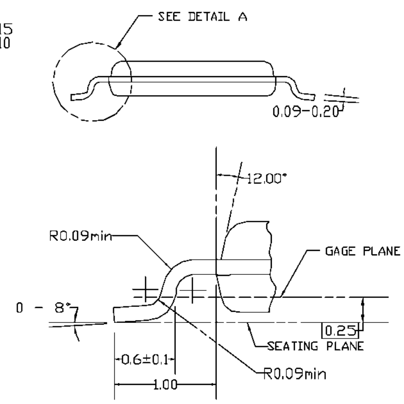




LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

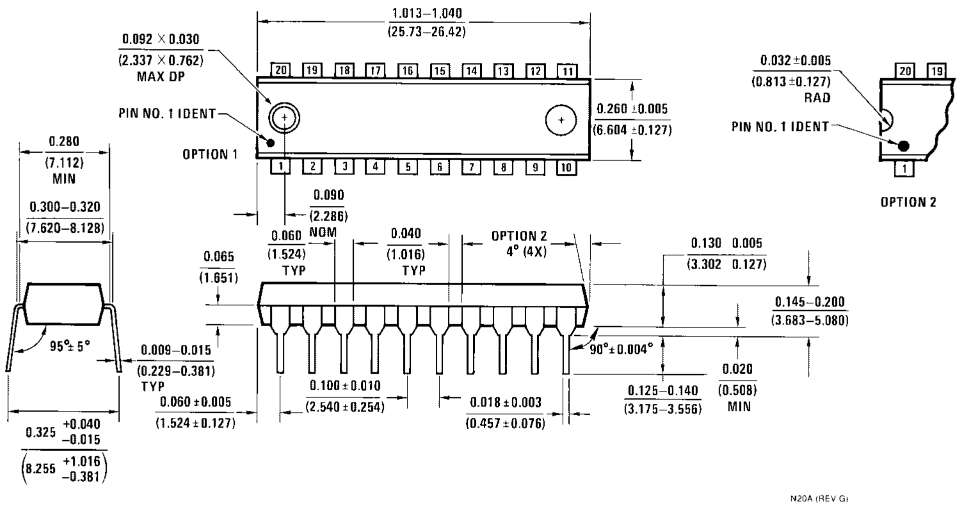
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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