September 1983 Revised May 2005

# MM74HC688 8-Bit Magnitude Comparator (Equality Detector)

#### **General Description**

FAIRCHILD

SEMICONDUCTOR

The MM74HC688 equality detector utilizes advanced silicon-gate CMOS technology to compare bit for bit two 8-bit words and indicates whether or not they are equal. The  $\overline{P=Q}$  output indicates equality when it is LOW. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information. The comparator's output can drive 10 low power Schottky equivalent loads. This comparator is functionally and pin compatible to the 74LS688. All inputs are protected from damage due to static discharge by diodes to  $\rm V_{\rm CC}$  and ground.

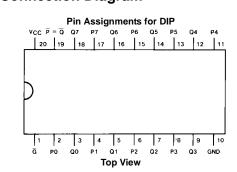
#### Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA (74 Series)
- Large output current: 4 mA (74 Series)
- Same as HC521

### **Ordering Code:**

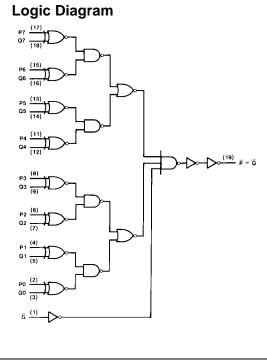
Order Number	Package Number	Package Description			
MM74HC688WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide			
MM74HC688SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide			
MM74HC688MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide			
MM74HC688N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide			
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.					

#### Connection Diagram



#### **Truth Table**

Ing	Inputs				
Data	Enable				
P,Q	G	$\overline{\mathbf{P}} = \overline{\mathbf{Q}}$			
P = Q	L	L			
P > Q	L	н			
P < Q	L	н			
Х	н	н			



**MM74HC688** 

(Note 2)

## Absolute Maximum Ratings(Note 1)

# Recommended Operating Conditions

Supply Voltage (V <sub>CC</sub> )	-0.5 to +7.0V		Min	Max	Units	
DC Input Voltage (V <sub>IN</sub> )	-1.5 to V <sub>CC</sub> +1.5V	Supply Voltage (V <sub>CC</sub> )	2	6	V	
DC Output Voltage (V <sub>OUT</sub> )	–0.5 to V <sub>CC</sub> +0.5V		0	V <sub>CC</sub>	V	
Clamp Diode Current (I <sub>IK</sub> , I <sub>OK</sub> )	±20 mA	(V <sub>IN</sub> , V <sub>OUT</sub> )				
DC Output Current, per pin (I <sub>OUT</sub> )	±25 mA	Operating Temperature Range $(T_A)$	-40	+85	°C	
DC $V_{CC}$ or GND Current, per pin (I <sub>CC</sub> )	±50 mA	Input Rise or Fall Times				
Storage Temperature Range (T <sub>STG</sub> )	-65°C to +150°C	$(t_r, t_f) V_{CC} = 2.0 V$		1000	ns	
Power Dissipation (P <sub>D</sub> )		$V_{CC} = 4.5V$		500	ns	
(Note 3)	600 mW	$V_{CC} = 6.0V$		400	ns	
S.O. Package only	500 mW	Note 1: Absolute Maximum Ratings are those	e values l	beyond whi	ch dam-	
Lead Temperature (T <sub>L</sub> )		age to the device may occur.				
(Soldering 10 seconds)	260°C	Note 2: Unless otherwise specified all voltages are referenced to ground.				
(20.20	200 0	Note 3: Power Dissipation temperature deration 12 mW/°C from 65°C to 85°C.	ng — pla	istic "N" pa	:kage: -	

## DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	Vcc	$T_A = 25^{\circ}C$		$T_A = -40$ to $85^{\circ}C$ $T_A = -55$ to $125^{\circ}C$		Units
	Faianetei		*CC	Тур		Guaranteed L	imits	Units
VIH	Minimum HIGH Level		2.0V		1.5	1.5	1.5	V
	Input Voltage		4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V <sub>IL</sub>	Maximum LOW Level		2.0V		0.5	0.5	0.5	V
	Input Voltage		4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V <sub>OH</sub>	Minimum HIGH Level	$V_{IN} = V_{IH} \text{ or } V_{IL}$						
	Output Voltage	$ I_{OUT}  \le 20 \ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$						
		$ I_{OUT}  \le 4.0 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V
		$ I_{OUT}  \le 5.2 \text{ mA}$	6.0V	5.7	5.48	5.34	5.2	V
V <sub>OL</sub>	Maximum LOW Level	$V_{IN} = V_{IH} \text{ or } V_{IL}$						
	Output Voltage	$ I_{OUT}  \le 20 \ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$						
		$ I_{OUT}  \le 4.0 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V
		$\left I_{OUT}\right  \leq 5.2 \ mA$	6.0V	0.2	0.26	0.33	0.4	V
I <sub>IN</sub>	Maximum Input	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
	Current							
I <sub>CC</sub>	Maximum Quiescent	$V_{IN} = V_{CC}$ or GND	6.0V		8.0	80	160	μΑ
	Supply Current	$I_{OUT} = 0 \ \mu A$						

Note 4: For a power supply of 5V  $\pm 10^{\circ}$  (the worst case output voltages (V<sub>OH</sub>, and V<sub>OL</sub>) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V<sub>IH</sub> and V<sub>IL</sub> occur at V<sub>CC</sub> = 5.5V and 4.5V respectively. (The V<sub>IH</sub> value at 5.5V is 3.85V.) The worst case leakage current (I<sub>IN</sub>, I<sub>CC</sub>, and I<sub>OZ</sub>) occur for CMOS at the higher voltage and so the 6.0V values should be used.

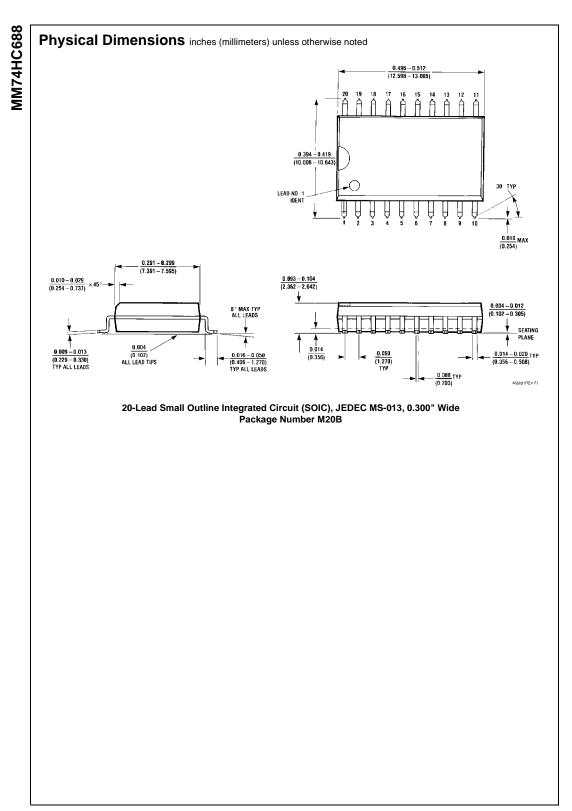
-	ectrical Characteristics $T_A = 25^{\circ}C$ , $C_L = 15 \text{ pF}$ , $t_r = t_f = 6 \text{ ns}$	i			
Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay, any P or Q to Output		21	30	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Enable to any Output		14	20	ns

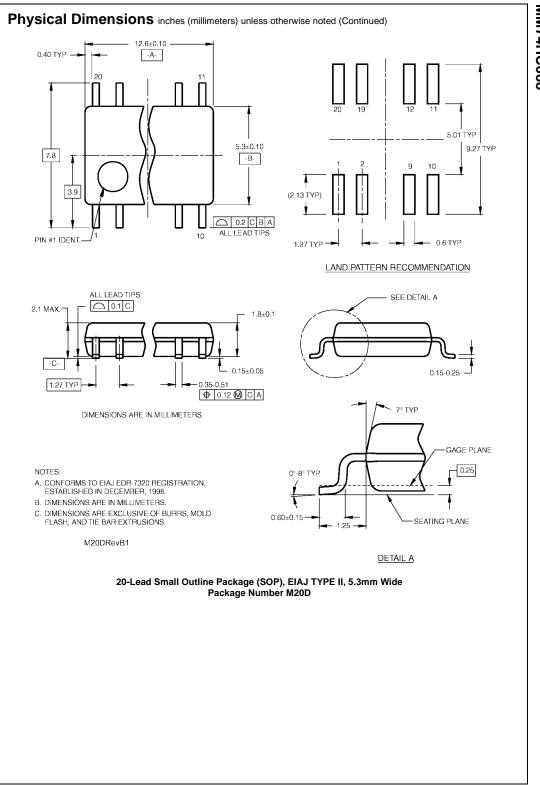
# **AC Electrical Characteristics**

 $V_{CC}$  = 2.0V to 6.0V,  $C_L$  = 50 pF,  $t_f$  =  $t_f$  = 6 ns (unless otherwise specified)

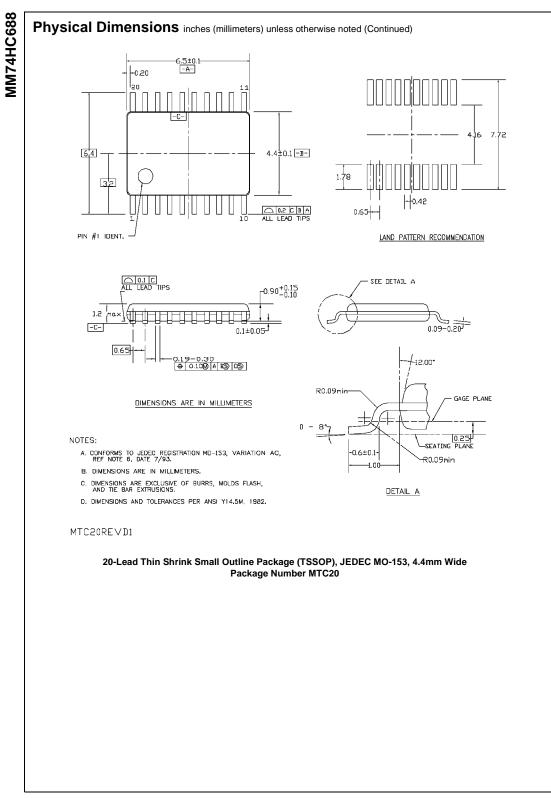
Symbol	Parameter	Conditions	v <sub>cc</sub>	T <sub>A</sub> = 25°C		$T_A = -40$ to $85^{\circ}C$	$T_A = -55$ to $125^{\circ}C$	Units
				Тур	yp Guaranteed Limits			Units
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation		2.0V	60	175	220	263	ns
	Delay, P or Q to		4.5V	22	35	44	53	ns
	Output		6.0V	19	30	38	45	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation		2.0V	45	120	150	180	ns
	Delay, Enable to		4.5V	15	24	30	36	ns
	Output		6.0V	13	20	25	30	ns
t <sub>THL</sub> , t <sub>TLH</sub>	Maximum Output Rise		2.0V	30	75	95	110	ns
	and Fall Time		4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C <sub>PD</sub>	Power Dissipation			45				pF
	Capacitance (Note 5)							
CIN	Maximum Input			5	10	10	10	pF
	Capacitance							

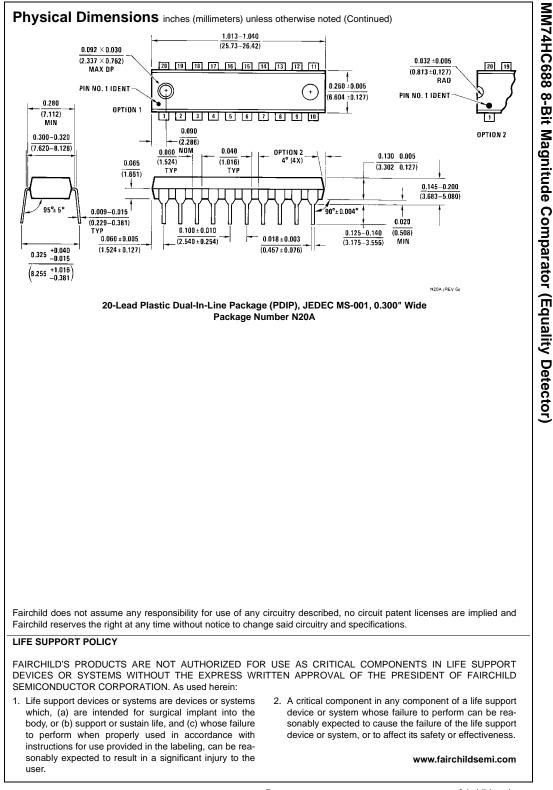
Note 5:  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .





**MM74HC688** 





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