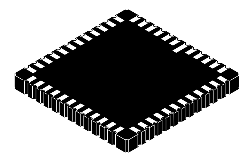
MT9M001-MONO

MT9M001C12STM (Monochrome) 1/2-inch Megapixel CMOS Digital Image Sensor

ON Semiconductor®

www.onsemi.com



CLCC48 14.22 × 14.22
CASE 848AX

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

General Description

The ON Semiconductor MT9M001 is an SXGA-format with a 1/2-inch CMOS active-pixel digital image sensor. The active imaging pixel array of 1280 (H) × 1024 (V). It incorporates sophisticated camera functions on-chip such as windowing, column and row skip mode, and snapshot mode. It is programmable through a simple two-wire serial interface.

This megapixel CMOS image sensor features ON Semiconductor's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

Table 1. KEY PERFORMANCE PARAMETERS

Parameter	Typical Value
Optical Format	1/2-inch (5:4)
Active Imager Size	6.66 mm (H) × 5.32 mm (V)
Active Pixels	1280 (H) × 1024 (V)
Pixel Size	5.2 μm × 5.2 μm
Shutter Type	Electronic Rolling Shutter (ERS)
Maximum Data Rate/Master Clock	48 MPS/48 MHz
Frame Rate − SXGA (1280 × 1024)	30 fps Progressive Scan; Programmable
ADC Resolution	10-bit, On-chip
Responsivity	2.1 V/lux-sec
Dynamic Range	68.2 dB
SNR_{MAX}	45 dB
Supply Voltage	3.0−3.6 V, 3.3 V Nominal
Power Consumption	363 mW at 3.3 V (Operating); 294 μW (Standby)
Operating Temperature	0°C to 70°C
Packaging	48-pin CLCC

The sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs an SXGA-size image at 30 frames per second (fps). An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

Features

- Array Format (5:4): 1280 (H) × 1024 (V) (1,310,720 Active Pixels). Total (Incl. Dark Pixels): 1312 (H) × 1048 (V) (1,374,976 Pixels)
- Frame Rate: 30 fps Progressive Scan; Programmable
- Shutter: Electronic Rolling Shutter (ERS)
- Window Size: SXGA; Programmable to Any Smaller Format (VGA, QVGA, CIF, QCIF, etc.)
- Programmable Controls: Gain, Frame Rate, Frame Size

Applications

- Digital Still Cameras
- Digital Video Cameras
- PC Cameras

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
MT9M001C12STM−DP	1 MP 1/2″ CIS	Dry Pack with Protective Film
MT9M001C12STM−DR	1 MP 1/2″ CIS	Dry Pack without Protective Film
MT9M001C12STM−DR1	1 MP 1/2″ CIS	Dry Pack Single Tray without Protective Film
MT9M001C12STM−TP	1 MP 1/2″ CIS	Tape & Reel with Protective Film
MT9M001C12STM−TR	1 MP 1/2″ CIS	Tape & Reel without Protective Film
MT9M001D00STMC84AC1−200	1 MP 1/2″ CIS	Die Sales, 200 μm Thickness

See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

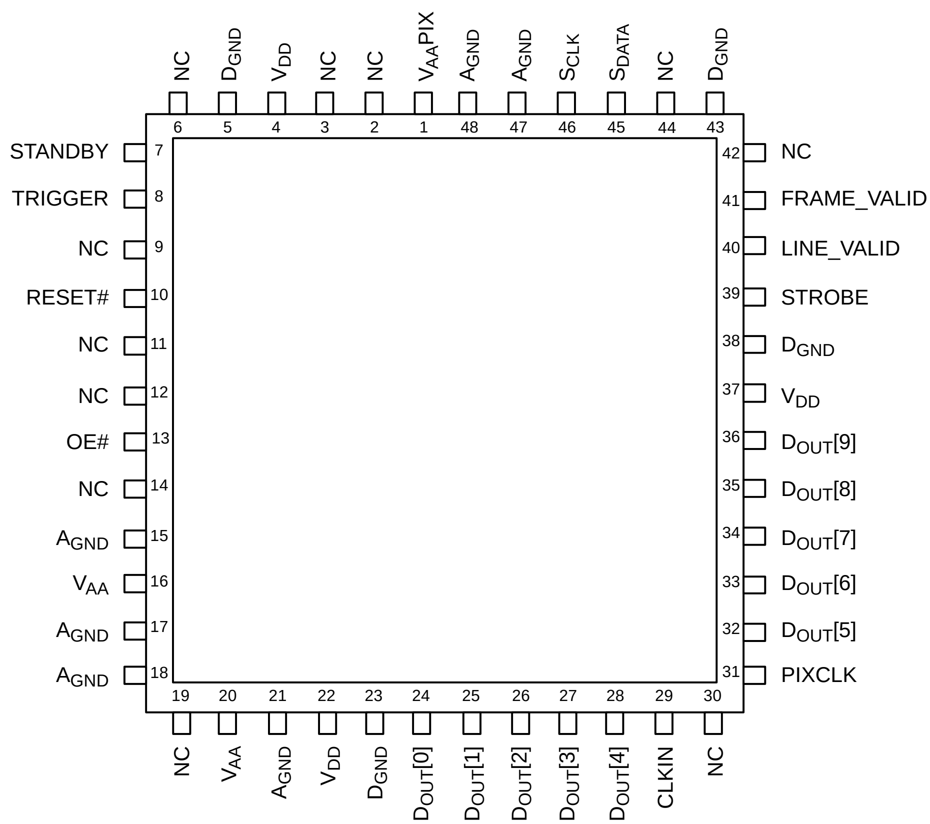


Figure 1. 48-Pin CLCC Package Pinout Diagram

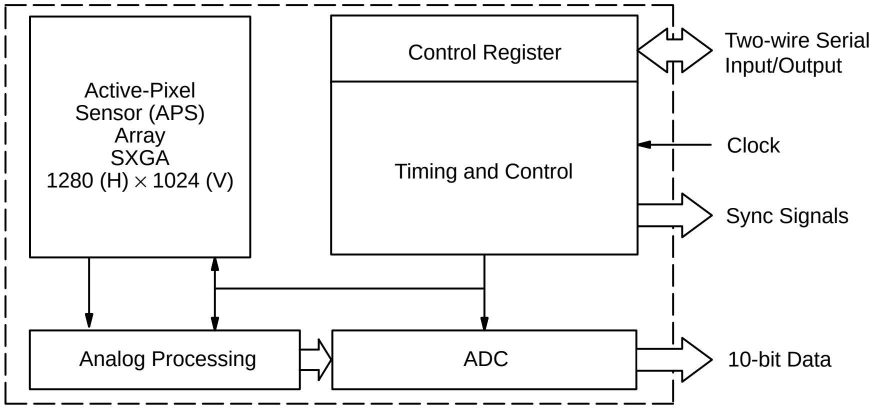


Figure 2. Block Diagram

Table 3. PIN DESCRIPTIONS

Pin Numbers	Symbol	Type	Description
29	CLKIN	Input	Clock in. Master clock into sensor (48 MHz maximum)
13	OE#	Input	Output enable. OE# when HIGH places outputs D_{OUT}[0:9], FRAME_VALID, LINE_VALID, PIXCLK, and STROBE into a tri-state configuration
10	RESET#	Input	Reset. Activates (LOW) asynchronous reset of sensor. All registers assume factory defaults
46	SCLK	Input	Serial clock. Clock for serial interface
7	STANDBY	Input	Standby. Activates (HIGH) standby mode, disables analog bias circuitry for power saving mode
8	TRIGGER	Input	Trigger. Activates (HIGH) snapshot sequence
45	S_{DATA}	Input/Output	Serial data. Serial data bus, requires 1.5 kΩ resistor to 3.3 V for pull-up
24–28, 32–36	D_{OUT}[0:9]	Output	Data out. Pixel data output bits 0:9, D_{OUT}[9] (MSB), D_{OUT}[0] (LSB)
41	FRAME_VALID	Output	Frame valid. Output is pulsed HIGH during frame of valid pixel data
40	LINE_VALID	Output	Line valid. Output is pulsed HIGH during line of selectable valid pixel data (see Reg0x20 for options)
31	PIXCLK	Output	Pixel clock. Pixel data outputs are valid during falling edge of this clock. Frequency = (master clock)
39	STROBE	Output	Strobe. Output is pulsed HIGH to indicate sensor reset operation of pixel array has completed
15, 17, 18, 21, 47, 48	A_{GND}	Supply	Analog ground. Provide isolated ground for analog block and pixel array
5, 23, 38, 43	D_{GND}	Supply	Digital ground. Provide isolated ground for digital block
16, 20	V_{AA}	Supply	Analog power. Provide power supply for analog block, 3.3 V ±0.3 V
1	VAAPIX	Supply	Analog pixel power. Provide power supply for pixel array, 3.3 V ±0.3 V (3.3 V)
4, 22, 37	V_{DD}	Supply	Digital power. Provide power supply for digital block, 3.3 V ±0.3 V
2, 3 ,6, 9, 11, 12, 14, 19, 30, 42, 44	NC	−	No connect. These pins must be left unconnected

PIXEL DATA FORMAT

Pixel Array Structure

The MT9M001 pixel array is configured as 1,312 columns by 1,048 rows (shown in Figure 3). The first 16 columns and the first eight rows of pixels are optically black, and can be used to monitor the black level. The last seven columns and the last seven rows of pixels are also optically black. The black row data is used internally for the automatic black level adjustment. However, the black rows can also be read out by setting the sensor to raw data output mode (Reg0x20, bit 11 = 1). There are 1,289 columns by 1,033 rows of optically active pixels, which provides a four-pixel boundary around the SXGA (1280 × 1024) image.

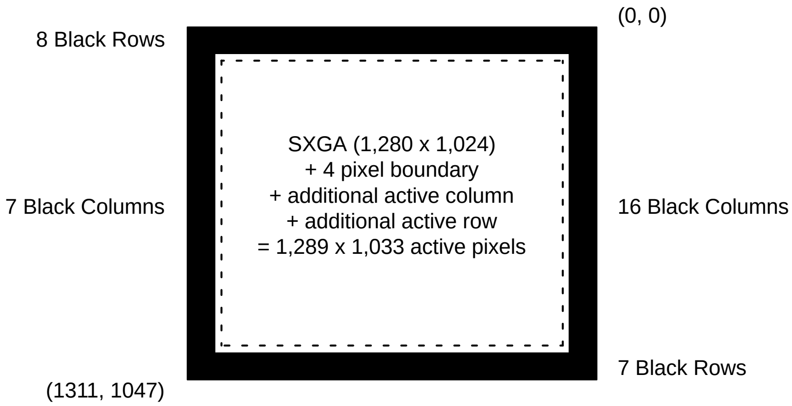


Figure 3. Pixel Array Description

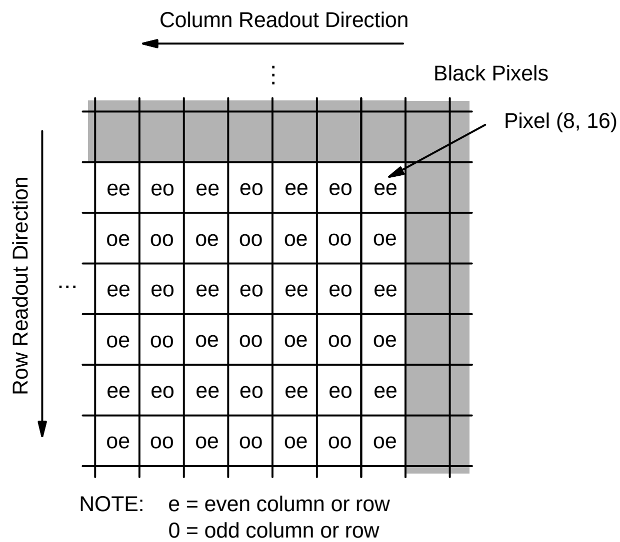


Figure 4. Pixel Pattern Detail (Top Right Corner)

Output Data Format

The MT9M001 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 5. The amount of horizontal blanking and vertical blanking is programmable through Reg0x05 and Reg0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. FRAME_VALID timing is described in "Output Data Timing".

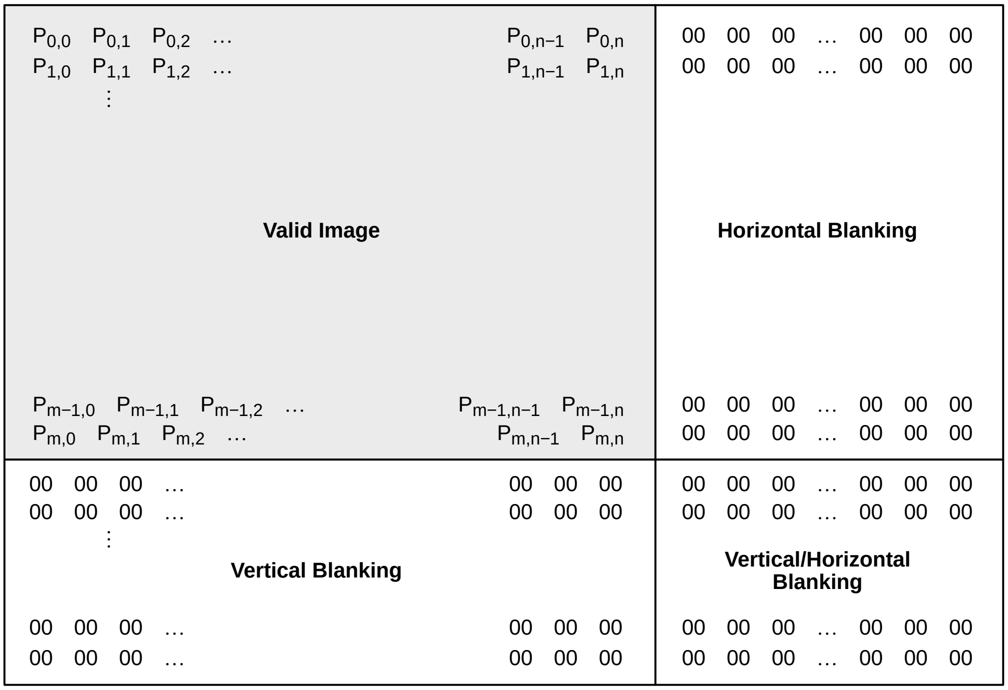


Figure 5. Spatial Illustration of Image Readout

Output Data Timing

The data output of the MT9M001 is synchronized with the PIXCLK output. When LINE_VALID is HIGH, one 10-bit pixel datum is output every PIXCLK period.

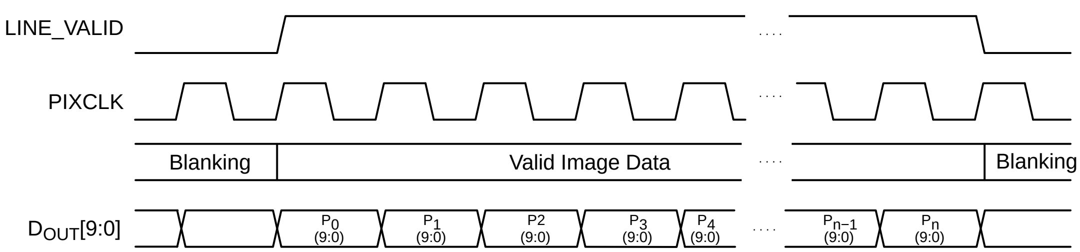


Figure 6. Timing Example of Pixel Data

The rising edges of the PIXCLK signal are nominally timed to occur on the rising D_{OUT} edges. This allows PIXCLK to be used as a clock to latch the data. D_{OUT} data is valid on the falling edge of PIXCLK. The PIXCLK is HIGH while master clock is HIGH and then LOW while master clock is LOW. It is continuously enabled, even during the blanking period. The parameters P1, A, P2, and Q in Figure 7 are defined in Table 4.

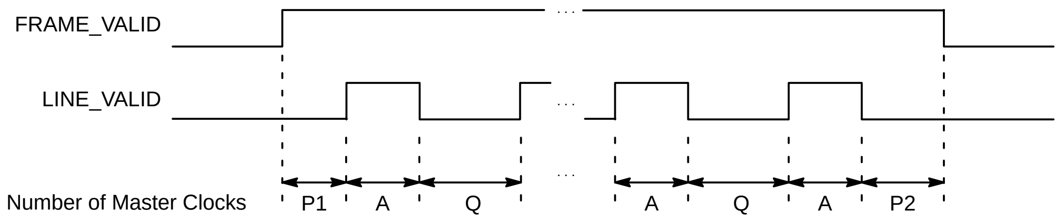


Figure 7. Row Timing and FRAME_VALID/LINE_VALID Signals

Frame Timing Formulas

Table 4. FRAME TIMING

Parameter	Name	Equation (MASTER CLOCK)	Default Timing
A	Active Data Time (Note 1)	(Reg0x04 + 1)	1,280 Pixel Clocks = 26.7 μs
P_1	Frame Start Blanking	(242)	242 Pixel Clocks = 5.04 μs
P_2	Frame End Blanking (Note 2)	(2 + Reg0x05 − 19) (MIN Reg0x05 value = 19)	2 Pixel Clocks = 0.042 μs
$Q = P_1 + P_2$	Horizontal Blanking (Note 2)	(244 + Reg0x05 − 19) (MIN Reg0x05 value = 19)	244 Pixel Clocks = 5.08 μs
A + Q	Row Time	((Reg0x04 + 1) + (244 + Reg0x05 − 19))	1,524 Pixel Clocks = 31.75 μs
V	Vertical Blanking	(Reg0x06 + 1) × (A + Q) (MIN Reg0x06 value = 15)	39,624 Pixel Clocks = 825.5 μs
$N_{ROWS} \times (A + Q)$	Frame Valid Time	(Reg0x03 + 1) × (A + Q)	1,560,576 Pixel Clocks = 32.51 ms
F	Total Frame Time	(Reg0x03 + 1 + Reg0x06 + 1) × (A + Q)	1,600,200 Pixel Clocks = 33.34 ms

1. Row skip mode should have no effect on the integration time. Column skip mode changes the effective value of Column Size (Reg0x04) as follows:
   Column Skip 2 => R4eff = (int(R4 / 4) × 2) + 1
   Column Skip 4 => R4eff = (int(R4 / 8) × 2) + 1
   Column Skip 8 => R4eff = (int(R4 / 16) × 2) + 1
   where the int() function truncates to the next lowest integer. Now use R4eff in the equation for row time instead of R4.
2. Default for Reg0x05 = 9. However, sensor ignores any value for Reg0x05 less than 19.

Sensor timing is shown above in terms of pixel clock and master clock cycles (please refer to Figure 6). The recommended master clock frequency is 48 MHz. The vertical blank and total frame time equations assume that the number of integration rows (bits 13 through 0 of Reg0x09) is less than the number of active plus blanking rows (Reg0x03 + 1 + Reg0x06 + 1). If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 5.

Table 5. FRAME TIME − LONG INTEGRATION TIME

Parameter	Name	Equation (MASTER CLOCK)	Default Timing
V’	Vertical Blanking (Long Integration Time)	(Reg0x09 – Reg0x03) × (A + Q)	39,624 Pixel Clocks = 82.5 μs
F’	Total Frame Time (Long Integration Time)	(Reg0x09 + 1) × (A + Q)	1,600,200 Pixel Clocks = 33.34 ms

SERIAL BUS DESCRIPTION

Registers are written to and read from the MT9M001 through the two-wire serial interface bus. The sensor is a two-wire serial interface slave and is controlled by the serial clock (S_{CLK}), which is driven by the serial interface master. Data is transferred into and out of the MT9M001 through the serial data (S_{DATA}) line. The S_{DATA} line is pulled up to 3.3 V off-chip by a 1.5 kΩ resistor. Either the slave or master device can pull the S_{DATA} line down − the serial interface protocol determines which device is allowed to pull the S_{DATA} line down at any given time.

Protocol

The two-wire serial interface defines several different transmission codes, as follows:

- a start bit
- the slave device 8-bit address
- a(an) (no) acknowledge bit
- an 8-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's eight-bit address. The last bit of the address determines if the request will be a read or a write, where a "0" indicates a write and a "1" indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data eight bits at a time, with the slave sending an acknowledge bit after each eight bits. The MT9M001 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of seven bits of address and 1 bit of direction. A "0" (0xBA) in the LSB (least significant bit) of the address indicates the write mode, and a "1" (0xBB) indicates read mode.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock − it can only change when the serial clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

TWO-WIRE SERIAL INTERFACE SAMPLE WRITE AND READ SEQUENCES

16-Bit WRITE Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 8. A start bit given by the master, followed by the write address, starts the sequence. The image sensor will then give an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each eight-bit transfer, the image sensor will give an acknowledge bit. All 16 bits must be written before the register will be updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

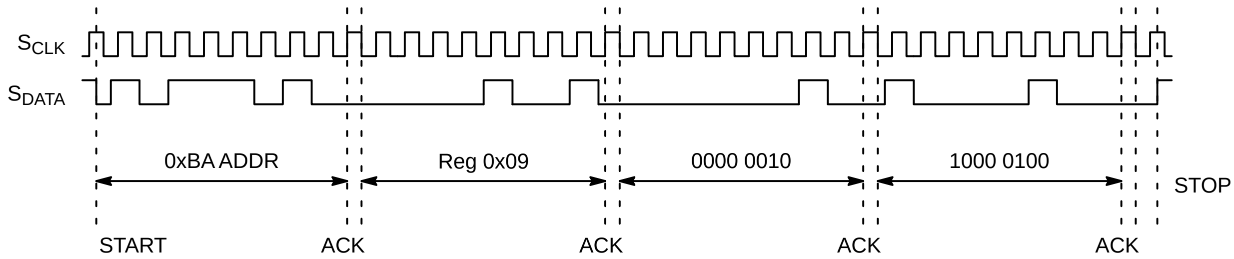


Figure 8. Timing Diagram Showing a WRITE to Reg0x09 with the Value 0x0284

16-Bit READ Sequence

A typical read sequence is shown in Figure 9. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

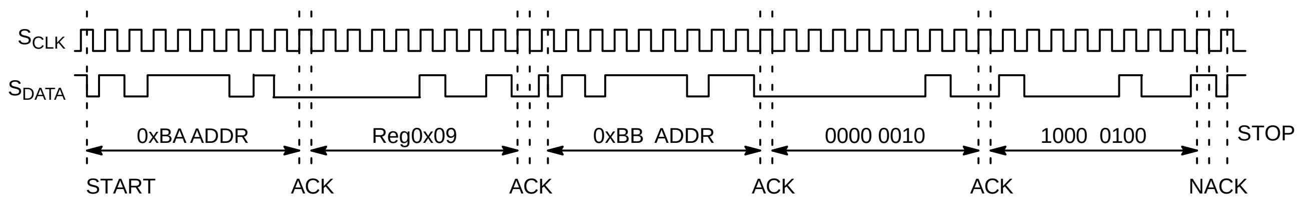


Figure 9. Timing Diagram Showing a READ from Reg0x09, Returned Value 0x0284

FEATURE DESCRIPTION

Signal Path

The MT9M001 signal path consists of two stages, a programmable gain stage and a programmable analog offset stage.

Programmable Gain Stage

A total programmable gain of 15 is available and can be calculated using the following formula:

Gain 1 to 8: Gain = (bit[6] + 1) × (bit[5:0] × 0.125)

For gain higher than eight, the user would need to set bit[6:5] = 11 and use the lower 3 LSB's bit[2:0] to set the higher gain values. The formula for obtaining gain greater than eight is as follows:

Total gain = 8 + bit[2:0]

For example, for total gain = 12, the value to program is bit[6–0] = 1100100.

The maximum total gain = 15, i.e. bit[6:0] = 1100111.

The gain circuitry in the MT9M001 is designed to offer signal gains from one to 15. The minimum gain of one corresponds to the lowest setting where the pixel signal is guaranteed to saturate the ADC under all specified operating conditions. Any reduction of the gain below this value may cause the sensor to saturate at ADC output values less than the maximum, under certain conditions. It is recommended that this guideline be followed at all times.

Since bit[6] of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, despite the same overall gain. Recommended gain settings are listed in Table 6.

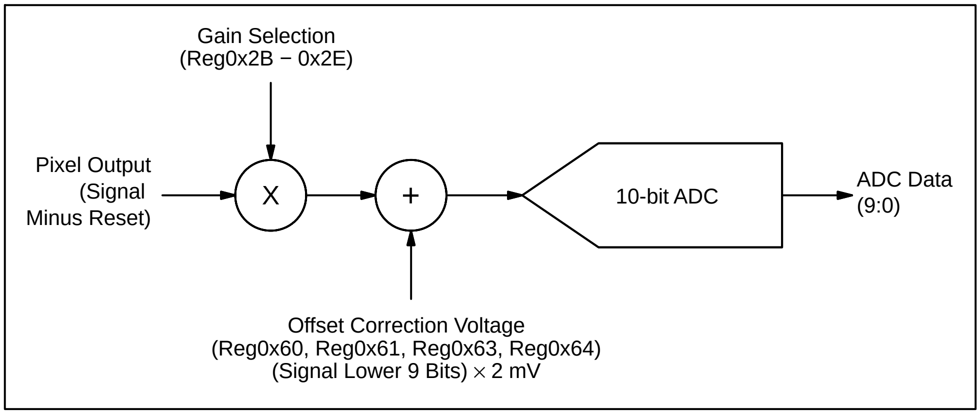


Figure 10. Signal Path

Table 6. RECOMMENDED GAIN SETTINGS AT 48 MHZ

Nominal Gain	Increments	Recommended Settings
1 to 4.000	0.125	0x08 to 0x20
4.25 to 8.00	0.25	0x51 to 0x60
9 to 15	1.0	0x61 to 0x67

Programmable Analog Offset Stage

The programmable analog offset stage corrects for analog offset that might be present in the analog signal. The user would need to program register 0x62 appropriately to enable the analog offset correction.

The lower eight bits (bit[7:0]) determines the absolute value of the analog offset to be corrected and bit[8] determines the sign of the correction. When bit[8] is "1", the sign of the correction is negative and vice versa. The analog value of the correction relative to the analog gain stage can be determined from the following formula:

Analog offset (bit[8] = 0) = bit[7:0] × 2 mV

Analog offset (bit[8] = 1) = − (bit[7:0] × 2 mV)

Column and Row Mirror Image

By setting bit 14 of Reg0x20, the readout order of the columns will be reversed, as shown in Figure 11.

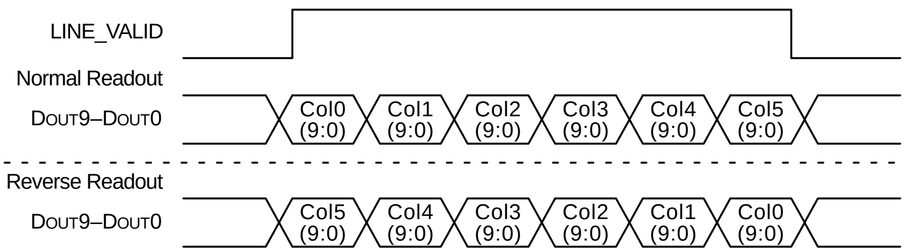


Figure 11. Readout of Six Columns in Normal and Column Mirror Output Mode

By setting bits 15 of Reg0x20 the readout order of the rows will be reversed, as shown in Figure 12.

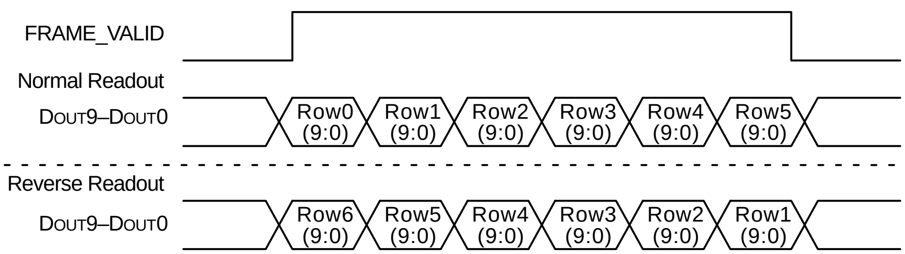


Figure 12. Readout of Six Rows in Normal and Row Mirror Output Mode

Column and Row Skip

By setting bit 3 of Reg0x20, only half of the columns set will be read out. An example is shown in Figure 13. Only columns with bit 1 equal to “0” will be read out (xxxxxxx0x). The row skip works in the same way and will only read out rows with bit 1 equal to “0”. Row skip mode is enabled by setting bit 4 of Reg0x20. For both row and column skips, the number of rows or columns read out will be half of what is set in Reg0x03 or Reg0x04, respectively.

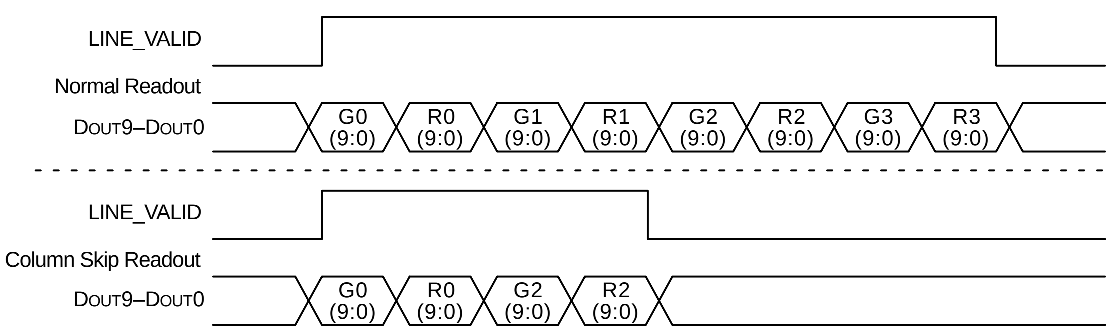


Figure 13. Readout of Eight Pixels in Normal and Column Skip Output Mode

Black Level Calibration

The MT9M001 has automatic black level calibration on-chip which can be overridden by the user, as described below and shown in Figure 14.

The automatic black level calibration measures the average value of 256 pixels from two dark rows of the chip for each of the four colors. The pixels are averaged as if they were light-sensitive and passed through the appropriate color gain. This average is then digitally filtered over many frames.

For each color, the new filtered average is compared to a minimum acceptable level (to screen for too low a black level) and a maximum acceptable level. If the average is lower than the minimum acceptable level, the offset correction voltage for that color is increased by one offset LSB (offset LSBs do not match ADC LSBs; typically, one offset LSB is approximately 2 mV). If it is above the maximum level, the level is decreased by 1 LSB (2 mV). The upper threshold is automatically adjusted upwards whenever an upward shift in the black level from below the minimum results in a new black level above the maximum. This prevents black level oscillation from below the minimum to above the maximum. The lower threshold is increased with the maximum gain setting according to the formula described under Reg0x5F. This prevents clipping of the black level.

Whenever the gain or any of the readout timing registers is changed (shutter width, vertical blanking, number of rows or columns, or the shutter delay) or if the black level recalculation bit, reset bit or restart bit is set, the running digitally filtered average is reset to the first average of the dark pixels. The digital filtering over many frames is then restarted. Whenever the gain or the readout timing registers are changed, the upper threshold is restored to its default value.

After changes to the sensor configuration, large shifts in the black level calibration can result. To quickly adapt to this shift, a rapid sweep of the black level during the dark-row readout is performed on the first frame after certain changes to the sensor registers. Any changes to the registers listed above will cause this recalculation. The data from this sweep allows the sensor to choose an accurate new starting point for the running average. This procedure can be disabled as described under Reg0x5F.

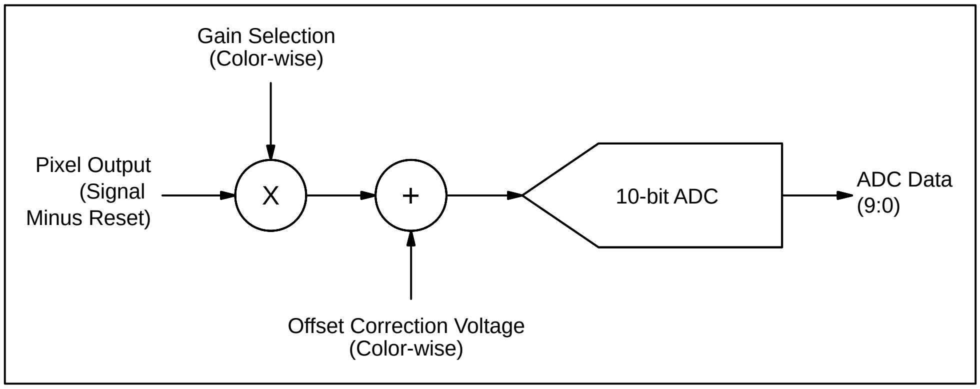


Figure 14. Black Level Calibration Flow Chart

Still Image Capture with External Synchronization

In continuous mode video image capture, the TRIGGER signal should be held LOW or “0”. To capture a still image, the sensor must first be put into snapshot mode by programming a “1” in register 0x1E, bit 8. In snapshot mode, the sensor waits for a TRIGGER signal (FRAME_VALID, LINE_VALID signals are LOW, pixel clock signal continues). When the TRIGGER signal is received (active HIGH), one frame is read out (a TRIGGER signal can also be achieved by programming a restart − for example, program a “1” to bit 0 of Reg0x0B). The reset, readout timing for that frame will be the same as for a continuous frame with similar register settings; the only difference is that only one frame is read out. General timing for the snapshot mode is shown in Figure 15.

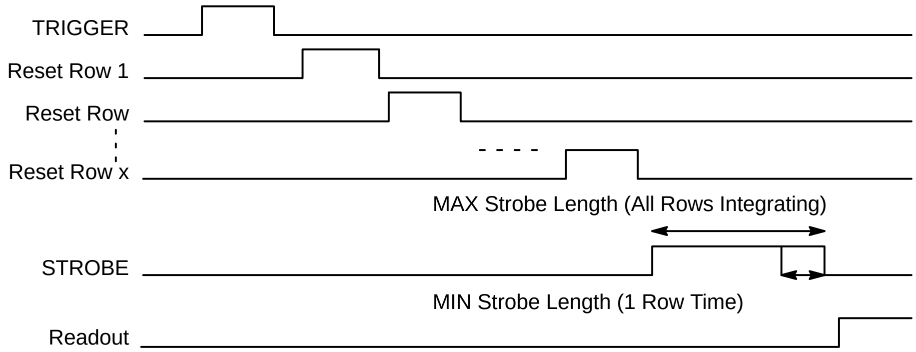


Figure 15. General Timing for Snapshot Mode

LINE_VALID Signal

By setting bit 9 and 10 of Reg0x20 the line valid signal can get three different output formats. The formats are shown when reading out four rows and two vertical blanking rows (Figure 16). In the last format, the LINE_VALID signal is the XOR between the continuously LINE_VALID signal and the FRAME_VALID signal.

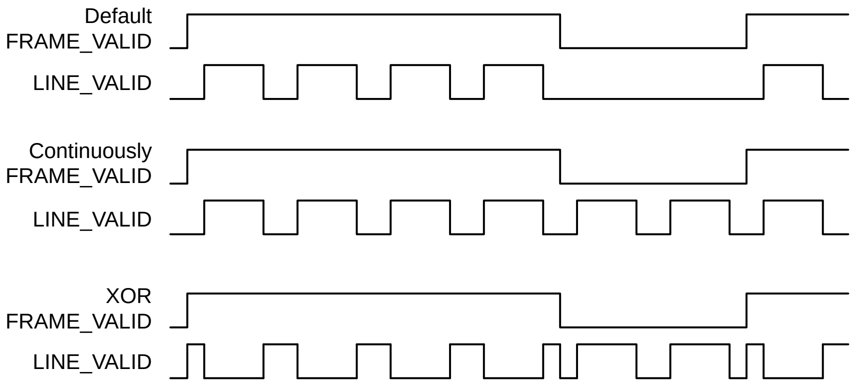


Figure 16. Different LINE_VALID Formats

ELECTRICAL SPECIFICATIONS

Data Output and Propagation Delays

By default, the MT9M001 launches pixel data, FRAME_VALID and LINE_VALID with the rising edge of PIXCLK. The expectation is that the user captures D_{OUT}[7:0], FRAME_VALID and LINE_VALID using the falling edge of PIXCLK.

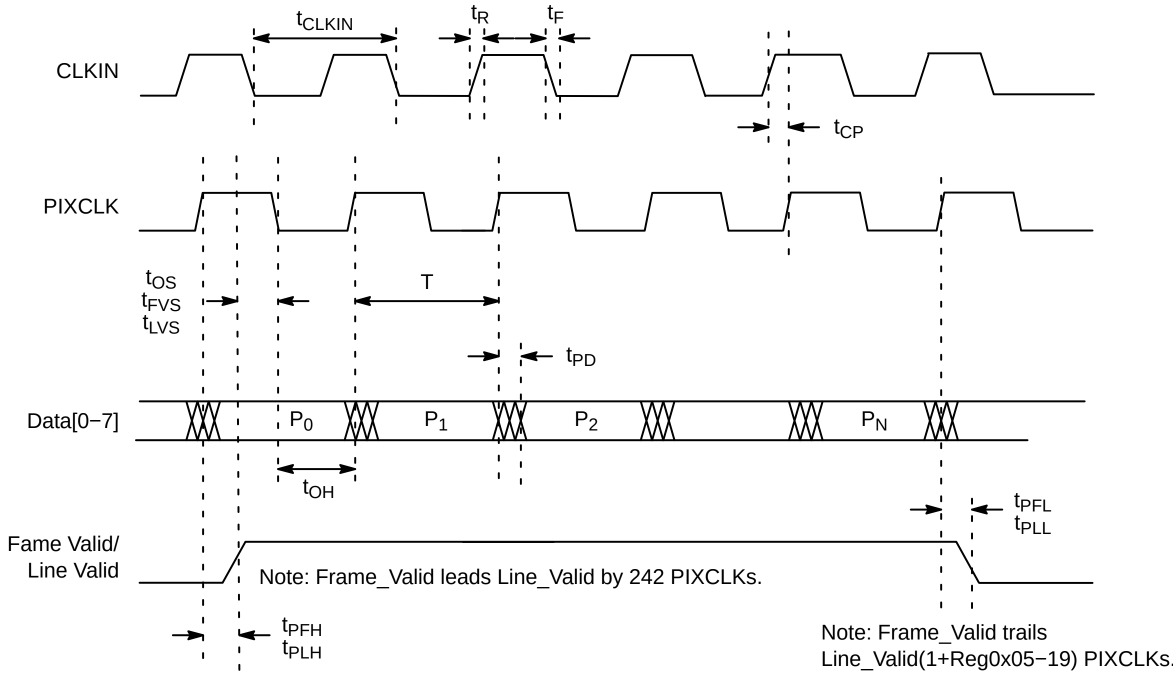


Figure 17. Data Output Timing Diagram

Table 7. DC ELECTRICAL CHARACTERISTICS
(DC Setup Conditions: f_{CLKIN} = 48 MHz, V_{DD} = 3.3 V, V_{AA} = 3.3 V, V_{AA}PIX = 3.3 V, T_A = 25°C)

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core Digital Voltage		3	3.3	3.6	V
V_{AA}	Analog Voltage		3	3.3	3.6	V
V_{AA}PIX	Pixel Supply Voltage		3	3.3	3.6	V
V_{IH}	Input High Voltage		V_{PWR} − 0.3		V_{PWR} + 0.3	V
V_{IL}	Input Low Voltage		−0.3		0.8	V
I_{IN}	Input Leakage Current	No Pull-up Resistor; V_{IN} = V_{DD} or D_{GND}	−15		15	μA
V_{OH}	Output High Voltage		V_{PWR} − 0.2		—	V
V_{OL}	Output Low Voltage				0.2	V
I_{OZ}	Tri-state Output Leakage Current		—		15	μA
I_{DD}	Digital Operating Current		—	20	24	mA
I_{AA}	Analog Operating Current		—	85	110	mA
	Pixel Supply Current		—	5	10	mA
I_{STDBYD}	Digital Standby Current	STDBY = V_{DD}, CLKIN = 0 MHz	—	9	20	μA
I_{STDBYD} w/CLK	Digital Standby Current	STDBY = V_{DD}, CLKIN = 48 MHz	—	55	125	μA
$I_{STDBYDA}$	Analog Standby Current	STDBY = V_{DD}	—	80	100	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 8. AC ELECTRICAL CHARACTERISTICS
(AC Setup Conditions: f_{CLKIN} = 48 MHz, V_{DD} = 3.3 V, V_{AA} = 3.3V, V_{AA}PIX = 3.3 V, Output Load = 30 pF, T_A = 25°C)

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_{CLKIIN}	Input Clock Frequency		1	−	48	MHz
t_{CLKIIN}	Input Clock Period		1000	−	20.83	ns
T	PIXCLK Period		1000	−	20.83	ns
t_R	Input Clock Rise Time		−	4	−	V/ns
t_F	Input Clock Fall Time		−	4	−	V/ns
	Clock Duty Cycle		45	50	55	%
t_{CP}	CLKIN to PIXCLK Propagation Delay		−	10	−	ns
t_{PD}	PIXCLK to Data Valid		−	−	1	ns
t_{PFH}	PIXCLK to FV High		−	−	7	ns
t_{PLH}	PIXCLK to LV High		−	−	7	ns
t_{PFL}	PIXCLK to FV Low		−	−	13	ns
t_{PLL}	PIXCLK to LV Low		−	−	13	ns
t_{OS}	Setup Time for Data before Falling Edge of PIXCLK		T/2 − 1	T/2	T/2 + 1	ns
t_{OH}	Hold Time for Data after Falling Edge of PIXCLK		T/2 − 1	T/2	T/2 + 1	ns
t_{FVS}	Setup Time for FV before Falling Edge of PIXCLK		2	3	−	ns
t_{LVS}	Setup Time for LV before Falling Edge of PIXCLK		2	3	−	ns
C_{LOAD}	Load Capacitance		−	−	30	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 9. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
T_{OP}	Operating Temperature	0	70	°C
T_{STG}	Storage Temperature	–40	125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Two-Wire Serial Bus Timing

The two-wire serial bus operation requires certain minimum master clock cycles between transitions. These are specified in the following diagrams in master clock cycles.

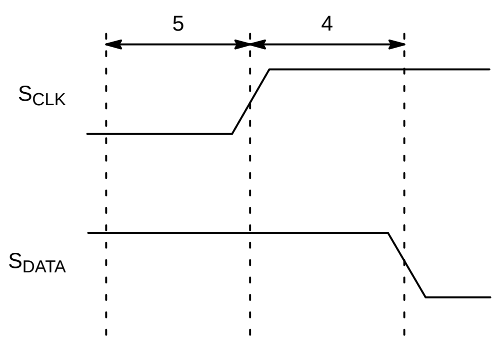
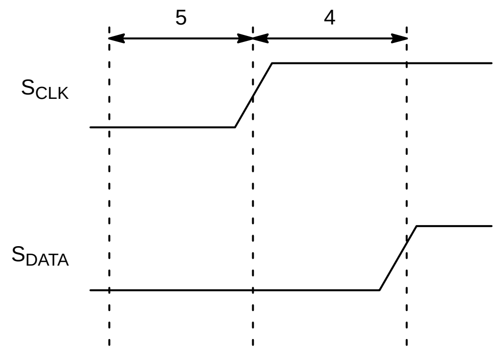
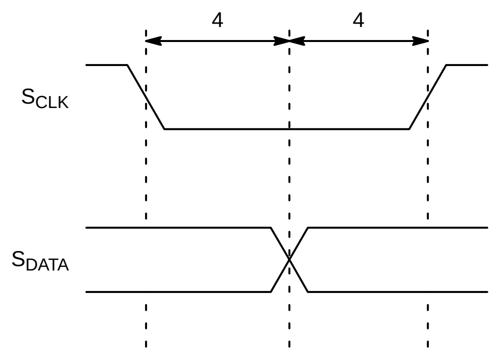


Figure 18. Serial Host Interface Start Condition Timing



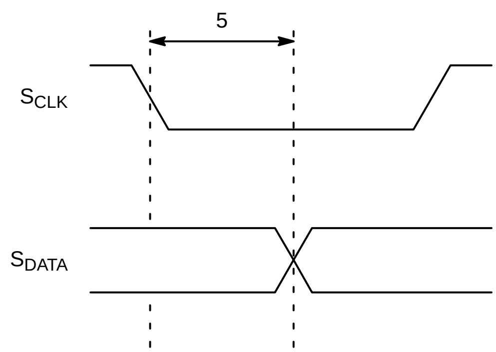
NOTE: All timing are in units of master clock cycle.

Figure 19. Serial Host Interface Stop Condition Timing



NOTE: S_{DATA} is driven by an off-chip transmitter.

Figure 20. Serial Host Interface Data Timing for WRITE



NOTE: S_{DATA} is pulled LOW by the sensor, or allowed to be pulled HIGH by a pull-up resistor off-chip.

Figure 21. Serial Host Interface Data Timing for READ

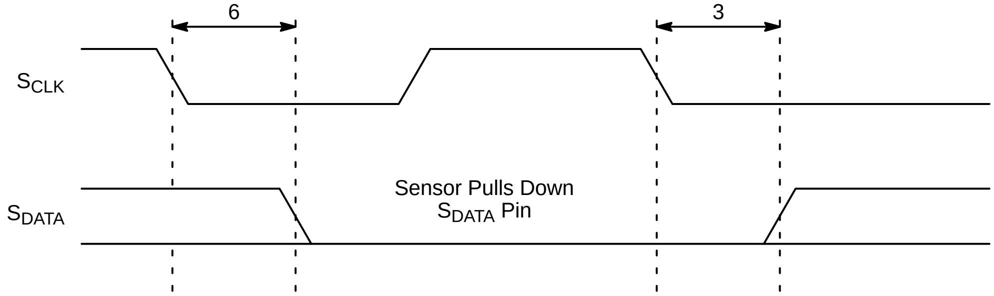
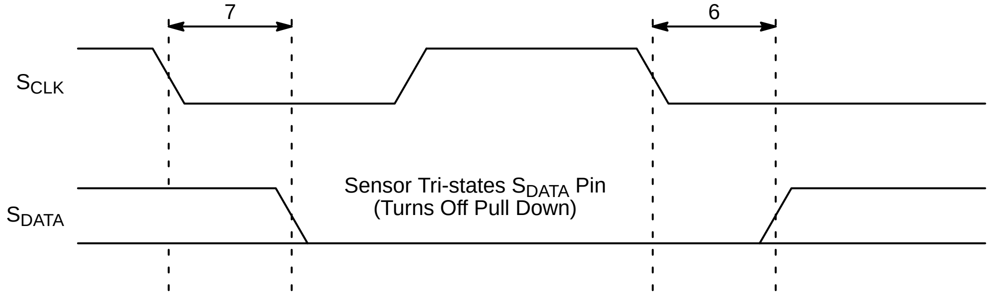


Figure 22. Acknowledge Signal Timing after an 8-bit WRITE to the Sensor



NOTE: After a read, the master receiver must pull down S_{DATA} to acknowledge receipt of data bits. When read sequence is complete, the master must generate a no acknowledge by leaving S_{DATA} to float HIGH. On the following cycle, a start or stop bit may be used.

Figure 23. Acknowledge Signal Timing after an 8-bit READ from the Sensor

Quantum Efficiency

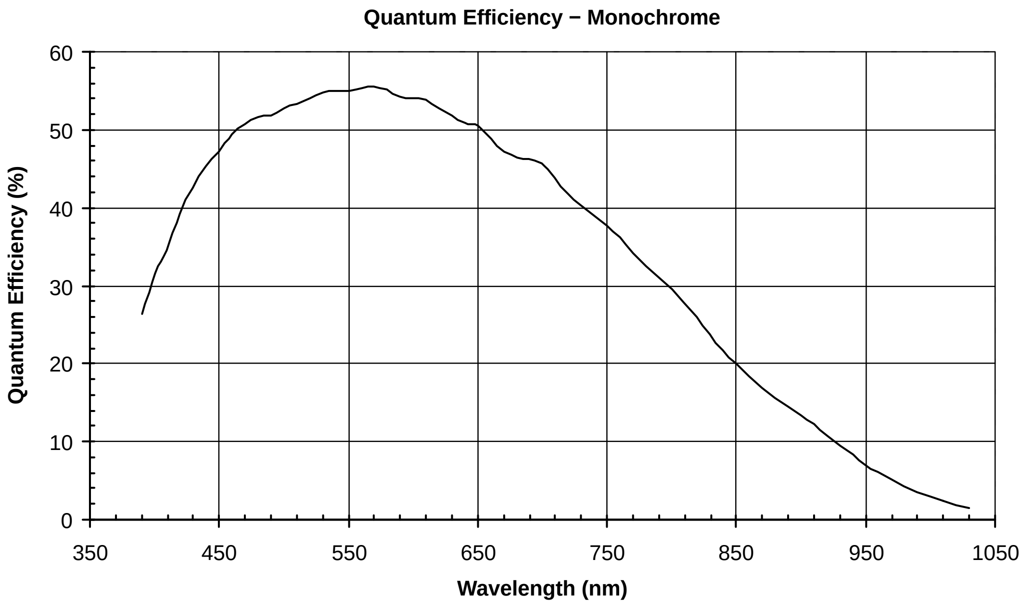


Figure 24. Quantum Efficiency − Monochrome

Image Center Offset and Orientation

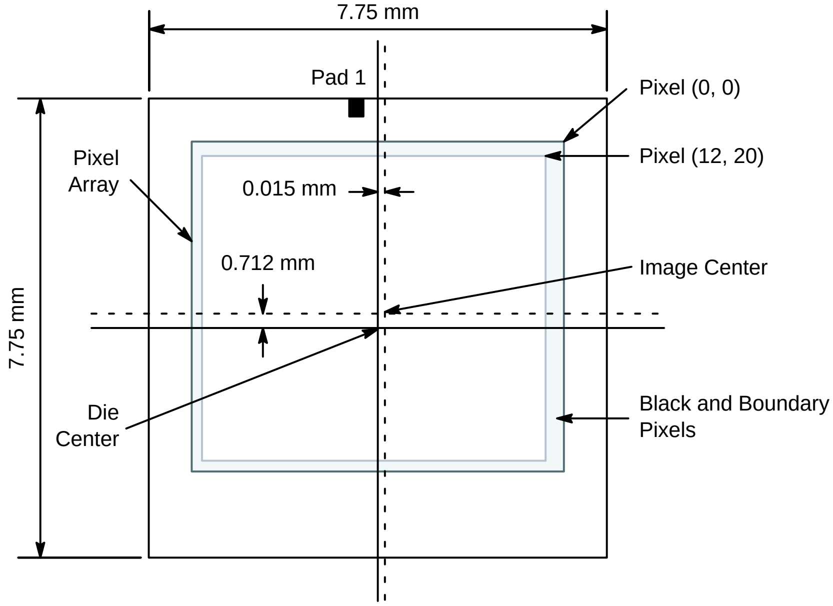


Figure 25. Image Center Offset

Table 10. OPTICAL AREA DIMENSIONS

Optical Area	Pixel	X-Dimension	Y-Dimension
SXGA	Center of Pixel (20, 12)	3,340.70 μm	3,372.45 μm
	Center of Pixel (1299, 1035)	−3,315.2 μm	−1,952.35 μm
Chip Size, mm	(Including Seal Ring)	7.75 mm	7.75 mm

1. X and Y coordinates referenced to center of die.
2. Die center = package center.
3. Image center offset from package center (x = 0.015 mm, y = 0.712 mm).

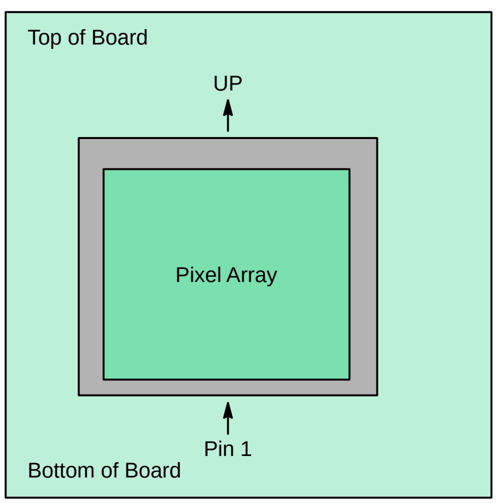
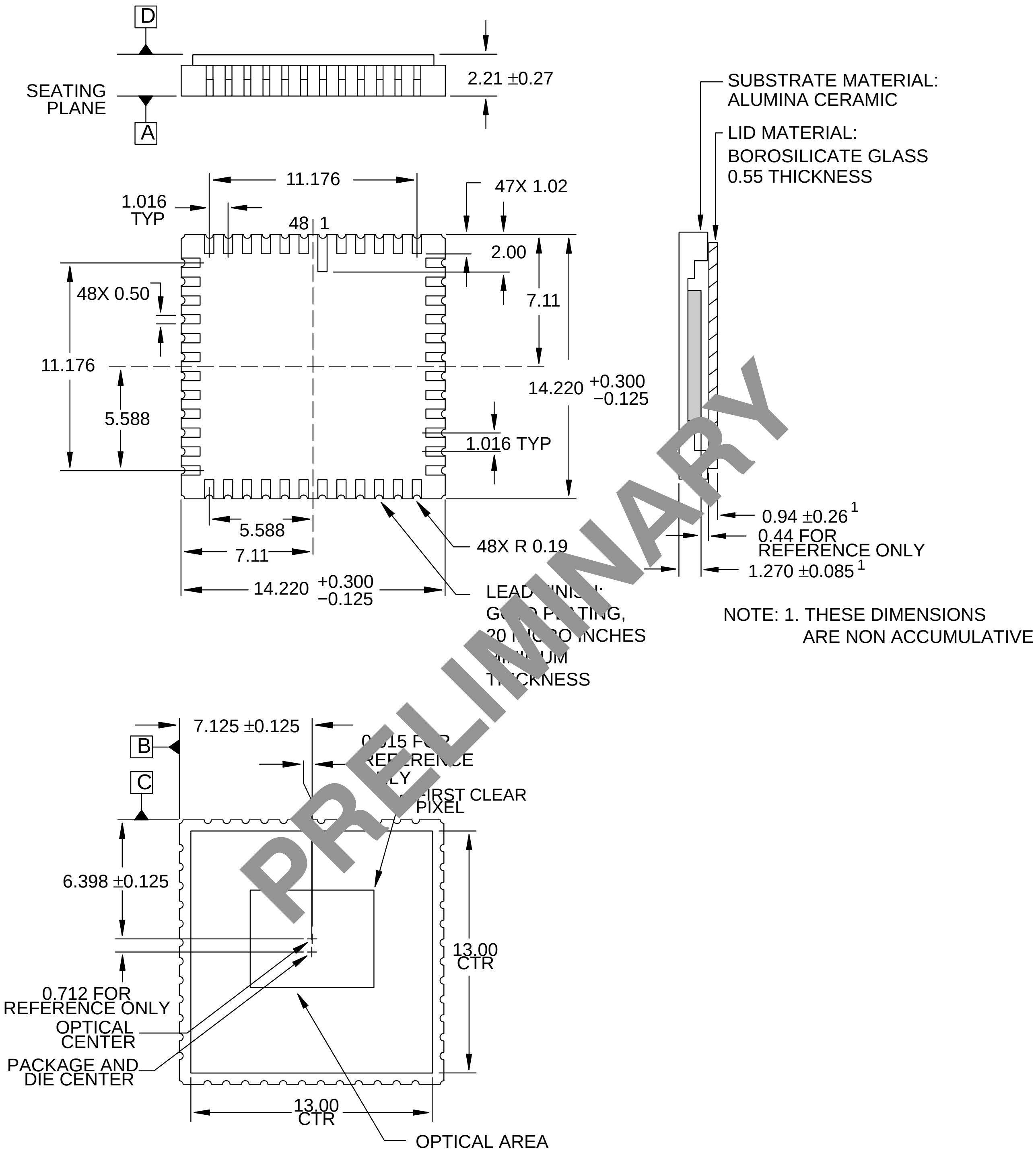


Figure 26. Optical Orientation

PACKAGE DIMENSIONS



MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES B AND C: 1º
MAXIMUM TILT OF OPTICAL AREA RELATIVE TO SEATING PLANE A: 50 MICRONS
MAXIMUM TILT OF OPTICAL AREA RELATIVE TO TOP OF COVER D: 50 MICRONS

Figure 27. 48-pin CLCC Package (Case 848AX)

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