1/2-Inch 3-Megapixel CMOS Digital Image Sensor

MT9T031

For the latest data sheet, refer to Aptina's Web site: www.aptina.com

Features

- High frame rate
- Global reset release
- Horizontal and vertical binning
- Column and row skip modes
- Superior low-light performance
- Low dark current
- Simple two-wire serial interface
- Programmable controls: Gain, frame rate, frame size, exposure
- Pin-for-pin compatible with Aptina's 1.3-megapixel MT9M001

Applications

- High resolution network cameras
- Wide field of view cameras
- Dome cameras with electronic pan, tilt, and zoom
- Hybrid video cameras with high resolution stills
- Detailed feature extraction for smart cameras

General Description

The Aptina® MT9T031 is a QXGA-format 1/2-inch CMOS active-pixel digital image sensor with an active imaging pixel array of 2,048H x 1,536V. It incorporates sophisticated camera functions on-chip such as windowing, column and row skip mode, and snapshot mode. It is programmable through a simple two-wire serial interface.

The 3-megapixel CMOS image sensor features Aptina's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

Table 1: Key Performance Parameters

Parameter		Typical Value
Optical format		1/2-inch (4:3)
Active imager size		6.55mm(H) x 4.92mm(V) 8.19 (Diagonal)
Active pixels		2,048H x 1,536V
Pixel size		3.2µm x 3.2µm
Color filter array		RGB Bayer pattern
Shutter type		Global reset release (GRR), electronic rolling shutter (ERS)
Maximum data rate/ master clock		48 MPS/48 MHz
Frame rate	QXGA (2,048 x 1,536)	Programmable up to 12 fps
	UXGA (1,600 x 1,200)	Programmable up to 20 fps
	HDTV (1,280 x 720)	Programmable up to 39 fps
	XGA (1,024 x 768)	Programmable up to 43 fps
	VGA (640 x 480)	Programmable up to 93 fps
ADC resolution		10-bit, on-chip
Responsivity		>1.0 V/lux-sec (550nm)
Dynamic range		61dB
SNR_{MAX}		43dB
Supply voltage		3.0V—3.6V (3.3V nominal)
Power consumption		244mW (nominal); 1.65µW (standby)
Operating temperature		0°C to 60°C
Packaging		48-pin CLCC

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9T031C12STC	48-Pin CLCC
MT9T031C12STCD ES	48-Pin CLCC demo
MT9T031C12STCH ES	48-Pin CLCC headboard

Table of Contents

List of Figures

List of Tables

General Description

The sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs a QXGA image at 12 frames per second (fps). An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

The MT9T031 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of consumer and industrial applications, including digital still cameras, digital video cameras, and PC cameras.

Figure 1: Block Diagram

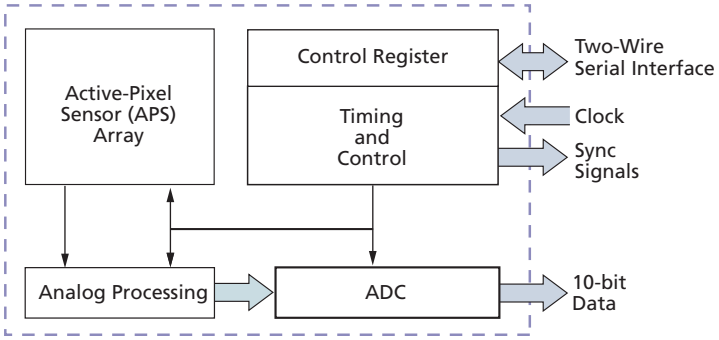
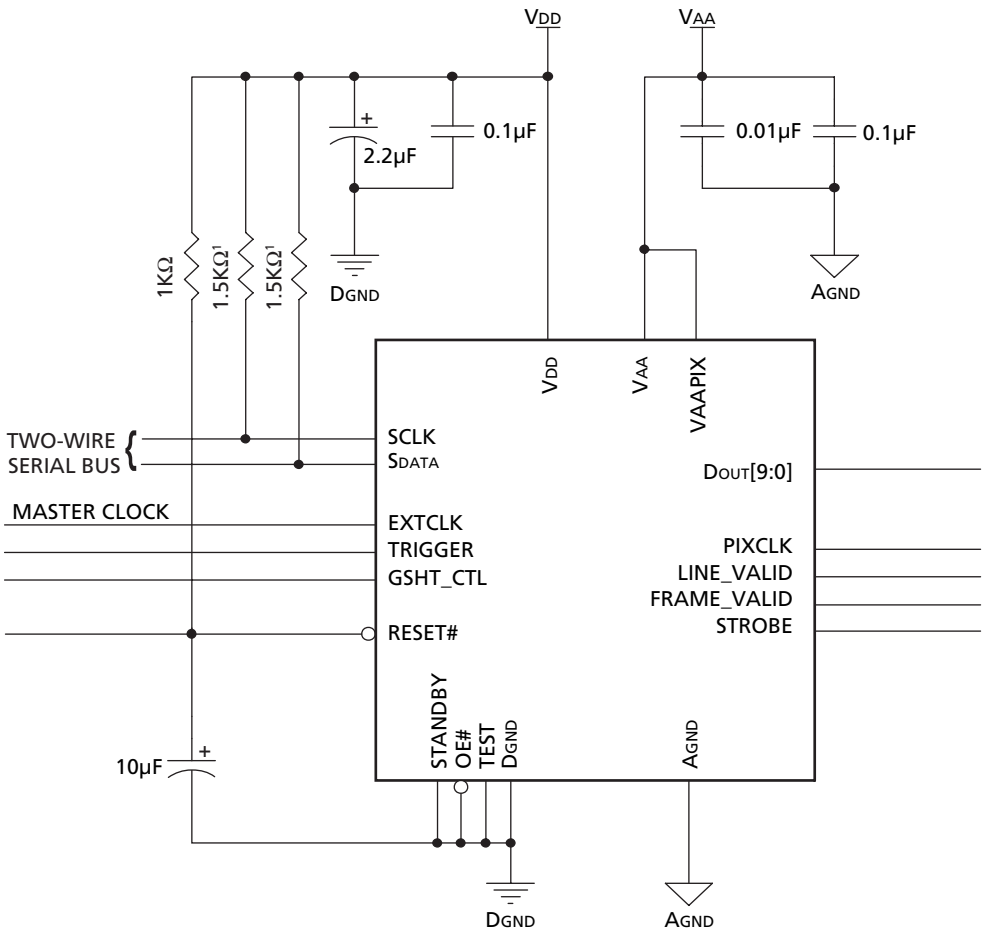


Figure 2: Typical Configuration (Connection)



Note: 1. Resistor value 1.5KΩ is recommended, but may be greater for slower two-wire speed.

Figure 3: 48-Pin CLCC

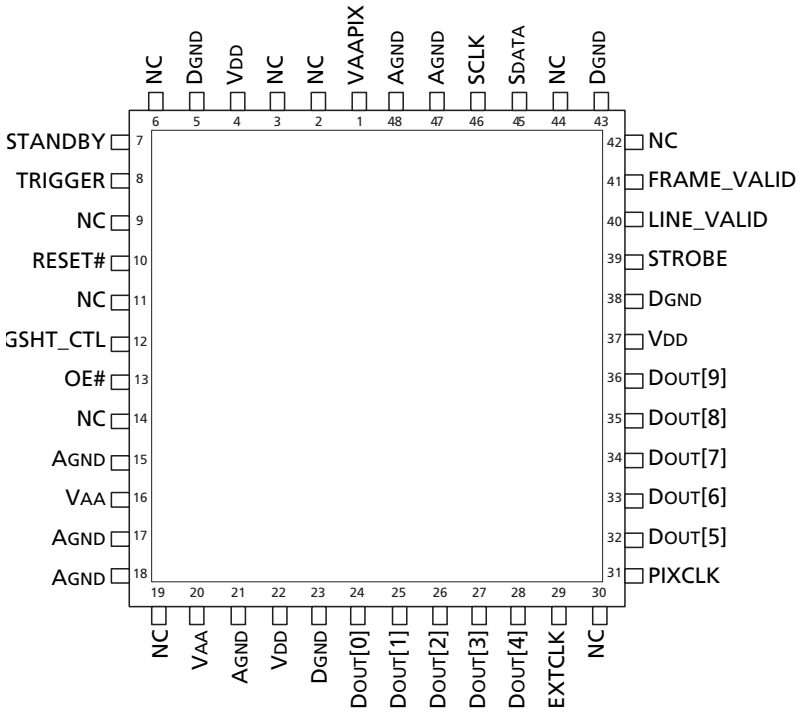


Table 3: Pin Descriptions

Pin Numbers	Symbol	Type	Description
7	STANDBY	Input	Standby: activates (HIGH) standby mode, disables analog bias circuitry for power saving mode.
8	TRIGGER	Input	Trigger: activates (HIGH) snapshot sequence.
10	RESET#	Input	Reset: activates (LOW) asynchronous reset of sensor. All registers assume factory defaults.
13	OE#	Input	Output enable: OE# when HIGH, places outputs DOUT[9:0], FRAME_VALID, LINE_VALID, PIXCLK, and STROBE into a tri-state configuration.
29	EXTCLK	Input	Clock in: master clock into sensor (48 MHz maximum).
46	SCLK	Input	Serial clock: clock for serial interface.
12	GSHT_CTL	Input	Global shutter control.
45	SDATA	I/O	Serial data: serial data bus, requires 1.5KΩ resistor to 3.3V for pull-up.
24, 25, 26, 27, 28, 32, 33, 34, 35, 36	DOUT[9:0]	Output	Data out: pixel data output bit 0, DOUT[9] (MSB), DOUT[0] (LSB).
31	PIXCLK	Output	Pixel clock: pixel data outputs are valid during falling edge of this clock. Frequency = (master clock).
39	STROBE	Output	Strobe: output is pulsed HIGH to indicate sensor reset operation of pixel array has completed.
40	LINE_VALID	Output	Line valid: output is pulsed HIGH during line of selectable valid pixel data (see R0x20 for options).
41	FRAME_VALID	Output	Frame valid: output is pulsed HIGH during frame of valid pixel data.
1	VAAPIX	Supply	Analog pixel power: provide power supply for pixel array, 3.3V ±0.3V.
4, 22, 37	VDD	Supply	Digital power: provide power supply for digital block, 3.3V ±0.3V.

Table 3: Pin Descriptions (Continued)

Pin Numbers	Symbol	Type	Description
5, 23, 38, 43	DGND	Supply	Digital ground: provide isolated ground for digital block.
16, 20	VAA	Supply	Analog power: provide power supply for analog block, 3.3V ±0.3V.
15, 17, 18, 21, 47, 48	AGND	Supply	Analog ground: provide isolated ground for analog block and pixel array.
2, 3, 6, 9, 11,14,19, 30 42, 44	NC	–	No connect: these pins must be left unconnected.

Pixel Data Format

Pixel Array Structure

The MT9T031 pixel array is configured as 2,112 columns by 1,568 rows, as shown in Figure 4. Columns from 0 through 27 and from 2,085 through 2,111 are optically black. Similarly, rows from 0 through 15 and from 1,561 through 1,567 are optically black. These optical black columns and rows can be used to monitor the black level. The black row data is used internally for the automatic black level adjustment. However, the black rows and columns can also be read out by setting R0x20 (11) and R0x1E (7), respectively. There are 2,057 columns by 1,545 rows of optically active pixels, which provides a four-pixel boundary around the QXGA (2,048 x 1,536) image to avoid boundary effects during color interpolation and correction.

The MT9T031 uses a Bayer color pattern, as shown in Figure 5. The even-numbered rows contain green and red color pixels, and odd-numbered rows contain blue and green color pixels. The even-numbered columns contain green and blue color pixels; odd-numbered columns contain red and green color pixels.

Figure 4: Pixel Array Description

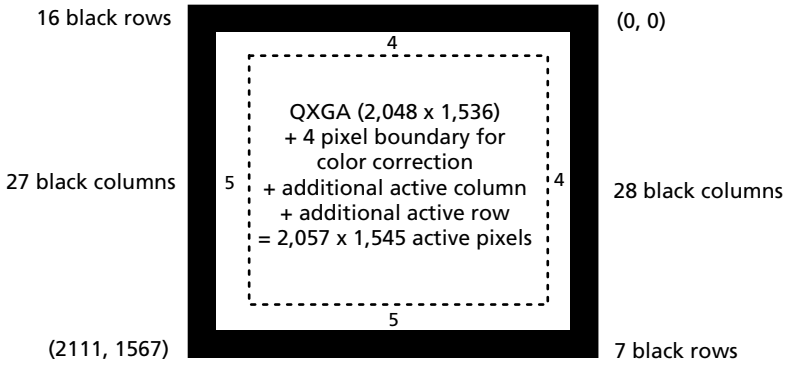
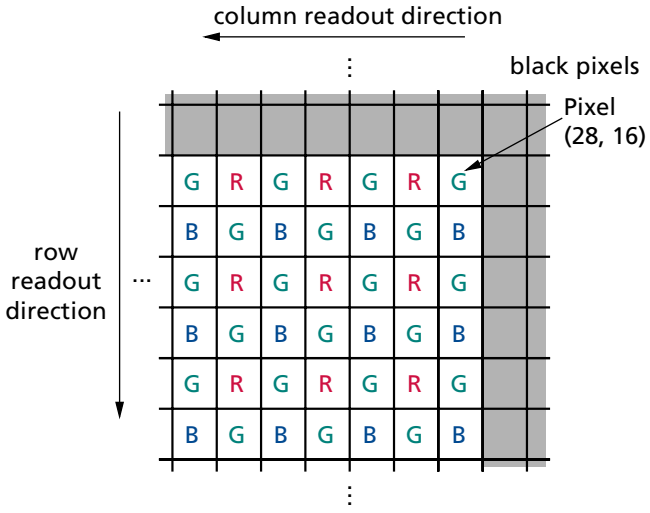


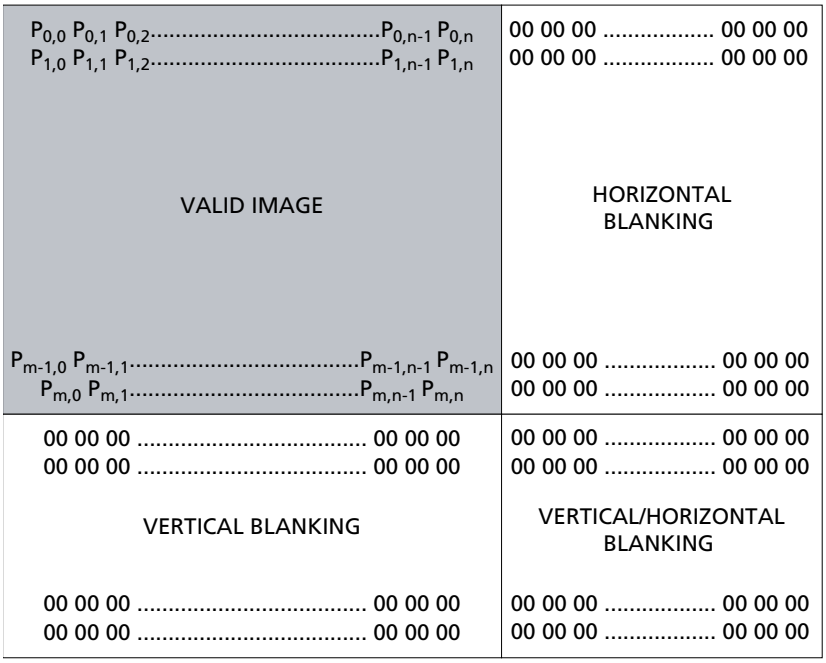
Figure 5: Pixel Color Pattern Detail (Top Right Corner)



Output Data Format

The MT9T031 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 6. The amount of horizontal blanking and vertical blanking is programmable through R0x05 and R0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. FRAME_VALID timing is described in "Output Data Timing" on page 11.

Figure 6: Spatial Illustration of Image Readout



Output Data Timing

The data output of the MT9T031 is synchronized with the PIXCLK output. When LINE_VALID is HIGH, one 10-bit pixel datum is output every PIXCLK period.

The PIXCLK can be used as a clock to latch the data. DOUT data is valid on the falling edge of PIXCLK in default mode. The PIXCLK is HIGH while master clock is HIGH and then LOW while master clock is LOW. It is continuously enabled, even during the blanking period. The parameters P, A, and Q shown in Figure 8 are defined in Table 4.

Figure 7: Timing Example of Pixel Data

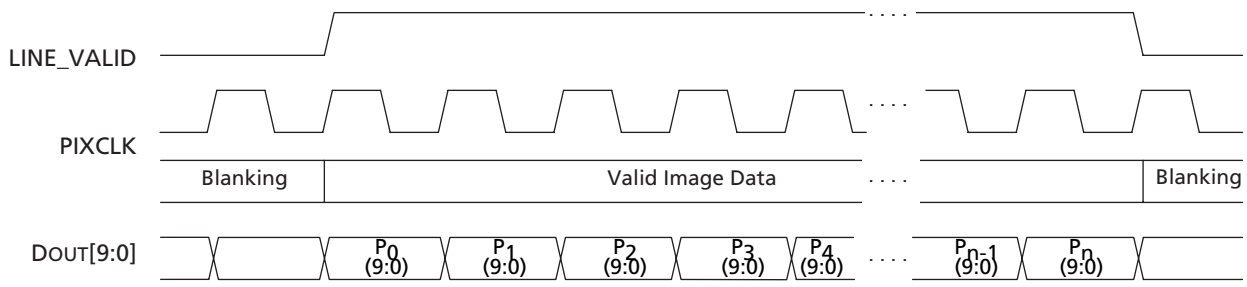
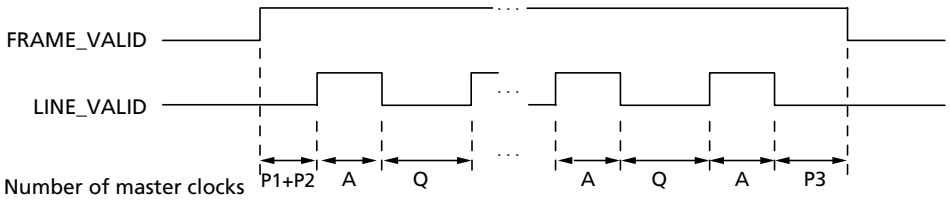


Figure 8: Row Timing and FRAME_VALID/LINE_VALID Signals



Frame Timing Formulas

Table 4: Frame Timing

Parameter	Name	Equation (Pixel Clocks = Master Clock)	Default Timing at 48 MHz
R	Active Rows	((R0x03 + 1)/((R0x22[2–0] + 1))) (rounded up to next even number)	1,536 pixel clocks = 32.0?s
A	Active Columns	((R0x04 + 1)/((R0x23[2–0] + 1))) (rounded up to next even number)	2,048 pixel clocks = 42.67?s
P1	Frame Start Blanking 1	331 if R0x22[5–4] = 0, normal 673 if R0x22[5–4] = 1, Bin 2X 999 if R0x22[5–4] = 2, Bin 3X	331pixel clocks = 6.89?s
P2	Frame Start Blanking 2	38 if R0x23[5–4] = 0, normal 22if R0x23[5–4] = 1, Bin 2X 14 if R0x23[5–4] = 2, Bin 3X	38 pixel clocks = 0.79?s
P3	Frame End Blanking 3	R0x05 (minimum R0x05 value = 21)	142 pixel clocks = 2.96?s
Q	Horizontal Blanking	P1 + P2 + P3	511 pixel clocks = 10.65?s
P4	Shutter Overhead	R0x0C + 316 x (R0x23[5–4] +1)	316 pixel clocks = 6.58?s
t_{ROW}	RowTime	The greater of: (A + Q) or (P1+ P4)	2,559 pixel clocks = 53.31?s
V	Vertical Blanking	(R0x06 + 1) x t_{ROW}	66,534 pixel clocks = 1.39ms
t_{FV}	Frame Valid Time	R x t_{ROW}	3,930,624 pixel clocks = 81.89ms
t_{FRAME}	Total Frame Time	The greater of: ((65536 x R0x08 + R0x09) x t_{ROW}) or (t_{FV} + V)	3,997,158 pixel clocks = 83.27ms

Register List and Default Values

Table 5: Core Registers

*1 = always 1; 0 = always 0; d = programmable; ? = read only

Register # Dec (Hex)	Register Description	Data Format (Binary)*	Default Value Dec (Hex)	Note
R0(R0x00)	Chip Version	???? ???? ???? ????	5665 (0x1621)	
R1(R0x01)	Row Start	0000 0ddd dddd dddd	20 (0x0014)	
R2(R0x02)	Column Start	0000 dddd dddd dddd	32 (0x0020)	
R3(R0x03)	Row Size	0000 0ddd dddd dddd	1535 (0x05FF)	
R4(R0x04)	Column Size	0000 dddd dddd dddd	2047 (0x07FF)	
R5(R0x05)	Horizontal Blanking	0000 0ddd dddd dddd	142 (0x008E)	
R6(R0x06)	Vertical Blanking	0000 0ddd dddd dddd	25 (0x0019)	
R7(R0x07)	Output Control	dddd dddd dddd dddd	2 (0x0002)	
R8(R0x08)	Shutter Width Upper	0000 0000 0000 dddd	0 (0x0000)	
R9(R0x09)	Shutter Width	dddd dddd dddd dddd	1561 (0x0619)	
R10(R0x0A)	Pixel Clock Control	dddd dddd dddd dddd	0 (0x0000)	
R11(R0x0B)	Frame Restart	0000 0000 0000 000d	0 (0x0000)	
R12(R0x0C)	Shutter Delay	0000 0ddd dddd dddd	0 (0x0000)	
R13(R0x0D)	Reset	0000 0000 0000 000d	0 (0x0000)	
R30(R0x1E)	Read Mode 1	dddd dddd dddd dddd	49216 (0xC040)	1, 2
R32(R0x20)	Read Mode 2	dddd dddd dddd dddd	8192 (0x2000)	
R33(R0x21)	Read Mode 3	0000 0000 0000 00dd	0 (0x0000)	
R34(R0x22)	Row Address Mode	dddd dddd dddd dddd	0 (0x0000)	
R35(R0x23)	Column Address Mode	0000 0ddd dddd dddd	0 (0x0000)	
R39(R0x27)	Reserved	—	1 (0x0001)	
R41(R0x29)	Reserved	—	1025 (0x0401)	
R43(R0x2B)	Green1 Gain	0ddd dddd dddd dddd	8 (0x0008)	
R44(R0x2C)	Blue Gain	0ddd dddd dddd dddd	8 (0x0008)	
R45(R0x2D)	Red Gain	0ddd dddd dddd dddd	8 (0x0008)	
R46(R0x2E)	Green2 Gain	0ddd dddd dddd dddd	8 (0x0008)	
R48(R0x30)	Reserved	—	0 (0x0000)	
R50(R0x32)	Test Data	0000 0ddd ddd dd00	0 (0x0000)	
R53(R0x35)	Global Gain	0ddd dddd dddd dddd	8 (0x0008)	
R60(R0x3C)	Reserved	—	16 (0x0010)	
R61(R0x3D)	Reserved	—	5 (0x0005)	
R62(R0x3E)	Reserved	—	3 (0x0003)	
R63(R0x3F)	Reserved	—	2 (0x0002)	
R64(R0x40)	Reserved	—	5 (0x0005)	
R65(R0x41)	Reserved	—	3 (0x0003)	
R66(R0x42)	Reserved	—	3 (0x0003)	
R67(R0x43)	Reserved	—	3 (0x0003)	
R68(R0x44)	Reserved	—	3 (0x0003)	
R69(R0x45)	Reserved	—	16 (0x0010)	
R70(R0x46)	Reserved	—	16 (0x0010)	
R71(R0x47)	Reserved	—	16 (0x0010)	
R72(R0x48)	Reserved	—	16 (0x0010)	
R73(R0x49)	Black Level	0000 dddd dddd dddd	168 (0x00A8)	

Table 5: Core Registers (Continued)

*1 = always 1; 0 = always 0; d = programmable; ? = read only

Register # Dec (Hex)	Register Description	Data Format (Binary)*	Default Value Dec (Hex)	Note
R74(R0x4A)	Reserved	—	16 (0x0010)	
R75(R0x4B)	Row Black Default Offset	0000 dddd dddd dddd	40 (0x0028)	
R76(R0x4C)	Reserved	—	48 (0x0030)	
R77(R0x4D)	Reserved	—	32 (0x0020)	
R78(R0x4E)	Reserved	—	16 (0x0010)	3
R79(R0x4F)	Reserved	—	20 (0x0014)	
R80(R0x50)	Reserved	—	32772 (0x8004)	
R81(R0x51)	Reserved	—	2 (0x0002)	
R82(R0x52)	Reserved	—	32772 (0x8004)	
R83(R0x53)	Reserved	—	2 (0x0002)	
R84(R0x54)	Reserved	—	16 (0x0010)	
R85(R0x55)	Reserved	—	16 (0x0010)	
R86(R0x56)	Reserved	—	32 (0x0020)	
R91(R0x5B)	Reserved	—	7 (0x0007)	
R92(R0x5C)	Reserved	—	1820 (0x071C)	
R93(R0x5D)	BLC Delta Thresholds	dddd dddd dddd dddd	11539 (0x2D13)	
R94(R0x5E)	Reserved	—	21348 (0x5364)	
R95(R0x5F)	Cal Thresholds	dddd dddd dddd dddd	8989 (0x231D)	
R96(R0x60)	Cal Green1 Offset	0000 000d dddd dddd	32 (0x0020)	
R97(R0x61)	Cal Green2 Offset	0000 000d dddd dddd	32 (0x0020)	
R98(R0x62)	Black Level Calibration	dddd dddd dddd dddd	0 (0x0000)	
R99(R0x63)	Red Offset	0000 000d dddd dddd	32 (0x0020)	
R100(R0x64)	Blue Offset	0000 000d dddd dddd	32 (0x0020)	
R101(R0x65)	Reserved	—	0 (0x0000)	
R103(R0x67)	Reserved	—	16383 (0x3FFF)	
R104(R0x68)	Reserved	—	0 (0x0000)	
R105(R0x69)	Reserved	—	0 (0x0000)	
R106(R0x6A)	Reserved	—	0 (0x0000)	
R107(R0x6B)	Reserved	—	0 (0x0000)	
R108(R0x6C)	Reserved	—	0 (0x0000)	
R109(R0x6D)	Reserved	—	0 (0x0000)	
R110(R0x6E)	Reserved	—	0 (0x0000)	
R112(R0x70)	Reserved	—	163 (0x00A3)	
R113(R0x71)	Reserved	—	41476 (0xA204)	
R114(R0x72)	Reserved	—	40966 (0xA006)	
R115(R0x73)	Reserved	—	9738 (0x260A)	
R116(R0x74)	Reserved	—	10252 (0x280C)	
R117(R0x75)	Reserved	—	21005 (0x520D)	
R118(R0x76)	Reserved	—	28756 (0x7054)	
R119(R0x77)	Reserved	—	0 (0x0000)	
R120(R0x78)	Reserved	—	40023 (0x9C57)	
R121(R0x79)	Reserved	—	40450 (0x9E02)	
R122(R0x7A)	Reserved	—	40452 (0x9E04)	
R123(R0x7B)	Reserved	—	40454 (0x9E06)	

Table 5: Core Registers (Continued)

*1 = always 1; 0 = always 0; d = programmable; ? = read only

Register # Dec (Hex)	Register Description	Data Format (Binary)*	Default Value Dec (Hex)	Note
R124(R0x7C)	Reserved	—	40966 (0xA006)	
R125(R0x7D)	Reserved	—	21256 (0x5308)	
R126(R0x7E)	Reserved	—	12808 (0x3208)	
R127(R0x7F)	Reserved	—	31826 (0x7C52)	
R128(R0x80)	Reserved	—	78 (0x004E)	
R129(R0x81)	Reserved	—	19968 (0x4E00)	
R130(R0x82)	Reserved	—	19458 (0x4C02)	
R131(R0x83)	Reserved	—	18444 (0x480C)	
R132(R0x84)	Reserved	—	18958 (0x4A0E)	
R134(R0x86)	Reserved	—	11788 (0x2E0C)	
R135(R0x87)	Reserved	—	0 (0x0000)	
R137(R0x89)	Reserved	—	19458 (0x4C02)	
R138(R0x8A)	Reserved	—	0 (0x0000)	
R139(R0x8B)	Reserved	—	20234 (0x4F0A)	
R140(R0x8C)	Reserved	—	14858 (0x3A0A)	
R144(R0x90)	Reserved	—	12 (0x000C)	
R145(R0x91)	Reserved	—	0 (0x0000)	
R146(R0x92)	Reserved	—	1 (0x0001)	
R241(R0xF1)	Reserved	—	0 (0x0000)	
R248(R0xF8)	Chip Enable	0000 0000 0000 00dd	1 (0x0001)	
R250(R0xFA)	Reserved	—	0 (0x0000)	
R251(R0xFB)	Reserved	—	0 (0x0000)	
R252(R0xFC)	Reserved	—	0 (0x0000)	
R253(R0xFD)	Reserved	—	0 (0x0000)	
R255(R0xFF)	Chip Version [Dup]	???? ???? ???? ????	5665 (0x1621)	

Note: 1. It is recommended that bit 14 be cleared.
2. Value 0x8040 is recommended.
3. Value of 0x20 is recommended.

Sensor Core Register Descriptions

Table 6: Core Registers

Reg. #	Bits	Default	Name
R0 R0x00	15:0	0x1621	Chip Version (RO)
	Chip version.		
R1 R0x01	15:0	0x0014	Row Start (RW)
	The first row to be read out, excluding any dark rows that may be read. To window the image down, set this register to the starting "Y" value. Setting a value less than 20 is not recommended because the dark rows should be read using R0x22.		
R2 R0x02	15:0	0x0020	Column Start (RW)
	The first column to be read out, excluding dark columns that may be read. To window the image down, set this register to the starting X value. Setting a value below 96 is not recommended because readout of dark columns should be controlled by R0x22.		
R3 R0x03	15:0	0x05FF	Row Size (RW)
	Number of rows in the image to be read out, excluding any dark rows or border rows that may be read. The minimum supported value is 2.		
R4 R0x04	15:0	0x07FF	Column Size (RW)
	Number of columns in the image to be read out, excluding any dark columns or border columns that may be read. The minimum supported value is 17.		
R5 R0x05	15:0	0x008E	Horizontal Blanking (RW)
	Horizontal Blank—default = 0x008E (142 pixels). Minimum value = 0x0015 (21).		
R6 R0x06	15:0	0x0019	Vertical Blanking (RW)
	Vertical Blank—default = 0x0019 (25 rows). Minimum value = 0x0003 (3).		
R7 R0x07	15:0	0x0002	Output Control (RW)
	15	0x0000	Reserved
	14	0x0000	Reserved
	13:9	X	Reserved
	8	0x0000	Reserved
	7	X	Reserved
	6	0x0000	Override pixel data Override pixel data. 0 = normal operation. 1 = output programmed test data (see R0x32). First valid columns will output contents of test data register; second columns will output inverted data. Third columns will output noninverted data, fourth inverted, etc.
	5:4	0x0000	Reserved
	3	0x0000	Reserved
	2	0x0000	Reserved
	1	0x0001	Chip Enable Chip Enable. 1 = normal operation. 0 = sensor readout is stopped and analog control signals are put in a state which draws minimal power.
R7 R0x07	0	0x0000	Sync changes Synchronize changes. 0 = normal operation, update changes to registers that affect image brightness (integration time, shutter delay, gain, horizontal and vertical blank, window size, row/column skip, or row mirror) at the next frame boundary. 1 = do not update any changes to these settings until this bit is returned to "0."
	This register controls various features of the output format for the sensor.		

Table 6: Core Registers (Continued)

Reg. #	Bits	Default	Name
R8 R0x08	15:0	0x0000	Shutter Width Upper (RW)
	The most significant bits of the shutter width, which are combined with Shutter Width (R0x09). The total shutter width is therefore: (((Shutter_Width_Upper) x 65536) + Shutter_Width). This should allow a shutter width from about 50us to about 50s at default row time.		
R9 R0x09	15:0	0x0619	Shutter Width (RW)
	Integration time in number of rows. The integration time is also influenced by the shutter delay (R0x0C) and the overhead time.		
R10 R0x0A	15:0	0x0000	Pixel Clock Control (RW)
	15	0x0000	Invert Pixel CLock
	14:11	X	Reserved
	10:8	0x0000	Shift pixel clock
	7	X	Reserved
	6:0	0x0000	Divide pixel clock
R11 R0x0B	15:0	0x0000	Frame Restart (RW)
	Setting bit 0 to “1” of R0x0B will cause the sensor to abandon the readout of the current frame and restart from the first row. This register automatically resets itself to 0x0000 after the frame restart. The first frame after this event is considered to be a "bad frame" (see description for R0x20, bit 0).		
R12 R0x0C	15:0	0x0000	Shutter Delay (RW)
	The amount of time from the end of the sampling sequence to the beginning of the pixel reset sequence. If the value in this register exceeds the row time, the reset of the row does not complete before the associated row is sampled, and the sensor does not generate an image. A programmed value of N reduces the integration time by (N/2) pixel clock periods in low power mode and by N pixel clock periods in full power mode.		
R13 R0x0D	15:0	0x0000	Reset (RW)
	Setting this bit will put the sensor into reset mode, which will set the sensor to its default power-up state. Clearing this bit will resume normal operation.		
R30 R0x1E	15:0	0xC040	Read Mode 1 (RW)
	15	0x0001	Reserved
	14	0x0001	Reserved
	13	0x0000	Reserved
	12	0x0000	Reserved
	11	0x0000	Strobe override Strobe Override—default is 0 (strobe signal created by digital logic). 1 = override strobe signal (strobe signal is set high when this bit is set, low when this bit is set low. It is assumed that strobe enable is set to “0” if strobe override is being used).

Table 6: Core Registers (Continued)

Reg. #	Bits	Default	Name
R30 R0x1E	10	0x0000	Strobe width Strobe Width—default is 0 (strobe signal width at minimum length, one row of integration time, prior to Line_Valid going high). 1 = extend strobe width (strobe signal width extends to entire time all rows are integrating; shutter width must be >= row size + vertical blanking).
	9	0x0000	Strobe enable Strobe Enable—default is 0 (no strobe signal). 1 = enable strobe (signal output from the sensor during the time all rows are integrating). See strobe width for more information.
	8	0x0000	Snap Shot Mode Snapshot Mode—default is 0 (continuous mode). 1 = enable Snapshot trigger signal can come from outside signal (trigger pin 8 on the sensor) or from serial interface register restart, i.e. programming a “1” to bit 0 of R0x0B.
	7	0x0000	Show dark columns
	6	0x0001	Noise suppression
	5:0	0x0000	Reserved
R32 R0x20	15:0	0x2000	Read Mode 2 (RW)
	15	0x0000	Mirror row
	14	0x0000	Mirror Column
	13	0x0001	Reserved
	12	0x0000	Reserved
	11	0x0000	Read dark rows
	10	0x0000	xor line_valid 1 = LINE_VALID = "Continuous" LINE_VALID XOR FRAME_VALID. 0 = LINE_VALID determined by bit 9 (default).
	9	0x0000	Continuous line valid 1 = "Continuous" LINE_VALID (continue producing Line_Valid during vertical blanking). 0 = Normal Line_Valid (default, no Line_Valid during vertical blank).
	8:2	0x0000	Reserved
	1	0x0000	Reserved
	0	0x0000	No bad frames No bad frames—1 = output all frames (including bad frames). 0 = default, only output good frames. A bad frame is defined as the first frame following a change to: window size or position, horizontal blanking, row or column skip, or mirroring.
R33 R0x21	15:0	0x0000	Read Mode 3 (RW)
	15:2	X	Reserved
	1	0x0000	Use GSHT_CTL Use GSHT_CTL—default = 0x0000. When set, the leading edge of the GSHT_CTL pad signal will be used to start the shutter sequence in snapshot mode, and the trailing edge will start the read sequence. When clear, the leading edge of the TRIGGER pad signal will be used to initiate the shutter sequence, the trailing edge of GSHT_CTL will start the exposure, and the trailing edge of the TRIGGER pad signal will be used to start the strobe and readout. Ineffective unless Snapshot (R0x1E[8]) and Global Reset are set.
	0	0x0000	Global Reset Global Reset—default = 0x0000—when set, snapshot mode will make use of the global reset — that is, the entire array will be released from reset simultaneously. Ineffective unless Snapshot (R0x1E[8]) is set.

Table 6: Core Registers (Continued)

Reg. #	Bits	Default	Name
R34 R0x22	15:0	0x0000	Row Address Mode (RW)
	15	X	Reserved
	14:12	0x0000	Reserved
	11	X	Reserved
	10:8	0x0000	Reserved
	7	X	Reserved
	6:4	0x0000	Reserved
	3	X	Reserved
	2:0	0x0000	Row Skip Row Skip—the number of row-pairs to skip for every row read. For example, "0" means read every row pair. "1" is skip 2X; 2 is skip 3X, etc. If Row Bin is non-zero, this should be set to the interval between the first rows in each bin. For full binning, Row Skip equals Row Bin.
R35 R0x23	15:0	0x0000	Column Address Mode (RW)
	15:11	X	Reserved
	10:8	0x0000	Reserved
	7:6	X	Reserved
	5:4	0x0000	Column Bin, Column Bin—the number of columns to be addressed per column read out minus one. Zero will produce standard 1:1 read out. A value of "1" will produce Bin 2X; "2" would be Bin 3X. Note: Column start address value must be a multiple of R0x23 [5-4] + 1.
	3	X	Reserved
	2:0	0x0000	Column Skip Column Skip—the number of column-pairs to skip for every pair read. Zero means read every column. "1" means skip one pair for every pair read (Skip 2X); 2 means skip 2 pairs for every pair read (Skip 3X) etc.
R43 R0x02B	15:0	0x0008	Green1 Gain (RW)
	15	X	Reserved
	14:8	0x0000	Digital Green1 Gain Green1 digital gain—default = 0x00 (0) = 1x gain.
	7	X	Reserved
	6	0x0000	Double Green1 Gain Green1 analog gain—default = 0x08 (8) = 1x gain.
	5:0	0x0008	Green1 Gain Value Green1 analog gain—default = 0x08 (8) = 1x gain.
R44 R0x2C	15:0	0x0008	Blue Gain (RW)
	15	X	Reserved
	14:8	0x0000	Digital Blue Gain Blue digital gain—default = 0x00 (0) = 1x gain.
	7	X	Reserved
	6	0x0000	Double Blue Gain Blue analog gain—default = 0x08 (8) = 1x gain.
	5:0	0x0008	Blue Gain Value Blue analog gain—default = 0x08 (8) = 1x gain.

Table 6: Core Registers (Continued)

Reg. #	Bits	Default	Name
R45 R0x2D	15:0	0x0008	Red Gain (RW)
	15	X	Reserved
	14:8	0x0000	Digital Red Gain Red digital gain—default = 0x00 (0) = 1x gain.
	7	X	Reserved
	6	0x0000	Double Red Gain Red analog gain—default = 0x08 (8) = 1x gain.
	5:0	0x0008	Red Gain Value Red analog gain—default = 0x08 (8) = 1x gain.
R46 R0x2E	15:0	0x0008	Green2 Gain (RW)
	15	X	Reserved
	14:8	0x0000	Digital Green2 Gain Green2 digital gain—default = 0x00 (0) = 1x gain.
	7	X	Reserved
	6	0x0000	Double Green2 Gain Green2 analog gain—default = 0x08 (8) = 1x gain.
	5:0	0x0008	Green2 Gain Value Green2 analog gain—default = 0x08 (8) = 1x gain.
R50 R0x32	15:0	0x0000	Test Data (RW)
	11:2	0x0000	Test Data The data inserted into the data path to produce test pattern when "Use Test Data" (R0x07, bit 6) is set. Test Data will be inserted for even columns, and the inverse will be inserted for odd columns.
R53 R0x35	15:0	0x0008	Global Gain (RW)
	15	X	Reserved
	14:8	0x0000	Digital Global Gain Global digital gain—default = 0x00 (0) = 1x gain. This register can be used to set all four gains at once. When read, it will return the value stored in R0x2B.
	7	X	Reserved
	6	0x0000	Double Global Gain Global analog gain—default = 0x08 (8) = 1x gain.
	5:0	0x0008	Global Gain Value This register can be used to simultaneously set all four gains. When read, it returns the value stored in R0x2B.
R73 R0x49	15:0	0x00A8	Black Level (RW)
	Desired black level in image.		
R75 R0x4B	15:0	0x0028	Row Black Default Offset (RW)
R93 R0x5D	15:0	0x2D13	BLC Delta Thresholds (RW)
	15	X	Reserved
	14:8	0x002D	High Delta Threshold High Coarse Threshold—default = 0x2D. If the average black value for a color is higher than this value or lower than Low Coarse Threshold, the coarse mode will be activated (if enabled). Once the black level is between the High Coarse Threshold and the Low Coarse Threshold, the fine method will be used. This value should be set no lower than High Target Threshold.
	7	X	Reserved
	6:0	0x0013	Low Delta Threshold Low Coarse Threshold—default = 0x13. This value should be less than Low Target Threshold. See High Coarse Threshold below.

Table 6: Core Registers (Continued)

Reg. #	Bits	Default	Name
R95 R0x5F	15:0	0x231D	Cal Thresholds (RW)
	15	X	Reserved
	14:8	0x0023	High Target Upper threshold for targeted black level in ADC LSBs.
	7	X	Reserved
	6:0	0x001D	Low Target Lower threshold for targeted black level in ADC LSBs.
R96 R0x60	15:0	0x0020	Cal Green1 Offset (RW)
	Analog calibration offset for green1 pixels, represented as a two's complement signed 8-bit value (if bit 8 is clear, the offset is positive and the magnitude is given by bits 7:0. If bit 8 is set, the offset is negative and the magnitude is given by not ([7:0]) + 1). If R0x60[0] = 0, this register is R/O and returns the current value computed by the black level calibration algorithm. If R0x60[0] = 1, this register is R/W and can be used to set the calibration offset manually. Green1 pixels share rows with red pixels.		
R97 R0x61	15:0	0x0020	Cal Green2 Offset (RW)
	Analog calibration offset for green2 pixels, represented as a two's complement signed 8-bit value (if bit 8 is clear, the offset is positive and the magnitude is given by bits 7:0. If bit 8 is set, the offset is negative and the magnitude is given by not ([7:0]) + 1.) If R0x60[0] = 0, this register is R/O and returns the current value computed by the black level calibration algorithm. If R0x60[0] = 1, this register is R/W and can be used to manually set the calibration offset. Green2 pixels share rows with blue pixels.		
R98 R0x62	15:0	0x0000	Black Level Calibration (RW)
	15	0x0000	Disable Fast Sample
	14	0x0000	Lock Green Calibration Lock Green Calibration—when set, only one calibration value will be used for both Green1 and Green2 channels. Default is 0, set to "0" at all times. Note: Gain for Green1 and Green2 channels must be equal for setting to be effective.
R98 R0x62	13	0x0000	Lock Red/Blue Calibration Lock Red/Blue Calibration—when set, only one calibration value will be used for both red and blue channels. Default is 0, set to "0" at all times. Note: Gain for Red and Blue channels must be equal for setting to be effective.
	12	0x0000	Recalculate BL Recalculate Black Level—1 = start a new running digitally filtered average for the black level (this is internally reset to "0" immediately), and do a rapid sweep to find the new starting point. 0 = normal operation (default).
	11	0x0000	Disable Binary search
	10:9	X	Reserved
	8	0x0000	Reserved
	7	0x0000	Reserved
	6:5	0x0000	Reserved
	4:3	0x0000	Reserved
	2	X	Reserved
	1	0x0000	Disable calib Force/disable black level calibration. 0 = Enable Offset Correction (default). 1 = disable Offset Correction Voltage (Offset Correction Voltage = 0.0V).
	0	0x0000	Manual override Manual override of black level correction. 1 = override automatic black level correction with programmed values. 0 = normal operation (default).

Table 6: Core Registers (Continued)

Reg. #	Bits	Default	Name
R99 R0x63	15:0	0x0020	Red Offset (RW)
	Analog calibration offset for red pixels, represented as a two's complement signed 8-bit value (if bit 8 is clear, the offset is positive and the magnitude is given by bits 7:0. If bit 8 is set, the offset is negative and the magnitude is given by not([7:0]) + 1). If R0x60[0] = 0, this register is R/O and returns the current value computed by the black level calibration algorithm. If R0x60[0] = 1, this register is R/W and can be used to manually set the calibration offset.		
R100 R0x64	15:0	0x0020	Blue Offset (RW)
	Analog calibration offset for blue pixels, represented as a two's complement signed 8-bit value (if bit 8 is clear, the offset is positive and the magnitude is given by bits 7:0. If bit 8 is set, the offset is negative and the magnitude is given by not ([7:0]) + 1). If R0x60[0] = 0, this register is R/O and returns the current value computed by the black level calibration algorithm. If R0x60[0] = 1, this register is R/W and can be used to set the calibration offset manually.		
R248 R0xF8	15:0	0x0001	Chip Enable (RW)
	15:2	X	Reserved
	1	0x0000	Synchronize changes Mirrors the functionality of R0x07 bit 0 (Synchronize changes). 0 = normal operation, update changes to registers that affect image brightness (integration time, integration delay, gain, horizontal and vertical blank, window size, row/column skip, or row/column mirror) at the next frame boundary. 1 = do not update any changes to these settings until this bit is returned to "0."
	0	0x0001	CE Mirrors the functionality of R0x07 bit 1,(Chip Enable). 1 = normal operation. 0 = stop sensor read out. When this is returned to "1," sensor read out restarts at the starting row in a new frame.
R255 R0xFF	15:0	0x1621	Chip Version (RO)
	Chip version.		

Feature Description

Window Control

R0x01, R0x02, R0x03, and R0x04

These registers control the size of the window.

Window Size

The default programmed window size is 2,048 columns by 1,536 rows (2,048H x 1,536V). The control logic allows the flexibility to change the window size by programming R0x03 and R0x04. R0x03 controls the window height (number of rows) and R0x04 controls the window width (number of columns). The value to be programmed in R0x03 is the desired number of rows -1. The value to be programmed in R0x04 is the desired number of columns -1.

The minimum value for R0x03 is 0x0001; for R0x04, 0x0001. Thus, the smallest window size is two columns by two rows (2H x 2V). The value of R0x03 and R0x04 must be an odd number (there can only be even number of columns). The user can program the window size to be any format desired. Table 7 shows examples of register settings to achieve various resolutions and frame rates.

Table 7: Standard Resolutions

Resolution	Frame Rate	Column_Size (R0x04)	Row_Size (R0x03)	Shutter Width (R0x09)
2,048 x 1,536 QXGA	12 fps	2,047	1,535	<1,552
1,600 x 1,200 UXGA	20 fps	1,599	1,199	<1,216
1,280 x 1,024 SXGA	27 fps	1,279	1,023	<1,040
1,024 x 768 XGA	43 fps	1,023	767	<784
800 x 600 SVGA	65 fps	799	599	<616
640 x 480 VGA	93 fps	639	479	<496

Table 8: Wide Screen (16:9) Resolutions

Resolution	Frame Rate	Column_Size (R0x04)	Row_Size (R0x03)	Shutter Width (R0x09)
1,920 x 1,080 HDTV	18 fps	1,919	1,079	<1,096
1,280 x 720 HDTV	39 fps	1,279	719	<736

Note: For Table 7 and Table 8 above, the settings for R0x05 (horizontal blanking) and R0x06 (vertical blanking) are 21 and 15 respectively, while all of the registers are set to default.

Electronic Panning

In addition to changing the window size, the user has the flexibility to change the location of the readout window. R0x01 controls the first row to be read out and R0x02 controls the first column to be read out. The default values are 0x0014 (decimal 20) for R0x01 and 0x0020 (decimal 32) for R0x02. The first column to be read out must be an even number.

R0x01 and R0x02, together with R0x03 and R0x04, allow the user to choose any segment of the imager array to be read out. This is especially beneficial when the user needs to zoom in on a small portion of the image and perform analysis on the image content.

Figure 9 shows some examples of the electronic panning/zoom-in and windowing capabilities of the sensor.

Blanking Control

R0x05 and R0x06

These registers control the blanking time in a row (called column fill-in or horizontal blanking) and between frames (vertical blanking). Horizontal blanking is specified in terms of pixel clocks. Vertical blanking is specified in terms of row readout times. The actual imager timing can be calculated using the equations given in Table 4 on page 12.

R0x05 controls the horizontal blanking time in a row. The value is specified in terms of pixel clocks. Default value of 0x008E for R0x05 results in a horizontal blanking time of 511 pixel clocks. The minimum value for R0x05 is 21. Thus, the minimum horizontal blanking time is 390 pixel clocks.

R0x06 controls the vertical blanking time in a row. The value is specified in terms of the number of rows. Default value of 0x0019 for R0x06 results in a vertical blanking time of 26-row time.

Frame Time

R0x03, R0x04, R0x05, and R0x06

Total frame time in terms of pixel clocks can be obtained using the formula given in Table 4 on page 12. The user can change the number of columns and rows read out, horizontal blanking and vertical blanking times to obtain different frame rates.

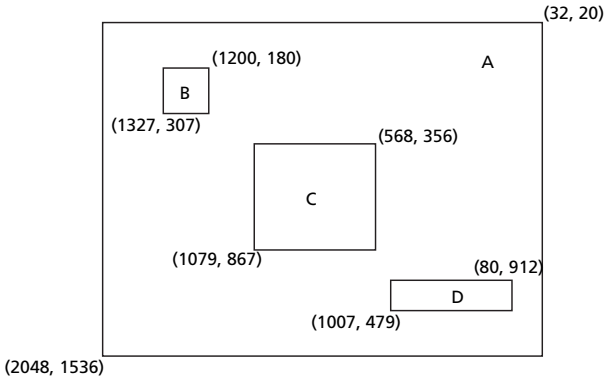
High Frame Rate Readout Modes

R0x01, R0x02, R0x03, R0x04, R0x05, and R0x06

In addition to having the flexibility to read out smaller standard formats, the sensor gives the user the option of reading out nonstandard formats. This is particularly useful if the user needs to zoom in on a particular segment of the image to perform high-speed mathematical calculations (e.g., high-speed viewfinder or auto focus applications).

In applications such as the auto focus mode, the user may need more horizontal resolution than vertical. Thus, the user can window down to the mid-section of the imager array by programming R0x01 and R0x03 to change the row start address and the window height. Figure 10 is an example of how the user may want to window down to 2,048H x 512V from the default of 2,048H x 1,536V. See also Table 9 for other auto focus mode resolutions.

Figure 9: Windowing Capabilities

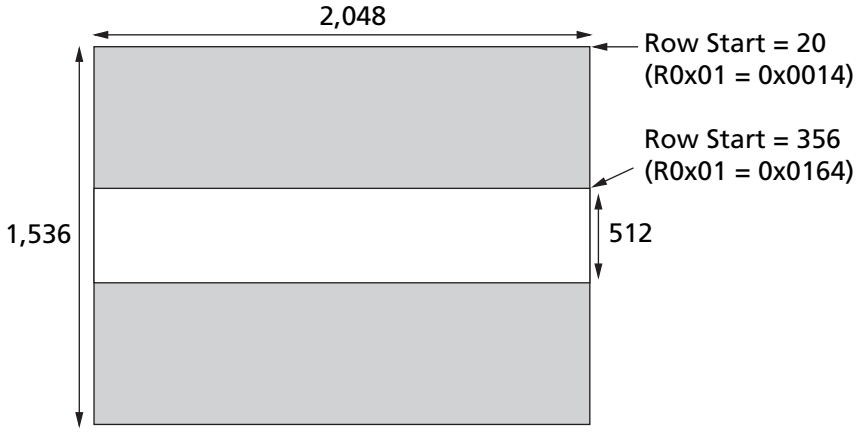


	Window Size	R0x01	R0x02	R0x03	R0x04
Window A	2,048 x 1,536	0x0014	0x0020	0x05FF	0x07FF
Window B	128 x 128	0x00B4	0x04B0	0x007F	0x007F
Window C	512 x 512	0x0164	0x0238	0x01FF	0x01FF
Window D	400 x 96	0x0390	0x0050	0x018F	0x005F

Table 9: Auto Focus Modes

Resolu-tion	Frame Rate	Column_ Size (R0x04)	Row_ Size (R0x03)	Horizontal_ Blank (R0x05)	Vertical_ Blank (R0x06)	Row_ Bin (R0x22)	Row_ Skip (R0x22)	Column_ Bin (R0x23)	Column_ Skip (R0x23)
2,048 x 512	30 fps	2,047	1,535	22	1	2	2	0	0
2,048 x 256	60 fps	2,047	1,535	22	0	2	5	0	0
2,048 x 128	120 fps	2,047	1,023	34	14	1	7	0	0

Figure 10: Windowing



The user can change R0x05 and R0x06 to obtain the desired frame rate. Also, the user may want to perform row skip modes to obtain larger field of view if high-frequency vertical resolution is not critical.

Pixel Integration Time Control

R0x09 and R0x0C

The integration time of the pixel is the amount of time the pixels are set to collect charge generated from light. The user can change the integration time of the sensor by programming R0x09. The value of R0x09 sets the number of row time for integration. The sensor also supports sub-row integration time for fine control of pixel integration time.

The formula for calculating the pixel integration time is (reference Table 4 on page 12 for P1 description):

$^{t}INT = (65536 \times R0x08 + R0x09) \times {}^{t}ROW - R0x0C - P1 + 132$

Typically, the value of R0x09 is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time. However, if R0x09 is increased beyond the total number of rows per frame, then additional blanking rows are added as needed.

While the user can adjust the integration time to the desired value according to the aforementioned formula, not all integration times may be desired under certain lighting conditions. If the light source has a flicker component, then the integration time needs to be set properly to avoid banding in the image.

Under 60Hz flicker, the integration time must be a multiple of 1/120 of a second to avoid flicker. Under 50Hz flicker, the integration time must be a multiple of 1/100 of a second to avoid flicker.

Snapshot Mode and Flash Control

R0x1E, STROBE pin and TRIGGER pin

Setting up for Snapshot Mode

Snapshot mode must be enabled before use by setting bit 8 = “1” of R0x1E. There are two important signals used for snapshot mode: TRIGGER and STROBE. The TRIGGER signal initiates the start of a single frame capture and STROBE is an output pulse that may be used to turn on a flash and/or activate a mechanical shutter.

Triggering A Snapshot

The TRIGGER signal required for starting a frame capture may be generated in the following two ways:

1. External TRIGGER Pulse
   Pin 8 is a digital input that may be used to supply an external trigger signal input. The snapshot operation begins after the TRIGGER pulse transitions from a HIGH to LOW state.
2. TRIGGER from Register Setting
   A second method for triggering a snapshot is by setting bit 0 = 1 of R0x0B (Restart). This register automatically returns bit 0 to “0” after the TRIGGER is initiated. This bit does not need to be reset by the user after use.

Strobe Pulse Output

The STROBE pulse must be enabled before use by setting R0x1E [bit 9] = 1. The STROBE signal has two options for pulse length and may be selected using R0x1E [bit 10] as shown in Table 10.

Table 10: STROBE Pulse Output

R0x1E, Bit 10	STROBE Pulse Width
0	1 row time (default)
1	((65536 x R0x08 + R0x09 – R) -16) x ^{t}ROW - V

After the TRIGGER pulse has signaled a snapshot operation, each row of the imager array is reset in sequence to clear out any accumulated signal. Once each row of the imager is reset, the STROBE pulse is output from the imager with a length dependent upon the characteristics described above. After the STROBE pulse goes low, the imager waits 16 additional rows and then each row from the pixel array is read out. No STROBE is generated unless the shutter width is greater than the output image height plus vertical blanking.

Global Shutter Release Snapshot Mode

R0x1E and R0x21

In addition to the standard snapshot mode, the MT9T031 has a global shutter release mode which may be combined with a mechanical shutter to achieve simultaneous exposure of all rows in the image.

Two global shutter modes are available: programmed exposure and bulb mode. In programmed exposure mode, the exposure time is dictated by {R0x08, R0x09} (Shutter Width). In bulb mode, the TRIGGER and GSHT_CTL pins are used to achieve an arbitrary exposure time.

Programmed Exposure Mode

To use programmed exposure mode:

1. Set up snapshot mode as normal (including any STROBE preferences).
2. Set R0x21 (Read Mode 3) to 0x0003.
3. Assert (transition LOW to HIGH) the GSHT_CTL pin to reset the array. This pin must remain HIGH for 18820 PIXCLKs.
4. Negate (transition HIGH to LOW) the GSHT_CTL pin to begin the exposure. The exposure starts 1000 PIXCLKs after the falling edge of GSHT_CTL.

Note: Unlike normal snapshot mode, R0x0B (Restart) may not be used to initiate the exposure in global shutter modes.

5. Row readout begins automatically. The mechanical shutter should be closed before row read out begins. The trailing edge of STROBE (if enabled) occurs ((65536 x R0x08 + R0x09) x ^{t}ROW + 2000) PIXCLKs after the falling edge of GSHT_CTL. Readout of the active window starts the lesser of 16 x ^{t}ROW or (R0x06 + 1) x ^{t}ROW later.

Bulb Mode

To use bulb mode:

1. Set up snapshot mode as normal (including any STROBE preferences).
2. Set R0x21 (Read Mode 3) to 0x0001.
3. Assert (transition LOW to HIGH) the GSHT_CTL pin.
4. Assert (transition LOW to HIGH) the TRIGGER pin to reset the array. This pin must remain HIGH for at least 18,820 PIXCLKs.
5. Negate (transition HIGH to LOW) the GSHT_CTL pin to begin the exposure. The exposure starts 1,000 PIXCLKs after the falling edge of GSHT_CTL.

Note: Unlike normal snapshot mode, R0x0B (Restart) may not be used to initiate the exposure in global shutter modes.

6. Negate (transition HIGH to LOW) the TRIGGER pin to begin row read out. The mechanical shutter should be closed before row read out begins. The trailing edge of STROBE (if enabled) occurs ((65536 x R0x08 + R0x09) x ^{t}ROW) PIXCLKs after the falling edge of TRIGGER. Read out of the active window starts the lesser of 16 x ^{t}ROW or (R0x06 + 1) x ^{t}ROW later. In this mode, the shutter width (R0x08, R0x09) would normally be set to a low number, allowing row readout to start immediately after the trailing edge of TRIGGER.

Skip and Bin Modes

Row and column skip modes use subsampling to reduce the output resolution without reducing field-of-view. The MT9T031 also has row and column binning modes, which can reduce the impact of aliasing introduced by the use of skip modes. This is achieved by the averaging of two or three adjacent rows and columns (adjacent same-color pixels). Both 2X and 3X binning modes are supported. Rows and columns can be binned independently.

Table 11: Bin and Skip Mode Resolution

Resolution	Frame Rate	Column_ Size (R0x04)	Row_ Size (R0x03)	Horizontal_ Blank (R0x05)	Vertical_ Blank (R0x06)	Row_ Bin (R0x22)	Row_ Skip (R0x22)	Column_ Bin (R0x23)	Column_ Skip (R0x23)
1,024 x 768 XGA	34 fps	2,047	1,535	22	40	1	1	1	1
800 x 600 SVGA	50 fps	1,599	1,199	22	30	1	1	1	1
640 x 480 VGA	48 fps	1,919	1,439	21	31	2	2	2	2

Note: Column start address value must be a multiple of R0x23 [5–4] + 1.

To use binning mode, set R0x22[5–4] (row bin) or R0x23[5–4] (column bin) to the desired reduction minus 1, as would be done for skip mode. Additionally, R0x22[2–0] (column skip) must be set no less than R0x22[5–4], and R0x23[2–0] (row skip) must be set no less than R0x23[5–4]. Row and column skip modes may be set higher than the corresponding binning modes to achieve greater reductions, but binning must be done. The different skip modes supported are between 2X and 8X in both column and row directions. The different binning modes supported are 2X and 3X. See Table 12 for register bits controlling the different bin and skip modes.

Table 12: Skip and Bin Modes

Register Bit	Skip/Bin Modes	Readouts
R0x23 Bit[2–0]	 No column skip Column skip 2X Column skip 3X Column skip 4X Column skip 8X	 col0, col1, col2, col3, col4, col5, etc. col0, col1, col4, col5, col8, col9, etc. col0, col1, col16, col7, col12, col13 etc. col0, col1, col8, col9, col16, col17, etc. col0, col1, col16, col17, col32, col33, etc.
Bit[5–4]	Column Bin 2X Column Bin 3X	Binning of 2 adjacent same-color pixels in a 4x4 window Binning of 3 pixel of each color plane in a 6x6 window
R0x22 Bit[2–0]	 No row skip Row skip 2X Row skip 3X Row skip 4X Row skip 8X	 row0, row1, row2, row3, row4, row5, etc. row0, row1, row4, row5, row8, row9, etc. row0, row1, row6, row7, row12, row13, etc. row0, row1, row8, row9, row16, row17, etc. row0, row1, row16, row17, row32, row33, etc.
Bit[5–4]	Row bin 2X Row bin 3x	Binning of 2 pixel of each color plane in a 4x4 window Binning of 3 pixel of each color plane in a 6x6 window

Note: Column and row skip modes 1x through 8x are available on the MT9T031. Also, the read outs shown assume column start and row start addresses are both “0”.

Figure 11: Column Skip 2X; Row Skip 2X Enabled

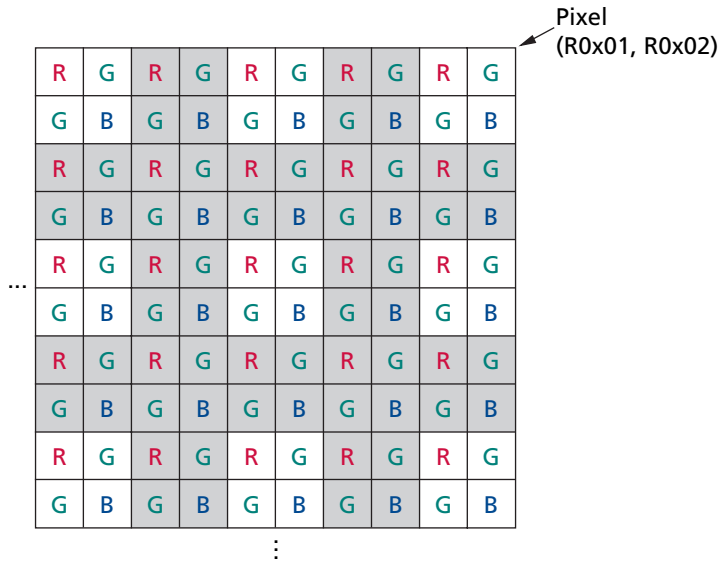


Figure 12: Column Skip 3X; Row Skip 3X Enabled

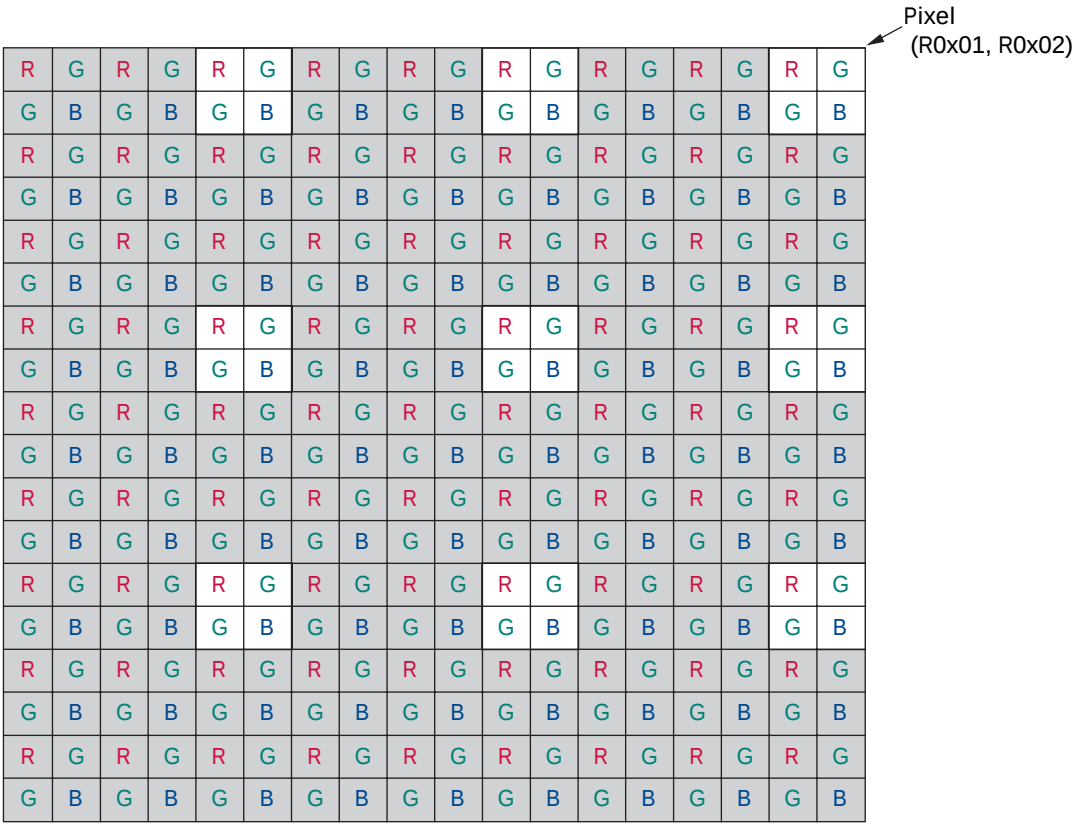


Figure 13: Column Skip 4X; Row Skip 4X Enabled

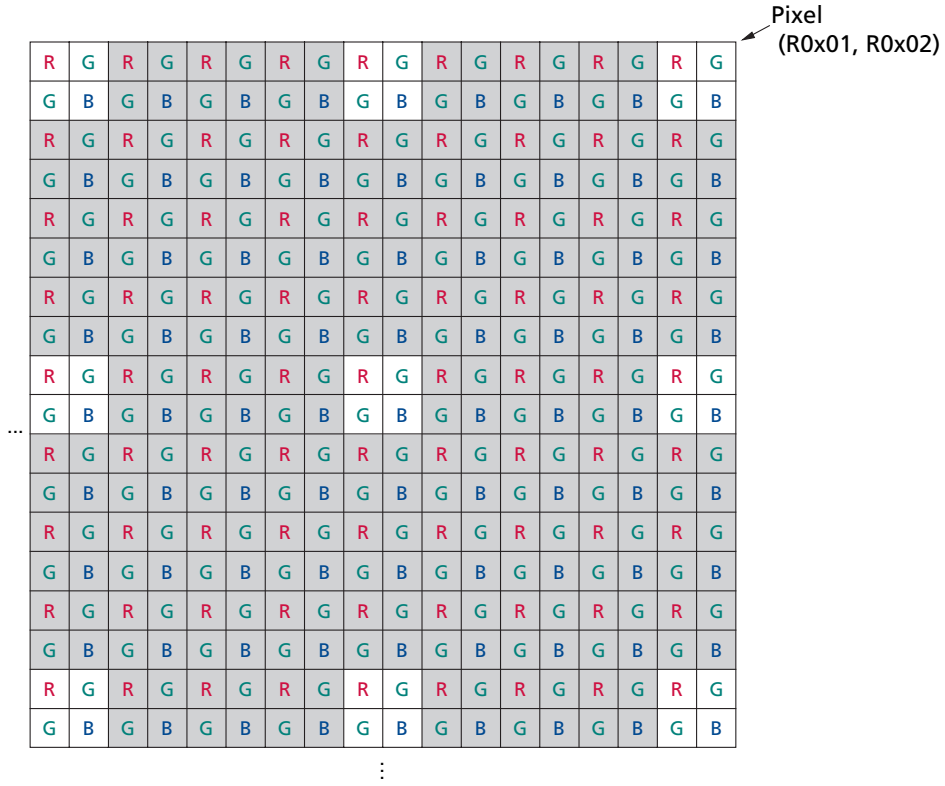


Figure 14: Column Skip 8X; Row Skip 8X Enabled

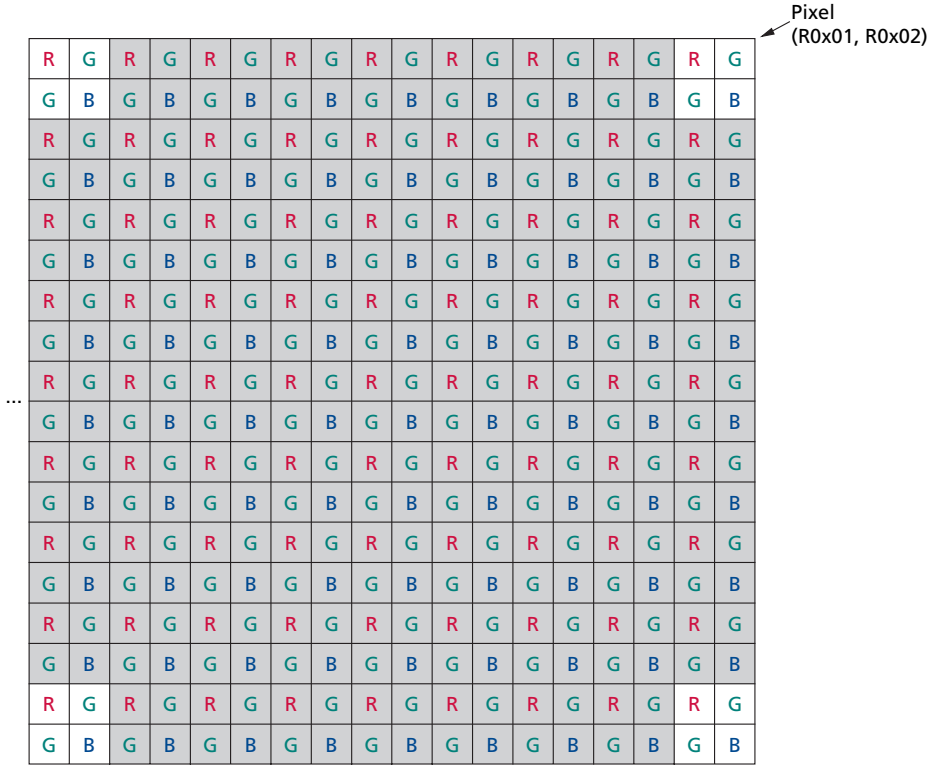
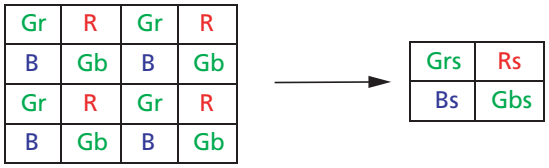
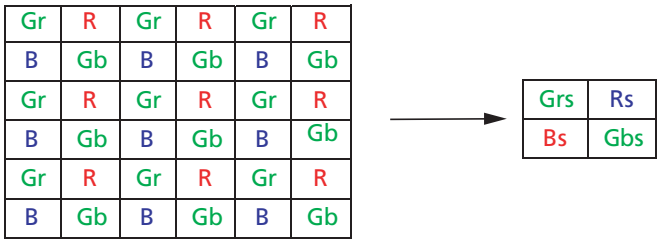


Figure 15: Bin 2-to-1: 2,048H x 1,536V (QXGA) to 1,024H x 768V (XGA)



Note: Grs = binning of 4 Gr[s] in a 4 x 4 window; Gbs = binning of 4 Gb[s] in a 4 x 4 window.
Rs = binning of 4 R[s] in a 4 x 4 window; B[s] = binning of 4 B[s] in a 4 x 4 window.

Figure 16: Bin 3-to-1: 2,048H x 1,536V (QXGA) to 640H x 480V (VGA)



Note: Grs = binning of 9 Gr[s] in a 6 x 6 window; Gbs = binning of 9 Gb[s] in a 6 x 6 window.
Rs = binning of 9 R[s] in a 6 x 6 window; Bs = binning of B[s] in a 6 x 6 window.

Smaller Format Resolution

R0x01, R0x02, R0x03, R0x04, R0x05, R0x06, R0x22, and R0x23

With the aforementioned flexible windowing capability of the sensor, the user is able to read out different resolution formats from default of QXGA to UXGA, SXGA, XGA, SVGA, VGA, CIF, QVGA, QCIF, etc. Below are some examples of programmable register settings to obtain the estimated frame rates for the desired formats.

The user can change the values of R0x05 and R0x06 to obtain different frame rates. The field of view of the image is reduced since the programmed settings effectively reduce the read out window to the specified settings without skipping any rows or columns.

If the user only changes the register settings mentioned above without changing the row and column start address, the read out window would start from that coordinate. To read out the center of the image or any portion that is desired, the user would need to program R0x01 and R0x02, thus performing electronic panning.

To maintain the same field of view while reducing the read out resolution, the user would need to perform row and column skip. For example, if the desired read out resolution needs to be XGA (1,024H x 7,68V) instead of QXGA (2,048H x 1,536V). To maintain the same field of view, the user can select column skip 2X and row skip 2X modes. This effectively reduces the horizontal and vertical resolution by 2X for a factor of 4X reduction in overall number of pixels that are read out.

To perform this read out mode, the user would need to set the following:

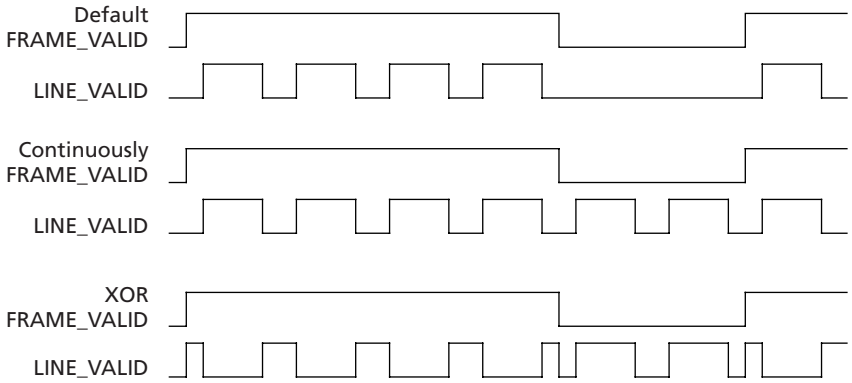
R0x03 = 0x05FF	1,536V rows
R0x04 = 0x07FF	2,048H columns
R0x23 Bit[2:0]=1	Column skip 2X—> 1,024H columns read out
R0x22 Bit[2:0] = 1	Row skip 2X —> 768 rows read out

If the user sets R0x03 = 0x02FF (768V rows), R0x04 = 0x03FF (1,024H columns), and then enable column skip 2X and row skip 2X, the effective readout resolution is 512H x 384V.

Line_Valid Formats

R0x20 is used to control many aspects of the readout of the sensor. By setting Bit 9 and 10 of R0x20 the LINE_VALID signal can get three different output formats. The formats are shown in Figure 17 when reading out four rows and two vertical blanking rows. In the last format the LINE_VALID signal is the XOR between the continuously LINE_VALID signal and the FRAME_VALID signal.

Figure 17: Different LINE_VALID Formats



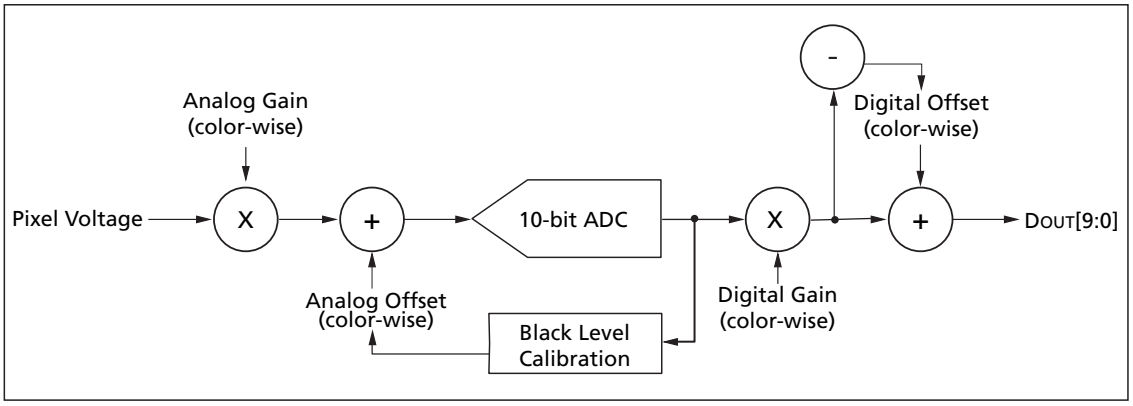
Signal Path

The MT9T031 sensor analog signal path consists of the pixel array, the column sample and hold (S/H) circuitry, the programmable gain stage, the analog offset correction and the analog-to-digital converter (ADC).

The reset and signal voltages from the pixel are sampled onto the column sample and hold circuitry on a row-wise basis. After signal sampling is complete, the differential signal (reset – signal) is transferred to the programmable gain stage.

After the gain stage, the differential signal goes through the analog offset correction circuitry. The user can decide if a positive or negative offset or no offset needs to be added to the differential signal. The signal is then sampled onto the sample and hold circuitry of the ADC before being digitized.

Figure 18: Signal Path



Gain Settings

R0x2B, R0x2C, R0x2D, R0x2E, and R0x35

The analog programmable gain stage consists of two stages of gain circuitry that operate in a pipelined manner. The first stage of gain has programmable gain of 1 or 2 while the second stage of gain has programmable gain of 1 to 4 with steps of 0.125 for a maximum analog gain of 8. The gain settings can be independently adjusted for the colors of Green1, Blue, Red, and Green2 and are programmed through R0x2B, R0x2C, R0x2D, and R0x2E, respectively. The gain may also be adjusted globally through R0x35. The first stage of gain is set by Bit(6), while the second stage gain is set by Bit(5–0). The gain is individually controllable for each color in the Bayer pattern as follows:

Analog Gain < = 8:

Gain = (Bit[6] + 1) x (Bit[5:0] x 0.125)

Digital Gain = 1 + Bit[14:8]/8

Total Gain = Analog Gain x Digital Gain

Since Bit[6] of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, despite the same overall gain, as shown in Table 13.

Table 13: Gain Increment Settings

Nominal Gain	Increments	Recommended Settings
1 to 4.000	0.125	0x0008 to 0x0020
4.25 to 8.00	0.25	0x0051 to 0x0060
9.0 to 128.0	1.0	0x0160 to 0x7860

Black Level Calibration

R0x5D, and R0x5F

The digitized black level of the MT9T031 sensor potentially varies with temperature or gain setting changes. The MT9T031 sensor allows the user the flexibility of automatic black level calibration or manual black level control.

Manual Black Level Calibration

R0x60, R0x61, R0x62, R0x63, and R0x64

The programmable analog offset stage corrects for analog offset that might be present in the analog signal. The user would need to program R0x62 appropriately to enable the analog offset correction. The analog offset settings can be independently adjusted for the colors of Green1, Green2, Red and Blue and are programmed through R0x60, R0x61, R0x63 and R0x64 respectively. Bit[8] of R0x60, R0x61, R0x63 and R0x64 (these registers have two's complement representation) determines the sign of the analog offset. Bit[8] = 1 makes the analog correction negative instead of positive.

The lower 8 bits (Bit[7:0]) determine the absolute value of the analog offset to be corrected and Bit[8] determines the sign of the correction. When Bit[8] is "1", the sign of the correction is negative and vice versa. The analog value of the correction relative to the analog gain stage can be determined from the following formula:

Analog offset = Bit[8:0] x 1 LSB

The 1 LSB value in the formula is an estimate amount. It deviates from 1 LSB with process variation.

Black Level

R0x49

Digital offset is applied such that the average black level of a frame in a resulting image equals the value of this register. This adjustment happens after black level calibration.

Reset

This register is used to reset the sensor registers to their default, power-up state. To reset the MT9T031, first write a "1" into bit 0 of this register to put the MT9T031 in reset mode, then write a "0" into bit 0 to resume operation.

Another way to reset the sensor is through the RESET# (pin 10) – by pulling the RESET# signal to 0V.

The reset operation is an asynchronous reset and the sensor remains in reset as long as RESET# signal = 0V. In both methods of reset, the sensor register settings returns to their default states.

Standby Control and Chip Enable

There are two steps required to put the sensor in standby mode:

1. Through the two-wire serial interface program R0x07 Bit[1] = 0. This stops the sensor readout and powers down analog circuitry of the sensor. The sensor stays in standby mode until the user reprograms R0x07 Bit[1] = 1.
2. Set STANDBY (pin 7) to HIGH.

Serial Bus Description

Registers are written to and read from the MT9T031 through the two-wire serial interface bus. The MT9T031 is a serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out of the MT9T031 through the serial data (SDATA) line. The SDATA line is pulled up to 3.3V off-chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial defines several different transmission codes, as follows:

- a start bit
- the slave device 8-bit address
- a(n) (no) acknowledge bit
- an 8-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request is a read or a write, where a “0” indicates a write and a “1” indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data eight bits at a time, with the slave sending an acknowledge bit after each eight bits. The MT9T031 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The eight-bit address of a two-wire serial interface device consists of seven bits of address and 1 bit of direction. A “0” (0xBA) in the LSB (least significant bit) of the address indicates write mode, and a “1” (0xBB) indicates read mode.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

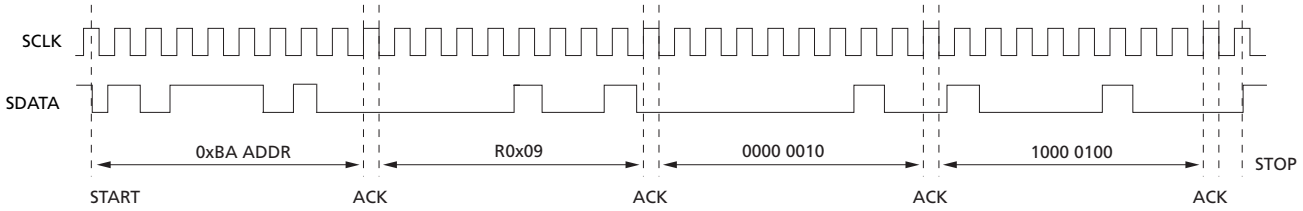
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample Write and Read Sequences

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 19. A start bit given by the master, followed by the write address, starts the sequence. The image sensor then gives an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each eight-bit transfer, the image sensor gives an acknowledge bit. All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

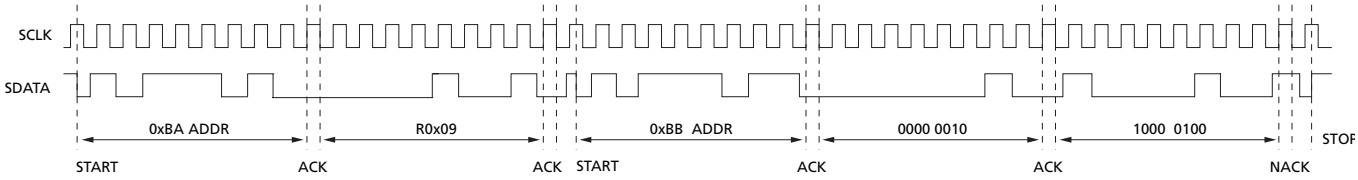
Figure 19: Timing Diagram Showing a Write to R0x09 with the Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure 20. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Figure 20: Timing Diagram Showing a Read from R0x09; Returned Value 0x0284

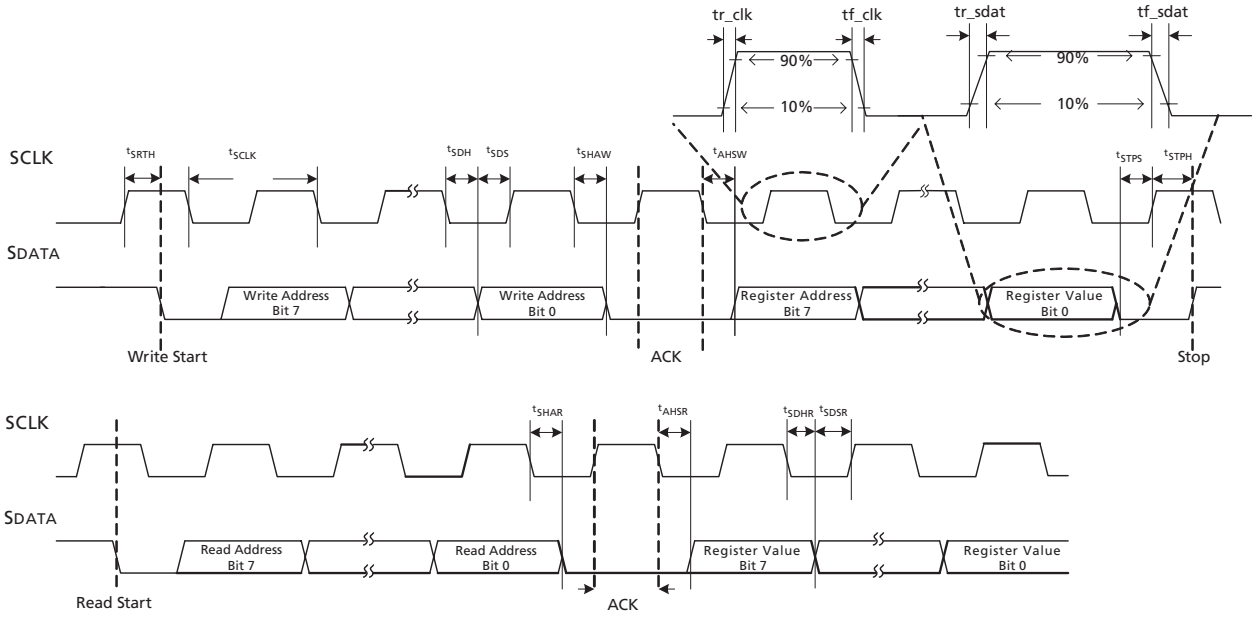


Electrical Specifications

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 21 and Table 14 on page 41.

Figure 21: Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after the WRITE command and register address are issued.

Table 14: Two-Wire Serial Bus Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
^{f}SCLK	Serial interface input clock frequency	–	–	–	1.2	MHz
^{t}SCLK	Serial Input clock period	–	–	–	83.3	µsec
	SCLK Duty Cycle	–	20	50	79	%
tr_sclk	SCLK rise time		–	173.4	–	ns
tf_sclk	SCLK fall time		–	64.2	–	ns
tr_sdat	SDATA rise time		–	172.6	–	ns
tf_sdat	SDATA fall time		–	63	–	ns
^{t}SRTH	Start hold time	WRITE/READ	100	145.8	200	ns
^{t}SDH	SDATA hold time	WRITE	0	0	0	ns
^{t}SDS	SDATA setup time	WRITE	0	0	0	ns
^{t}SHAW	SDATA hold to ACK	WRITE	580	623	680	ns
^{t}AHSW	ACK hold to SDATA	WRITE	580	623	680	ns
^{t}STPS	Stop setup time	WRITE/READ	0	0	0	ns
^{t}STPH	Stop hold time	WRITE/READ	0	0	0	ns
^{t}SHAR	SDATA hold to ACK	READ	580	623	680	ns
^{t}AHSR	ACK hold to SDATA	READ	580	623	680	ns
^{t}SDHR	SDATA hold	READ	0	0	0	ns
^{t}SDSR	SDATA setup	READ	0	0	0	ns

I/O Timing

By default, the MT9T031 launches pixel data, FRAME_VALID and LINE_VALID with the rising edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FRAME_VALID and LINE_VALID using the falling edge of PIXCLK. See Figure 22 and Table 15 for I/O Timing (AC) characteristics.

Figure 22: I/O Timing Diagram

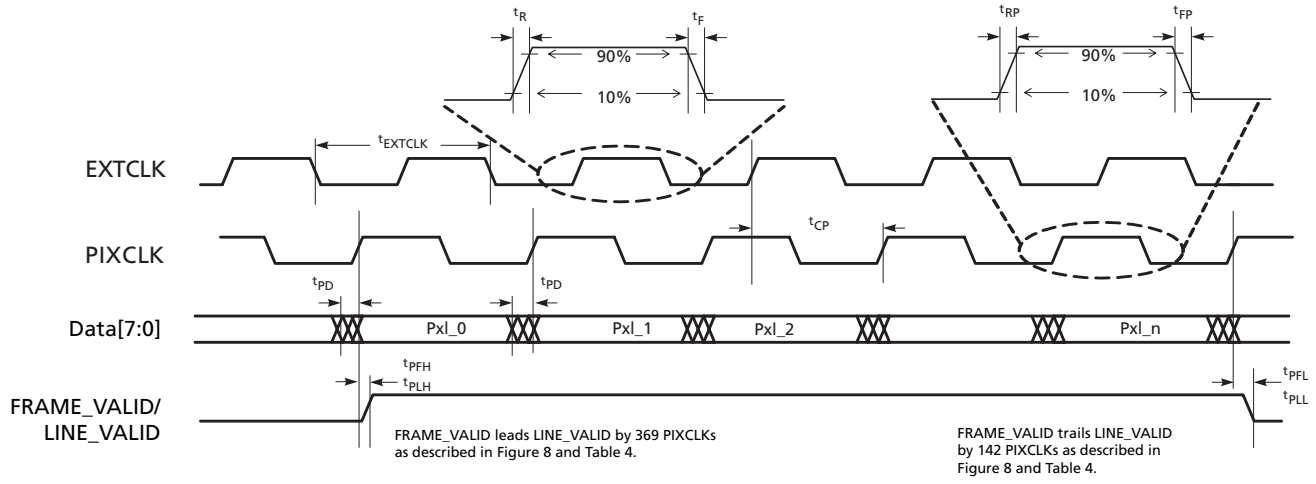


Table 15: I/O Timing Characteristics

Symbol	Definition	Conditions	Min	Typ	Max	Units
^{f}EXTCLK1	Input clock frequency		1	–	48	MHz
^{t}EXTCLK1	Input clock period		1000	–	20.8	ns
^{t}R	Input clock rising edge slew rate		–	4	–	V/ns
^{t}F	Input clock falling edge slew rate		–	4	–	V/ns
^{t}RP	Pixclk rising edge slew rate		–	4	–	V/ns
^{t}FP	Pixclk falling edge slew rate		–	4	–	V/ns
	Clock duty cycle		40	50	60	%
^{t}JITTER	Input clock jitter 48 MHz		–	306	–	ps
^{t}CP	EXTCLK to PIXCLK propagation delay	Nominal voltages	–	5	–	ns
^{f}PIXCLK	PIXCLK frequency	Default	1	–	48	MHz
^{t}PD	PIXCLK to data valid	Default	0.6	4.02	8.8	ns
^{t}PFH	PIXCLK to FV HIGH	Default	1.0	3.98	7.6	ns
^{t}PLH	PIXCLK to LV HIGH	Default	1.1	4.08	6.8	ns
^{t}PFL	PIXCLK to FV LOW	Default	1.1	4.08	6.8	ns
^{t}PLL	PIXCLK to LV LOW	Default	2.1	4.56	8.6	ns
C_{LOAD}	Output load capacitance		–	30	–	pF

Table 16: DC Electrical Characteristics

^{f}EXTCLK = 48 MHz, V_{DD} = 3.3V, V_{AA} = 3.3V, VAAPIX = 3.3V, T_A = 25°C

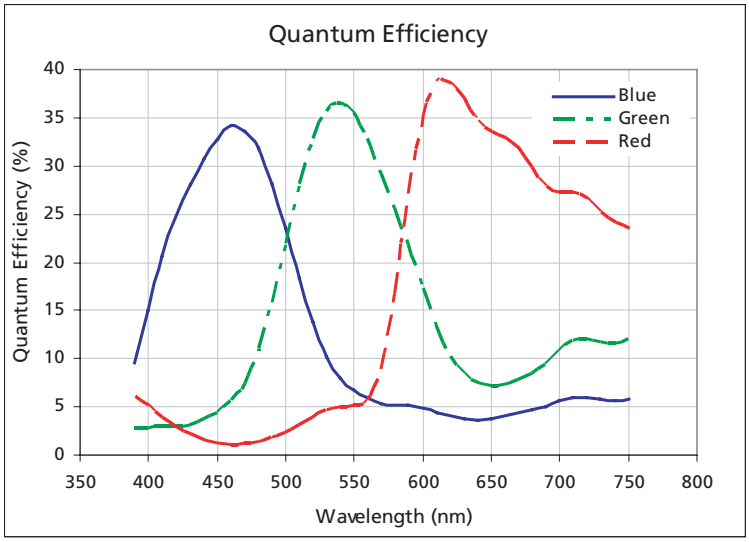
Symbol	Definition	Condition	Min	Typ	Max	Units
V_{DD}	Core digital voltage		3	3.3	3.6	V
V_{AA}	Analog voltage		3	3.3	3.6	V
VAAPIX	Pixel supply voltage		3	3.3	3.6	V
V_{IH}	Input high voltage		1.70			V
V_{IL}	Input low voltage				1.45	V
I_{IN}	Input leakage current	No Pull-up Resistor; V_{IN} = V_{DD} or DGND	–5		5	µA
V_{OH}	Output high voltage	At specified I_{OH}	3.3			V
V_{OL}	Output low voltage	At specified I_{OL}	0		0.3	V
I_{OH}	Output high current	At specified V_{OH}			11.5	mA
I_{OL}	Output low current	At specified V_{OL}			12.5	mA
I_{OZ}	Tri-state output leakage current				5	µA
I_{DD}	Digital operating current	0 lux, 48 MHz	23.6	24	27.8	mA
I_{AA}	Analog operating current	0 lux, 48 MHz	44.6	46.0	54.9	mA
I_{AAPIX}	Pixel supply current	0 lux, 48 MHz	3.7	3.9	4.9	mA
I_{STDBYD}	Digital standby current	Input clock disabled, 0 lux		0.2	2.0	µA
I_{STDBYA}	Analog standby current	Input clock disabled, 0 lux		0.2	2.0	µA
$I_{STDBYDA}$	Pixel standby current	Input clock disabled, 0 lux		0.1	1.0	µA

Table 17: Absolute Maximum Ratings

Symbol	Definition	Conditions	Min	Max	Units
V_{DD}_MAX	Core digital voltage		–0.3	3.6	V
V_{AA}_MAX	Analog voltage		–0.3	3.6	V
V_{AAPIX}_MAX	Pixel supply voltage		–0.3	3.6	V
V_{IN}_MAX	Input voltage		–	1.9	V
I_{DD}_MAX	Digital operating current		–	29.5	mA
I_{AA}_MAX	Analog operating current		–	56.3	mA
I_{AAPIX}_MAX	Pixel supply current		–	6.4	mA
T_{OP}[2]	Operating temperature	Measure at junction	0	60	°C
T_{ST}[1]	Storage temperature		–40	125	°C

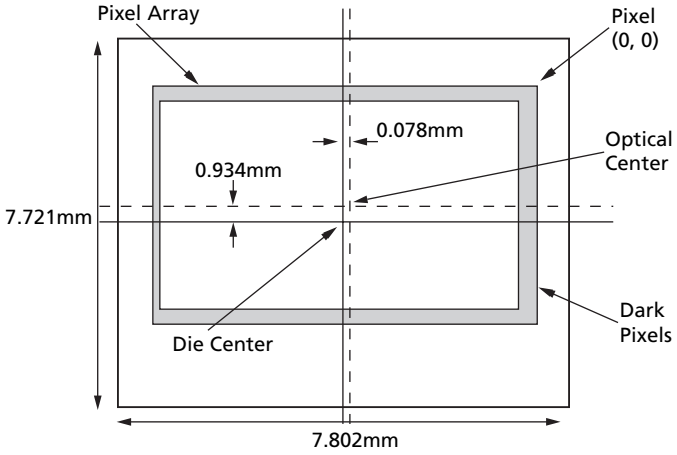
Note:
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. In order to keep dark current and shot noise artifacts from impacting image quality, care should be taken to keep T_{OP} at a minimum.

Figure 23: Quantum Efficiency



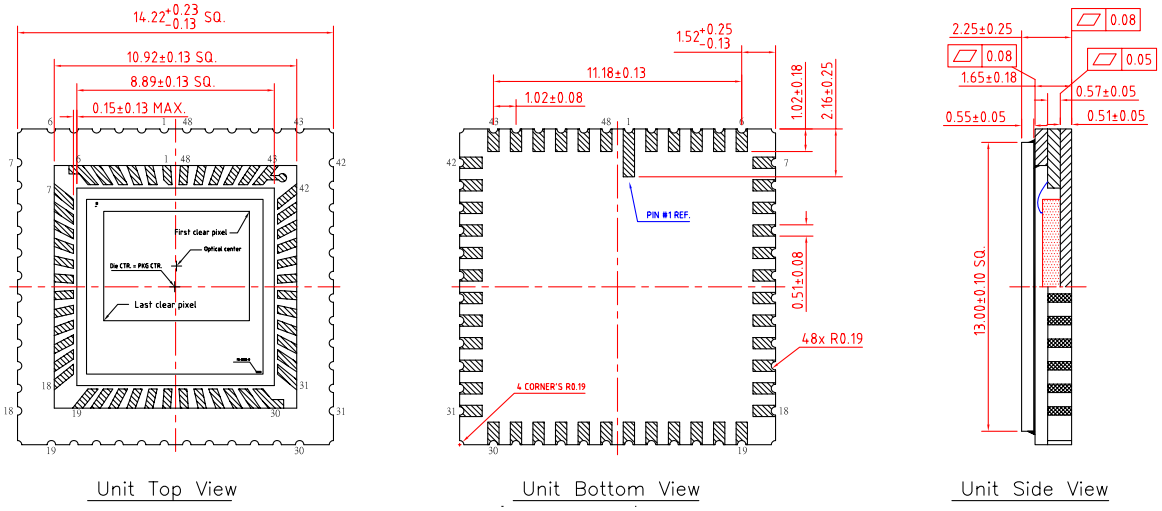
Note: Diagram not to scale.

Figure 24: Image Center Offset



Note: Diagram not to scale.

Figure 25: 48-Pin CLCC



NOTE:

1. ALL EXPOSED METALLIZED AREA SHALL BE GOLD PLATED 60 MICRO INCHES MIN. THK. OVER NICKEL PLATED UNLESS OTHERWISE SPECIFIED IN PURCHASE ORDEI
2. SEAL AREA AND DIE ATTACH AREA SHALL BE WITHOUT METALLIZATION.
3. DIE PLACEMRNT ACCARUCY = ±0.125mm
4. WAFER THICKNESS = 0.675mm (26.57 mil) .
5. EPOXY THICKNESS FOR DIE ATTACHMENT IS 0.025~0.050mm
6. GLASS TRANSMITTANCE >=90%.
7. GLASS TILT = 0.10mm MAX.
8. DIE LOCATION : DIE CENTER AIMS AT PACKAGE CENTER.

Note: All dimensions in millimeters.

Revision History

Rev. E 5/3/11

- Updated trademarks
- Applied updated template

Rev. D 6/10

- Updated to non-confidential

Rev. C 5/4/10

- Added Figure 24: “Image Center Offset,” on page 44

Rev. B 9/09

- Updated to Aptina template
- Changed 48-pin PLCC to 48-pin CLCC in Table 1, “Key Performance Parameters,” on page 1, in Figure 3: “48-Pin CLCC,” on page 8, and in Figure 25: “48-Pin CLCC,” on page 45
- Updated Figure 25: “48-Pin CLCC,” on page 45

Rev. A, Production. 07/06

- Initial release

10 Eunos Road 8 13-40, Singapore Post Center, Singapore 408600 prodmktg@aptina.com www.aptina.com

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Image Sensors ***category:***

Click to view products by ON Semiconductor ***manufacturer:***

Other Similar products are found below :

KAF-16803-ABA-DD-BA KAF-4320-AAA-JP-B1 KAF-16200-ABA-CD-B2 KAF-50100-AAA-JD-BA KAI-0340-FBA-CB-AA-SINGLE KAI-11002-ABA-CD-B1 KAI-2020-ABA-CD-BA KAI-2093-ABA-CB-B2 KAI-2020-ABA-CP-BA KAI-01150-FBA-FD-BA KAF-8300-AXC-CD-AA KAI-11002-ABA-CD-B2 KAF-3200-ABA-CD-B2 AR0331SRSC00SUCA0-DPBR EKL3104 MT9V138C12STC-DP1 KAI-08051-AXA-JP-BA KLI-8023-RAA-ED-AA KAF-0402-ABA-CP-B2 KLI-8023-AAA-ED-AA KAF-16200-FXA-CD-B2 KAI-04050-AAA-JP-BA NOM02A4-AG01G NOM02A4-AR03G KAF-1603-AAA-CP-B2 KAF-1001-AAA-CP-B1 NOIV1SE2000A-QDC KAI-1003-AAA-CR-B2 KAI-0340-FBA-CB-AA-DUAL KAF-0402-ABA-CD-B1 KAI-01050-FBA-JD-BA AR0237IRSH12SHRA0-DR NOIV1SE5000A-QDC OV02659-A47A AR0132AT6M00XPEA0-DRBR DR2X2K7_INVAR_RGB_V6 DR2X4K7_INVAR_RGB_V6 NOIP1SE1300A-QDI AR0132AT6C00XPEA0-DRBR1 AR0140AT3C00XUEA0-DPBR2 AR0144CSSC00SUKA0-CPBR1 AR0144CSSC00SUKA0-CPBR2 AR0230CSSC00SUEA0-DPBR2 AR0238CSSC12SHRA0-DP2 AR0330CM1C00SHAA0-DP2 AR0330CM1C00SHAA0DR AR0330CM1C00SHAA0-DP1 AR0330CS1C12SPKA0-CP2 AR0521SR2M09SURA0-DP1 AR0522SRSC09SURA0-DP1