

NB2305A

3.3 V Zero Delay Clock Buffer

The NB2305A is a versatile, 3.3 V zero delay buffer designed to distribute high-speed clocks. It accepts one reference input and drives out five low-skew clocks. It is available in a 8 pin package.

The -1H version of the NB2305A operates at up to 133 MHz, and has higher drive than the -1 devices. All parts have on-chip PLL's that lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

Multiple NB2305A devices can accept the same input clock and distribute it. In this case the skew between the outputs of the two devices is guaranteed to be less than 700 ps.

All outputs have less than 200 ps of cycle-to-cycle jitter. The input and output propagation delay is guaranteed to be less than 350 ps, and the output to output skew is guaranteed to be less than 250 ps.

The NB2305A is available in two different configurations, as shown in the ordering information table. The NB2305AI is the base part. The NB2305AI1H is the high drive version of the -1 and its rise and fall times are much faster than -1 part.

Features

- 15 MHz to 133 MHz Operating Range, Compatible with CPU and PCI Bus Frequencies
- Zero Input – Output Propagation Delay
- Multiple Low-Skew Outputs
- Output-Output Skew Less than 250 ps
- Device-Device Skew Less than 700 ps
- One Input Drives 5 Outputs
- Less than 200 ps Cycle-to-Cycle Jitter is Compatible with Pentium® Based Systems
- Accepts Spread Spectrum Clock at the Input
- Available in 8 Pin, 150 mil SOIC Package and 8 Pin TSSOP 4.4 mm
- 3.3 V Operation, Advanced 0.35 μ CMOS Technology
- Guaranteed Across Commercial and Industrial Temperature Ranges
- These are Pb-Free Devices



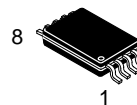
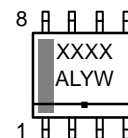
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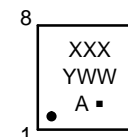
MARKING DIAGRAMS*



SOIC-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948S



XXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

NB2305A

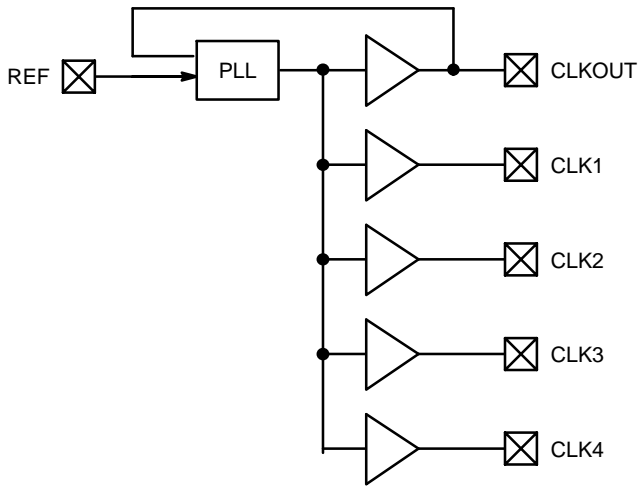


Figure 1. Block Diagram

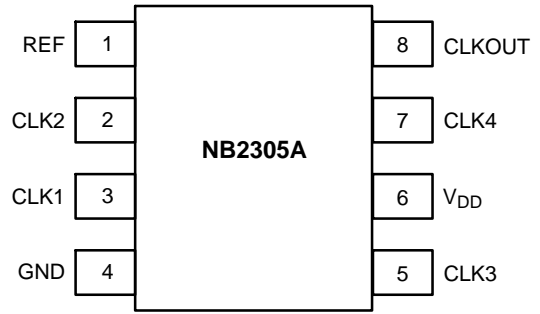


Figure 2. Pin Configuration

Table 1. PIN DESCRIPTION

| Pin # | Pin Name | Description |
|-------|-----------------|---|
| 1 | REF (Note1) | Input reference frequency, 5 V tolerant input. |
| 2 | CLK2 (Note 2) | Buffered clock output. |
| 3 | CLK1 (Note 2) | Buffered clock output. |
| 4 | GND | Ground. |
| 5 | CLK3 (Note 2) | Buffered clock output. |
| 6 | V _{DD} | 3.3 V supply. |
| 7 | CLK4 (Note 2) | Buffered clock output. |
| 8 | CLKOUT (Note 2) | Buffered clock output, internal feedback on this pin. |

1. Weak pulldown.
2. Weak pulldown on all outputs.

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Table 2. MAXIMUM RATINGS

| Parameter | Min | Max | Unit |
|---|------|----------------|------|
| Supply Voltage to Ground Potential | -0.5 | +7.0 | V |
| DC Input Voltage (Except REF) | -0.5 | $V_{DD} + 0.5$ | V |
| DC Input Voltage (REF) | -0.5 | 7.0 | V |
| Storage Temperature | -65 | +150 | °C |
| Maximum Soldering Temperature (10 sec) | | 260 | °C |
| Junction Temperature | | 150 | °C |
| Static Discharge Voltage (per MIL-STD-883, Method 3015) | | >2000 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. RECOMMENDED OPERATING CONDITIONS FOR INDUSTRIAL TEMPERATURE DEVICES

| Parameter | Description | Min | Max | Unit |
|-----------|---|--------------------------|-----------------|------|
| V_{DD} | Supply Voltage | 3.0 | 3.6 | V |
| T_A | Operating Temperature (Ambient Temperature) | Industrial Commercial | -40 85 70 | °C |
| C_L | Load Capacitance, below 100 MHz | | 30 | pF |
| C_L | Load Capacitance, from 100 MHz to 133 MHz | | 10 | pF |
| C_{IN} | Input Capacitance | | 7 | pF |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS $V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

| Parameter | Description | Test Conditions | Min | Max | Unit |
|-----------|----------------------------------|---|-----|----------------|---------------|
| V_{IL} | Input LOW Voltage (Note 3) | | | 0.8 | V |
| V_{IH} | Input HIGH Voltage (Note 3) | | 2.0 | | V |
| I_{IL} | Input LOW Current | $V_{IN} = 0\text{ V}$ | | 50 | μA |
| I_{IH} | Input HIGH Current | $V_{IN} = V_{DD}$ | | 100 | μA |
| V_{OL} | Output LOW Voltage | $I_{OL} = 8\text{ mA (-1)}$ $I_{OL} = 12\text{ mA (-1H)}$ | | 0.4 | V |
| V_{OH} | Output HIGH Voltage | $I_{OH} = -8\text{ mA (-1)}$ $I_{OH} = -12\text{ mA (-1H)}$ | 2.4 | | V |
| I_{DD} | Supply Current (Commercial Temp) | Unloaded outputs at 66.67 MHz, Select inputs at V_{DD} | | 34 | mA |
| I_{DD} | Supply Current (Industrial Temp) | Unloaded outputs at 100 MHz 66.67 MHz 33 MHz Select inputs at V_{DD} or GND, at Room Temp | | 50 34 19 | mA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. REF input has a threshold voltage of $V_{DD}/2$.

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Table 5. SWITCHING CHARACTERISTICS $V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ (Note 4)

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|------------|--|---|----------|----------|------------|------|
| $1/t_1$ | Output Frequency | 30 pF load 10 pF load | 15 15 | | 100 133 | MHz |
| $1/t_1$ | Duty Cycle = $(t_2 / t_1) * 100$ (-1, -1H) (-1H) | Measured at 1.4 V, $F_{OUT} = 66.67\text{ MHz}$ < 50 MHz | 40 45 | 50 50 | 60 55 | % |
| t_3 | Output Rise Time (-1) (-1H) | Measured between 0.8 V and 2.0 V | | | 2.5 1.5 | ns |
| t_4 | Output Fall Time (-1) (-1H) | Measured between 2.0 V and 0.8 V | | | 2.5 1.5 | ns |
| t_5 | Output-to-Output Skew | All outputs equally loaded | | | 250 | ps |
| t_6 | Delay, REF Rising Edge to CLKOUT Rising Edge | Measured at $V_{DD}/2$ | | 0 | ± 350 | ps |
| t_7 | Device-to-Device Skew | Measured at $V_{DD}/2$ on the CLKOUT pins of the device | | 0 | 700 | ps |
| t_J | Cycle-to-Cycle Jitter | Measured at 66.67 MHz, loaded outputs | | | 200 | ps |
| t_{LOCK} | PLL Lock Time | Stable power supply, valid clock presented on REF pin | | | 1.0 | ms |

4. All parameters specified with loaded outputs.

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, for obtaining zero-input-output delay.

SWITCHING WAVEFORMS

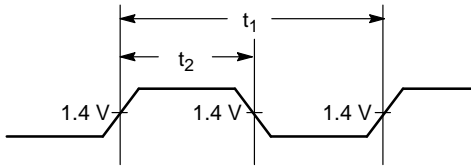


Figure 3. Duty Cycle Timing

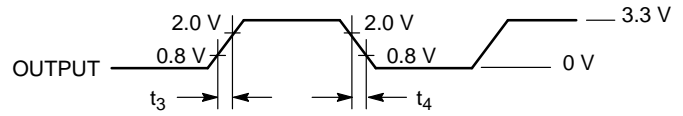


Figure 4. All Outputs Rise/Fall Time

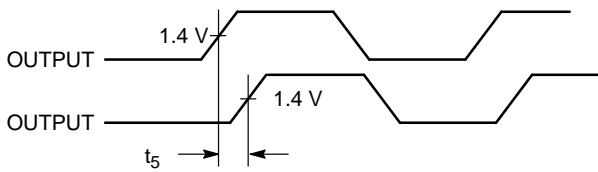


Figure 5. Output - Output Skew

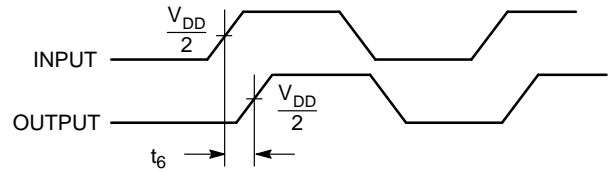


Figure 6. Input - Output Propagation Delay

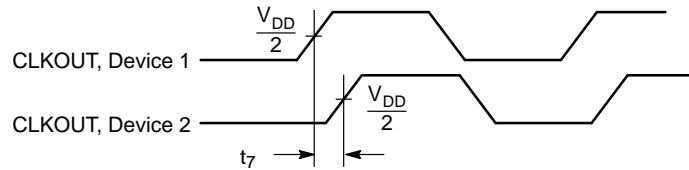


Figure 7. Device - Device Skew

NB2305A

TEST CIRCUITS

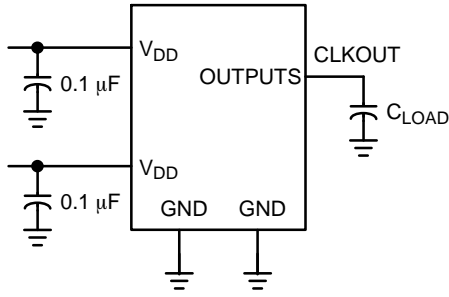


Figure 8. Test Circuit #1

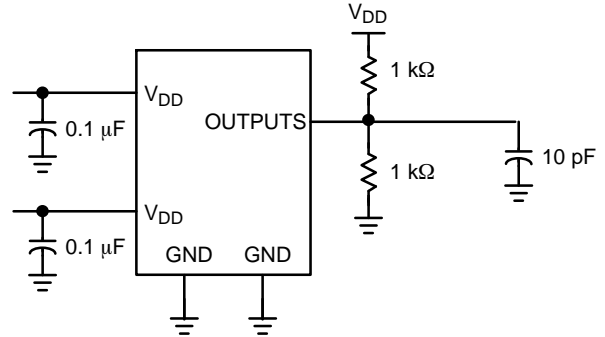


Figure 9. Test Circuit #2
For parameter t_8 (output slew rate) on -1H devices

ORDERING INFORMATION

| Device | Marking | Operating Range | Package | Shipping [†] | Availability |
|-----------------|---------|-------------------------|-------------------|-----------------------|--------------|
| NB2305AI1DG | 511 | Industrial & Commercial | SOIC-8 (Pb-Free) | 98 Units / Rail | Now |
| NB2305AI1DR2G | 511 | Industrial & Commercial | SOIC-8 (Pb-Free) | 2500 Tape & Reel | Now |
| NB2305AI1HDG | 511H | Industrial & Commercial | SOIC-8 (Pb-Free) | 98 Units / Rail | Now |
| NB2305AI1HDR2G | 511H | Industrial & Commercial | SOIC-8 (Pb-Free) | 2500 Tape & Reel | Now |
| NB2305AI1DTG | 511 | Industrial & Commercial | TSSOP-8 (Pb-Free) | 100 Units / Rail | Now |
| NB2305AI1DTR2G | 511 | Industrial & Commercial | TSSOP-8 (Pb-Free) | 2500 Tape & Reel | Now |
| NB2305AI1HDTG | 5IH | Industrial & Commercial | TSSOP-8 (Pb-Free) | 100 Units / Rail | Now |
| NB2305AI1HDTR2G | 5IH | Industrial & Commercial | TSSOP-8 (Pb-Free) | 2500 Tape & Reel | Now |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

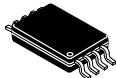
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|--|---|---|---|
| <p>STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER</p> | <p>STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1</p> | <p>STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1</p> | <p>STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE</p> |
| <p>STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE</p> | <p>STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE</p> | <p>STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd</p> | <p>STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1</p> |
| <p>STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON</p> | <p>STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND</p> | <p>STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1</p> | <p>STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> | <p>STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN</p> | <p>STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON</p> | <p>STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC</p> | <p>STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE</p> | <p>STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1</p> | <p>STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6</p> | <p>STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND</p> | <p>STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT</p> | <p>STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT</p> | <p>STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC</p> | <p>STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN</p> | <p>STYLE 28: PIN 1. SW_TO_GND 2. DASIC OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN</p> |
| <p>STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1</p> | <p>STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1</p> | | |

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

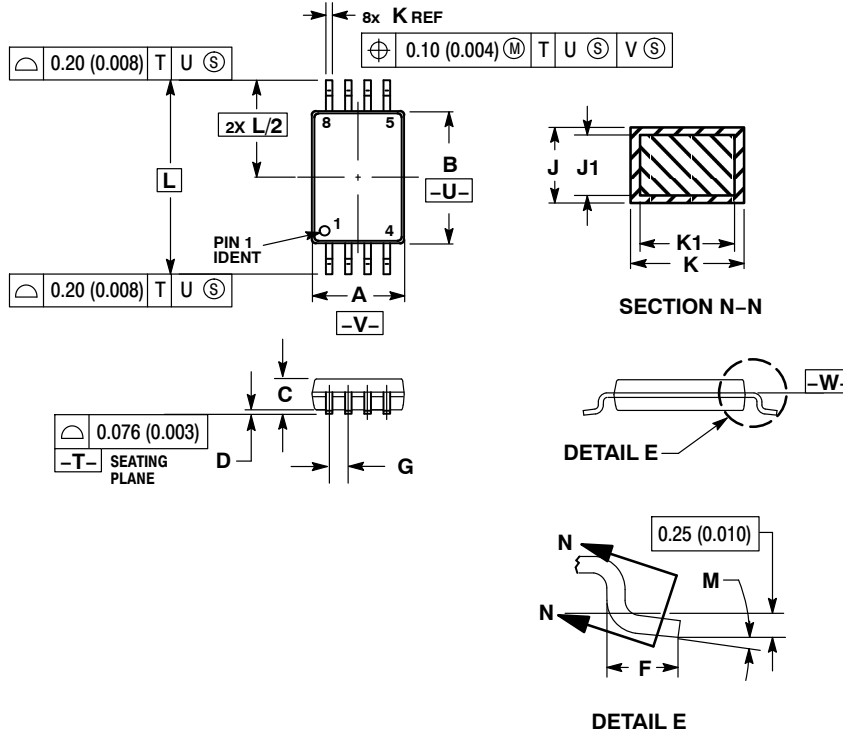
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SCALE 2:1

TSSOP-8
CASE 948S-01
ISSUE C

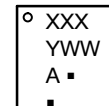
DATE 20 JUN 2008



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.10 | --- | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.70 | 0.020 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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