NB3H63143G

3.3 V / 2.5 V Programmable OmniClock Generator

with Single Ended (LVCMOS/LVTTL) and Differential (LVPECL/LVDS/ HCSL/CML) Outputs with Individual Output Enable and Individual VDDO

The NB3H63143G, which is a member of the OmniClock family, is a one−time programmable (OTP), low power PLL−based clock generator that supports any output frequency from 8 kHz to 200 MHz. The device accepts fundamental mode parallel resonant crystal or a single ended (LVCMOS/LVTTL) reference clock as input. It generates either three single ended (LVCMOS/LVTTL) outputs, or one single ended output and one differential (LVPECL/LVDS/HCSL/CML) output. The output signals can be modulated using the spread spectrum feature of the PLL (programmable spread spectrum type, deviation and rate) for applications demanding low electromagnetic interference (EMI). Individual output enable pins OE[2:0] are available to enable/disable the outputs. Individual output voltage pins VDDO[2:0] are available to independently set the output voltage of each output. Up to four different configurations can be written into the device memory. Two selection pins (SEL[1:0]) allow the user to select the configuration to use. Using the PLL bypass mode, it is possible to get a copy of the input clock on any or all of the outputs. The device can be powered down using the Power Down pin (PD#). It is possible to program the internal input crystal load capacitance and the output drive current provided by the device. The device also has automatic gain control (crystal power limiting) circuitry which avoids the device overdriving the external crystal.

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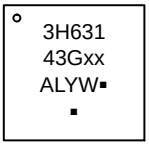
QFN16
CASE 485AE

MARKING DIAGRAM



3H63143G	= Specific Device Code
xx	= Specific Program Code (Default ‘00’ for Unprogrammed Part)
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 23 of this data sheet.

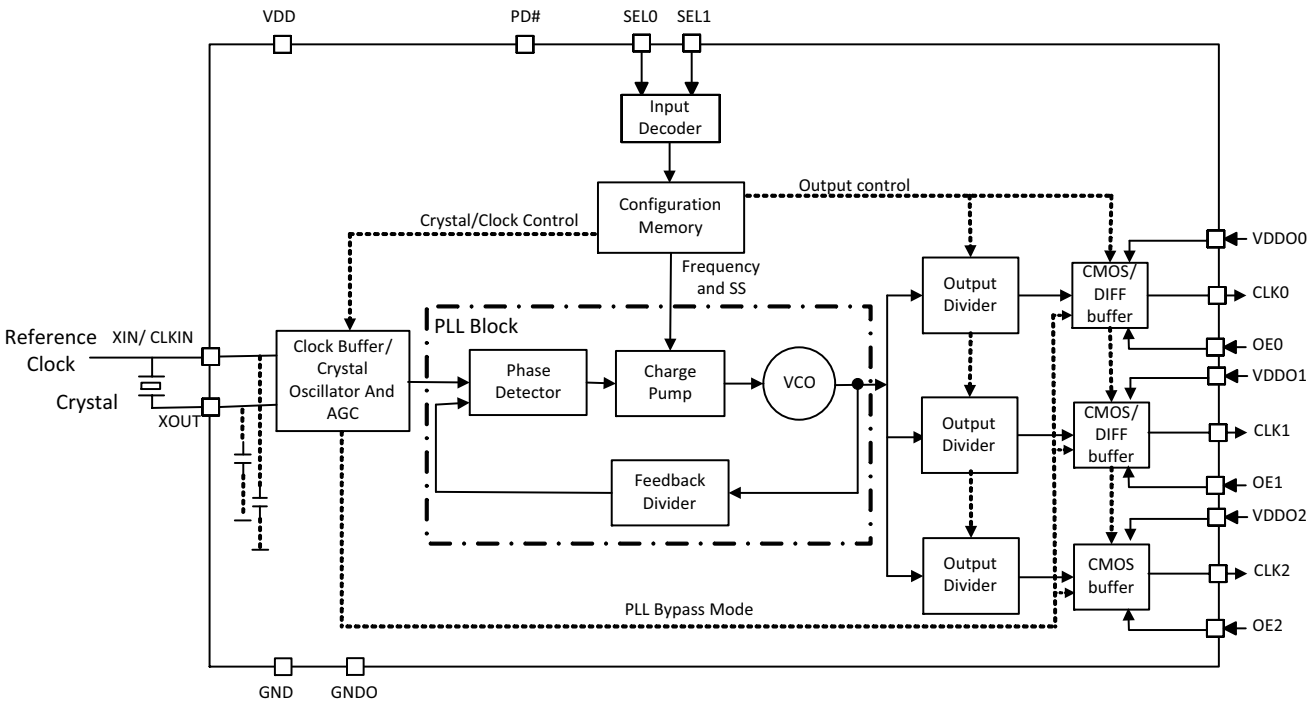
Features

- Member of the OmniClock Family of Programmable Clock Generators
- Operating Power Supply: 3.3 V ±10%, 2.5 V ±10%
- I/O Standards
  - Inputs: LVCMOS/LVTTL, Fundamental Mode Crystal
  - Outputs: 1.8 V to 3.3 V LVCMOS/LVTTL
  - Outputs: LVPECL, LVDS, HCSL and CML
- 3 Programmable Single Ended (LVCMOS/LVTTL) Outputs from 8 kHz to 200 MHz
- 1 Programmable Differential Clock Output up to 200 MHz
- Input Frequency Range
  - Crystal: 3 MHz to 50 MHz
  - Reference Clock: 3 MHz to 200 MHz
- Configurable Spread Spectrum Frequency Modulation Parameters (Type, Deviation, Rate)
- Individual Output Enable Pins
- Independent Output Voltage Pins
- Programmable Internal Crystal Load Capacitors
- Programmable Output Drive Current for Single Ended Outputs
- Power Saving Mode through Power Down Pin
- Programmable PLL Bypass Mode
- Programmable Output Inversion
- Programming and Evaluation Kit Available for Field Programming and Quick Evaluation
- Temperature Range −40°C to 85°C
- Packaged in 16−pin QFN
- These are Pb−Free Devices

Typical Applications

- eBooks and Media Players
- Smart Wearables, Smart Phones, Portable Medical and Industrial Equipment
- Set Top Boxes, Printers, Digital Cameras and Camcorders

BLOCK DIAGRAM



Notes:
1. CLK0 and CLK1 can be configured to be one LVPECL, LVDS, HCSL or CML output, or two single ended LVCMOS/LVTTL outputs.
2. Dotted lines are the programmable control signals to internal IC blocks.
3. OE[2:0], SEL[1:0] have internal pull up resistors. PD# has internal pull down resistor.

Figure 1. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

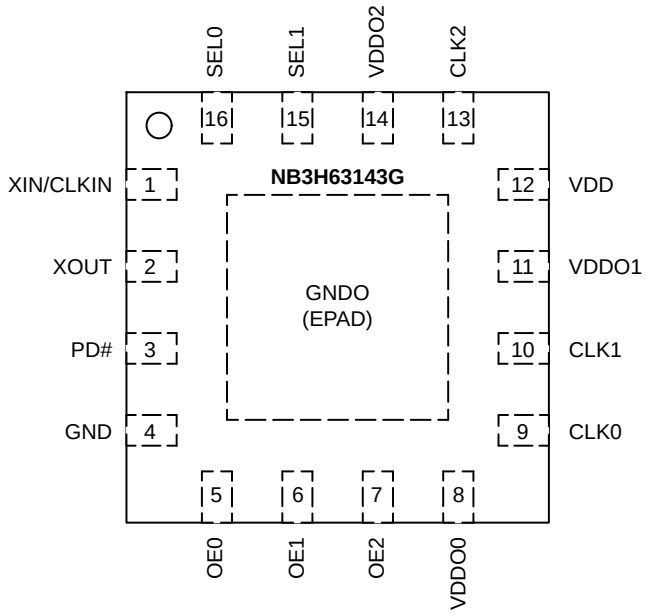


Figure 2. Pin Connections (Top View) − QFN16 (with EPAD)

Table 1. PIN DESCRIPTION

Pin No.	Pin Name	Pin Type	Description
1	XIN/CLKIN	Input	3 MHz to 50 MHz crystal input connection or an external single ended reference input clock between 3 MHz and 200 MHz.
2	XOUT	Output	Crystal output. Float this pin when external reference clock is connected at XIN.
3	PD#	Input	Asynchronous LVCMOS/LVTTL input. Active Low Master Reset to disable the device and set outputs Low. Internal pull−down resistor. This pin needs to be pulled High for normal operation of the chip.
4	GND	Ground	Power supply ground.
5, 6, 7	OE[2:0]	Input	2−Level LVCMOS/LVTTL Inputs for Enabling/Disabling output clocks CLK[2:0] respectively. Internal pull−up resistor.
8	VDDO0	Power	CLK0 Output power supply ≤ VDD
9	CLK0	SE/DIFF Output	Supports 8 kHz to 200 MHz Single Ended (LVCMOS/LVTTL) signals or Differential (LVPECL/LVDS/HCSL/CML) signals. Using PLL Bypass mode, the output can also be a copy of the input clock. The single ended output will be LOW and differential outputs will be complementary LOW/HIGH until the PLL has locked and the frequency has stabilized.
10	CLK1	SE/DIFF Output	Supports 8 kHz to 200 MHz Single Ended (LVCMOS/LVTTL) signals or Differential (LVPECL/LVDS/HCSL/CML) signals. Using PLL Bypass mode, the output can also be a copy of the input clock. The single ended output will be LOW and differential outputs will be complementary LOW/HIGH until the PLL has locked and the frequency has stabilized.
11	VDDO1	Power	CLK1 Output power supply ≤ VDD
12	VDD	Power	3.3V / 2.5V power supply.
13	CLK2	SE Output	Supports 8 kHz to 200 MHz Single Ended (LVCMOS/LVTTL) signals. Using PLL Bypass mode, the output can also be a copy of the input clock. The single ended output will be LOW until the PLL has locked and the frequency has stabilized.
14	VDDO2	Power	CLK2 Output power supply ≤ VDD
15, 16	SEL[1:0]	Input	2−Level LVCMOS/LVTTL Inputs for Configuration Selection. Configuration parameters include individual output frequencies, spread spectrum configuration, enable/disable status of each output, output type, internal crystal load capacitance configuration, etc. Configuration can be switched dynamically, but may require the PLL to re−lock. Internal pull−up resistor.
EPAD	GNDO	Ground	Power supply ground for Outputs.

Table 2. OUTPUT CONFIGURATION SELECT FUNCTION TABLE

SEL1	SEL0	Output Configuration
L	L	I
L	H	II
H	L	III
H	H	IV

Table 3. POWER DOWN FUNCTION TABLE

PD#	Function
0	Device Powered Down
1	Device Powered Up

Table 4. OUTPUT ENABLE FUNCTION TABLE

OE[2:0]	Function
0	CLK Disabled
1	CLK Enabled

TYPICAL CRYSTAL PARAMETERS

Crystal: Fundamental Mode Parallel Resonant

Frequency: 3 MHz to 50 MHz

Table 5. MAX CRYSTAL LOAD CAPACITORS RECOMMENDATION

Crystal Frequency Range	Max Cap Value
3 MHz − 30 MHz	20 pF
30 MHz − 50 MHz	10 pF

Shunt Capacitance (C0): 7 pF (Max)

Equivalent Series Resistance 150 Ω (Max)

FUNCTIONAL DESCRIPTION

The NB3H63143G is a 3.3 V/2.5 V programmable, single ended/differential clock generator, designed to meet the timing requirements for consumer and portable markets. It has a small package size and it requires low power during operation and while in standby. This device provides the ability to configure a number of parameters as detailed in the following section. The One−Time Programmable memory allows programming and storing of up to four configurations in the memory space.

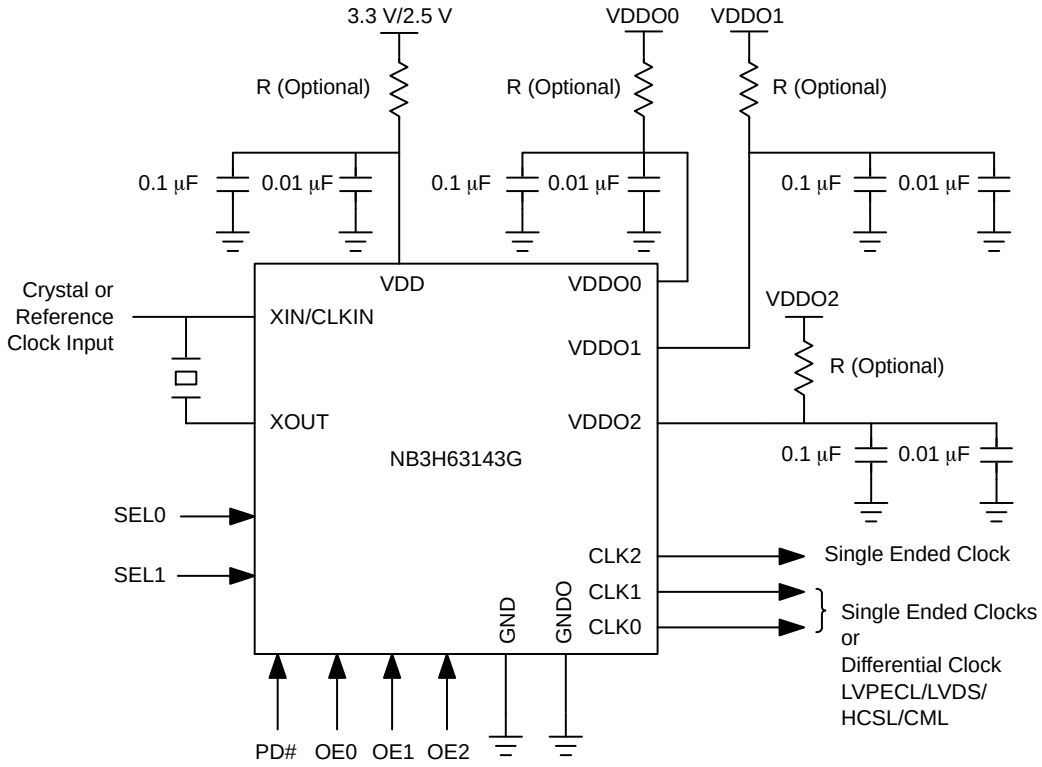


Figure 3. Power Supply and Output Supply Noise Suppression

Power Supply

Device Supply

The NB3H63143G is designed to work with a 3.3 V/2.5 V VDD power supply. For VDD operation of 1.8 V, refer to the NB3V63143G datasheet. In order to suppress power supply noise it is recommended to connect decoupling capacitors of 0.1 μF and 0.01 μF close to the VDD pin as shown in Figure 3.

Output Power Supply

Each output CLK[2:0] has a separate output power supply VDDO[2:0] pin to control its output voltage. The output power supply can be as high as VDD. It can be as low as 2.5 V for clock output types LVPECL/CML and as low as 1.8 V if using other clock output types. This feature removes the need for external voltage converters for each of the outputs thus reducing component count, saving board space and facilitating board design. In order to suppress power supply noise it is recommended to connect decoupling capacitors of 0.1 μF and 0.01 μF close to each VDDO pin as shown in Figure 3.

Clock Input

Input Frequency

The clock input block can be programmed to use a fundamental mode crystal from 3 MHz to 50 MHz or a single ended reference clock source from 3 MHz to 200 MHz. When using output frequency modulation for EMI reduction, for optimal performance, it is recommended to use crystals with a frequency greater than 6.75 MHz as input. Crystals with ESR values of up to 150 Ω are supported. While using a crystal as input, it is important to set crystal load capacitor values correctly to achieve good performance.

Programmable Crystal Load Capacitors

The provision of internal programmable crystal load capacitors eliminates the necessity of external load capacitors for standard crystals. The internal load capacitors can be programmed to any value between 4.36 pF and 20.39 pF with a step size of 0.05 pF. Refer to Table 5 for recommended maximum load capacitor values for stable operation. There are three modes of loading the crystal − with internal chip capacitors only, with external capacitors only or with the both internal and external capacitors. Check with the crystal vendor's load capacitance specification for setting of the internal load capacitors. The minimum value of 4.36 pF internal load capacitor need to be considered while selecting external capacitor value. The internal load capacitors will be bypassed when using an external reference clock.

Automatic Gain Control (AGC)

The Automatic Gain Control (AGC) feature adjusts the gain to the input clock based on its signal strength to maintain a good quality input clock signal level. This feature takes care of low clock swings fed from external reference clocks and ensures proper device operation. It also enables maximum compatibility with crystals from different manufacturers, processes, quality and performance. AGC also takes care of power dissipation in the crystal; avoids overdriving the crystal and thus extending the crystal life. In order to calculate the AGC gain accurately and avoid increasing the jitter on the output clocks, the user needs to provide the crystal load capacitance as well as other crystal parameters like ESR and shunt capacitance (C0).

Programmable Clock Outputs

Output Type and Frequency

The NB3H63143G provides three independent single ended LVCMOS/LVTTL outputs, or one single ended LVCMOS/LVTTL output and one LVPECL/LVDS/HCSL/CML differential output. The device supports any single ended output or differential output frequency from 8 kHz up to 200 MHz with or without frequency modulation. All outputs have individual output enable pins (refer to the Output Enable/Disable section on page 7). It should be noted that certain combinations of output frequencies and spread spectrum configurations may not be recommended for optimal and stable operation.

For differential clocking, CLK0 and CLK1 can be configured as LVPECL, LVDS, HCSL or CML. While using differential signaling format at the output, it is required to use only VDDO1 as output supply and use only the OE1 pin for the output enable function. (refer to the Application Schematic in Figure 4). When all 3 outputs are single ended, VDDO0 and OE0 have normal functionality.

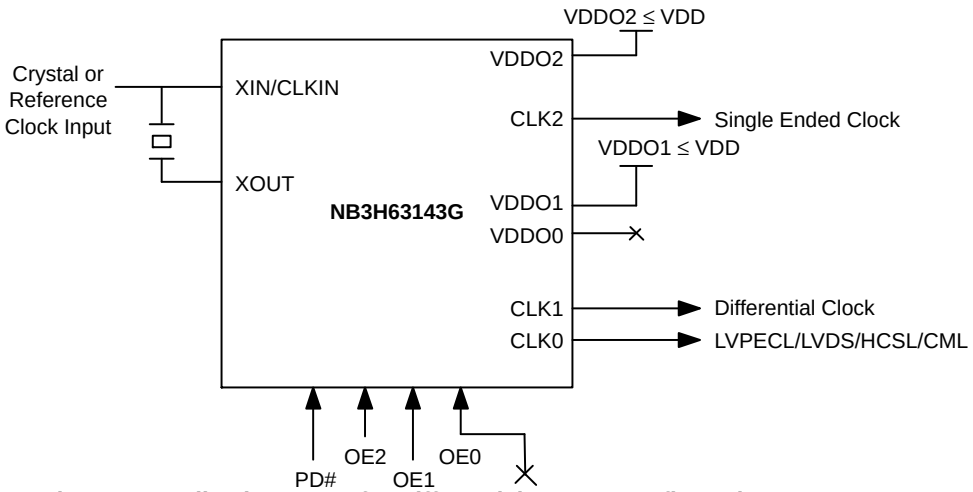


Figure 4. Application Setup for Differential Output Configuration

Programmable Output Drive

The drive strength or output current of each of the LVCMOS clock outputs is programmable independently. For each VDDO supply voltage, four distinct levels of LVCMOS output drive strengths can be selected as mentioned in DC Electrical Characteristics. This feature provides further load drive and signal conditioning as per the application requirement.

PLL BYPASS Mode

PLL Bypass mode can be used to buffer the input clock on any of the outputs or all of the outputs. Any of the clock outputs can be programmed to generate a copy of the input clock.

Output Inversion

All output clocks of the NB3H63143G can be phase inverted relative to each other. This feature can also be used in conjunction with the PLL BYPASS mode.

Spread Spectrum Frequency Modulation

Spread spectrum is a technique using frequency modulation to achieve lower peak electromagnetic interference (EMI). It is an elegant solution compared to techniques of filtering and shielding. The NB3H63143G modulates the output of its PLL in order to “spread” the bandwidth of the synthesized clock, decreasing the peak amplitude at the center frequency and at the frequency’s harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum modulation’.

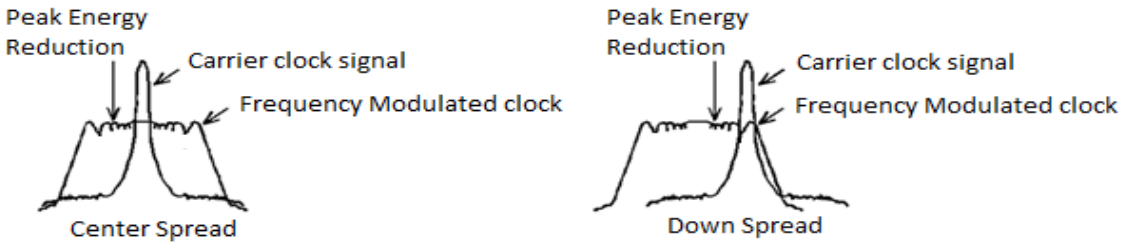


Figure 5. Frequency Modulation or Spread Spectrum Clock for EMI Reduction

The outputs of the NB3H63143G can be programmed to have either center spread from ±0.125% to ±3% or down spread from −0.25% to −4%. The programmable step size for spread spectrum deviation is 0.125% for center spread and 0.25% for down spread respectively. Additionally, the frequency modulation rate is also programmable. Frequency modulation from 30 kHz to 130 kHz can be selected. Spread spectrum, when on, applies to all the outputs of the device but not to output clocks that use the PLL bypass feature. There exists a tradeoff between the input clock frequency and the desired spread spectrum profile. For certain combinations of input frequency and modulation rate, the device operation could be unstable and should be avoided. For spread spectrum applications, the following limits are recommended:

Fin (Min) = 6.75 MHz

Fmod (range) = 30 kHz to 130 kHz

Fmod (Max) = Fin / 225

For any input frequency selected, the above limits must be observed for a good spread spectrum profile.

For example, the minimum recommended reference frequency for a modulation rate of 30 kHz would be 30 kHz * 225 = 6.75 MHz. For 27 MHz, the maximum recommended modulation rate would be 27 MHz / 225 = 120 kHz

Control Inputs

Configuration Space Selection

The SEL[1:0] pins are used to select one of the pre−programmed configurations statically or dynamically while the device is powered on. These pins are 2−level LVCMOS/LVTTL. Up to four configurations can be stored in the memory space of the device. Clock outputs can be independently enabled or disabled through the configuration space. To have a given clock output enabled, it must be enabled in both the configuration space and through its respective output enable pin.

The PLL re−locking and stabilization time must be taken into consideration when dynamically changing the configurations. Table 6 shows an example of four configurations.

Table 6. EXAMPLE CONFIGURATION SPACE SETTINGS

Configuration Selection	Input Frequency	Output Frequency	VDD	VDDO	SS%	SS Mod Rate	Output Drive	Output Inversion	Output Enable	PLL Bypass	Notes
I	25 MHz	CLK0=100 MHz CLK1=8 kHz CLK2=25 MHz	3.3 V	VDDO0=2.5 V VDDO1=1.8 V VDDO2=1.8 V	−0.5%	110 kHz	CLK0=12mA CLK1=8mA CLK2=4mA	CLK0=N CLK1=N CLK2=Y	CLK0=Y CLK1=Y CLK2=Y	CLK0=N CLK1=N CLK2=Y	CLK2 Ref clk
II	40 MHz	CLK0=125 MHz CLK1=40 MHz CLK2=10 MHz	3.3 V	VDDO0=2.5 V VDDO1=1.8 V VDDO2=1.8 V	±0.25%	30 kHz	CLK0=4mA CLK1=4mA CLK2=4mA	CLK0=N CLK1=N CLK2=N	CLK0=Y CLK1=Y CLK2=Y	CLK0=N CLK1=Y CLK2=N	CLK1 Ref clk
III	100 MHz	CLK0=100 MHz CLK1=100 MHz CLK2=100 MHz	3.3 V	VDDO0=2.5 V VDDO1=1.8 V VDDO2=1.8 V	No SS	NA	CLK0=12mA CLK1=8mA CLK2=4mA	CLK0=N CLK1=Y CLK2=Y	CLK0=Y CLK1=Y CLK2=Y	CLK0=Y CLK1=Y CLK2=Y	All Three Outputs are Ref clks
IV	25 MHz	CLK0=100 MHz CLK1=100 MHz CLK2=48 MHz	3.3 V	VDDO0=NA VDDO1=2.5 V VDDO2=3.3 V	−1%	100 kHz	CLK2=16mA	CLK0=NA CLK1=NA CLK2=N	CLK0=NA CLK1=Y CLK2=Y	CLK0=NA CLK1=N CLK2=N	CLK[1:0] is Differential Output

Output Enable/Disable

Output Enable pins (OE[2:0]) are LVCMOS/LVTTL input pins that individually enable or disable the outputs CLK[2:0] respectively. These inputs only disable the output buffers thus not affecting the rest of the blocks on the device. When using a differential output, only the OE1 pin must be used to enable/disable the differential output (the OE0 pin will be ignored). The hardware OE pins have an effect only when the respective outputs are enabled in the configuration space. The output disable state can be set to high impedance (Hi−Z) or Low.

Power Down

Power saving mode can be activated though the power down PD# input pin. This input is an LVCMOS/LVTTL active Low Master Reset that disables the device and sets the outputs Low. By default it has an internal pull−down resistor. The device functions are disabled by default and when the PD# pin is pulled high the device functions are activated.

Default Device State

The NB3H63143G parts shipped from ON Semiconductor are blank, with no inputs/outputs programmed. The parts need to be programmed by the field sales or by a distributor or by the users themselves before they can be used. Programmable clock software downloadable from the ON Semiconductor website can be used along with the programming kit to achieve this purpose. For mass production, parts can be factory programmed with a customer qualified configuration and sourced from ON Semiconductor as a dash part number (Eg. NB3H63143G−01).

Table 7. ATTRIBUTES

Characteristic	Value
ESD Protection − Human Body Model	2 kV
Internal Input Default State Pull Up/Down Resistor	50 kΩ
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)	MSL1
Flammability Rating − Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125in
Transistor Count	130k
Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Rating	Unit
VDD	Positive Power Supply with Respect to Ground	−0.5 to +4.6	V
V_I	Input Voltage with Respect to Chip Ground	−0.5 to VDD + 0.5	V
T_A	Operating Ambient Temperature Range (Industrial Grade)	−40 to +85	°C
T_{STG}	Storage Temperature	−65 to +150	°C
T_{SOL}	Max. Soldering Temperature (10 sec)	265	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3) 0 lfpm 500 lfpm	 32.3 24.22	 °C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	3.6	°C/W
T_J	Junction Temperature	125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power). JESD51.7 type board. Back side Copper heat spreader area 100 sqmm, 2 oz (0.070mm) copper thichness.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD	Core Power Supply Voltage	3.3 V operation 2.5 V operation	2.97 2.25	3.3 2.5	3.63 2.75	V
VDDO[2:0]	Output Power Supply Voltage (Note 4)	3.3 V operation 2.5 V operation 1.8 V operation	2.97 2.25 1.7	3.3 2.5 1.8	3.63 2.75 1.9	V
CL	Clock output load capacitance for LVCMOS / LVTTL clock	fout < 100 MHz fout ≥ 100 MHz			15 5	pF
fclkin	Crystal Input Frequency Reference Clock Frequency	Fundamental Crystal Single ended clock input	3 3		50 200	MHz
C_X	Xin / Xout pin stray capacitance	(Note 5)		4.5		pF
C_{XL}	Crystal load capacitance	(Note 6)		10		pF
ESR	Crystal ESR				150	Ω

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. The output power supply voltage VDDO[2:0] must always be less than or equal to core power supply voltage VDD.
5. The Xin/ Xout pin stray capacitance needs to be subtracted from crystal load capacitance (along with PCB and trace capacitance) while selecting appropriate load for the crystal in order to get minimum ppm error.
6. Refer to XTAL parameters supplied by the vendor.

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3 V ±10%, 2.5 V ±10%, VDDO[2:0] = 3.3 V ± 10%, 2.5 V ± 10%, 1.8 V ± 0.1V; GND = 0 V, T_A = −40°C to 85°C, Note 7)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{DD\_3.3\ V}$	Power Supply Current for Core	Configuration Dependent. VDD = 3.3 V, T_A = 25°C, XIN/CLKIN = 25 MHz (XTAL), CLK[0:2] = 100 MHz, 16 mA output drive		13		mA
$I_{DD\_2.5\ V}$	Power Supply Current for Core	Configuration Dependent. VDD = 2.5 V, T_A = 25°C, XIN/CLKIN = 25 MHz (XTAL), CLK[0:2] = 100 MHz, 12 mA output drive		13		mA
I_{PD}	Power Down Supply Current	PD# is Low to Make All Outputs OFF			20	μA
V_{IH}	Input HIGH Voltage	Pins XIN, SEL[1:0], OE[2:0]	0.65 V_{DD}		V_{DD}	V
		Pin PD#	0.85 V_{DD}		V_{DD}	
V_{IL}	Input LOW Voltage	Pins XIN, SEL[1:0], OE[2:0]	0		0.35 V_{DD}	V
		Pin PD#	0		0.15 V_{DD}	
Zo	Nominal Output Impedance	Configuration Dependent. 12 mA Drive		22		Ω
$R_{PUP/PD}$	Internal Pull Up/ Pull Down Resistor	VDD = 3.3 V VDD = 2.5 V		50 80		kΩ
Cprog	Programmable Internal Crystal Load Capacitance	Configuration Dependent	4.36		20.39	pF
	Programmable Internal Crystal Load Capacitance Resolution			0.05		
Cin	Input Capacitance	Pins PD#, SEL[1:0], OE[2:0]		4	6	pF

DC ELECTRICAL CHARACTERISTICS (continued)
(V_{DD} = 3.3 V ±10%, 2.5 V ±10%, VDDO[2:0] = 3.3 V ± 10%, 2.5 V ± 10%, 1.8 V ± 0.1V; GND = 0 V, T_A = −40°C to 85°C, Note 7)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
LVCMOS/LVTTL OUTPUTS						
V_{OH}	Output HIGH Voltage	VDDO = 3.3 V, I_{OH} = 4 mA	0.75xVDDO			V
		VDDO = 3.3 V, I_{OH} = 8 mA				
		VDDO = 3.3 V, I_{OH} = 12 mA				
		VDDO = 3.3 V, I_{OH} = 16 mA				
		VDDO = 2.5 V, I_{OH} = 2 mA				
		VDDO = 2.5 V, I_{OH} = 4 mA				
		VDDO = 2.5 V, I_{OH} = 8 mA				
		VDDO = 2.5 V, I_{OH} = 12 mA				
		VDDO = 1.8 V, I_{OH} = 1 mA				
		VDDO = 1.8 V, I_{OH} = 2 mA				
		VDDO = 1.8 V, I_{OH} = 4 mA				
		VDDO = 1.8 V, I_{OH} = 8 mA				
V_{OL}	Output LOW Voltage	VDDO = 3.3 V, I_{OL} = 4 mA			0.25xVDDO	V
		VDDO = 3.3 V, I_{OL} = 8 mA				
		VDDO = 3.3 V, I_{OL} = 12 mA				
		VDDO = 3.3 V, I_{OL} = 16 mA				
		VDDO = 2.5 V, I_{OL} = 2 mA				
		VDDO = 2.5 V, I_{OL} = 4 mA				
		VDDO = 2.5 V, I_{OL} = 8 mA				
		VDDO = 2.5 V, I_{OL} = 12 mA				
		VDDO = 1.8 V, I_{OL} = 1 mA				
		VDDO = 1.8 V, I_{OL} = 2 mA				
		VDDO = 1.8 V, I_{OL} = 4 mA				
		VDDO = 1.8 V, I_{OL} = 8 mA				
I_{DDO_LVCMOS}	LVCMOS Output Supply Current	Configuration Dependent. T_A = 25°C, CLK[0:2] = f_{out} in PLL bypass mode				mA
		Measured on VDDO = 3.3 V				
		f_{out} = 33.33 MHz, C_L = 5 pF		6		
		f_{out} = 100 MHz, C_L = 5 pF		16		
		f_{out} = 200 MHz, C_L = 5 pF		32		
		Measured on VDDO = 2.5 V				
		f_{out} = 33.33 MHz, C_L = 5 pF		4		
		f_{out} = 100 MHz, C_L = 5 pF		12		
		f_{out} = 200 MHz, C_L = 5 pF		24		
		Measured on VDDO = 1.8 V				
		f_{out} = 33.33 MHz, C_L = 5 pF		3		
		f_{out} = 100 MHz, C_L = 5 pF		8		
		f_{out} = 200 MHz, C_L = 5 pF		16		

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3 V ±10%, 2.5 V ±10%, VDDO[2:0] = 3.3 V ± 10%, 2.5 V ± 10%, 1.8 V ± 0.1 V; GND = 0 V, T_A = −40°C to 85°C, Note 19)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
HCSL OUTPUTS (Note 8)						
V_{OH_HCSL}	Output HIGH Voltage (Note 9)	VDDO = 3.3 V, 2.5 V, 1.8 V		700		mV
V_{OL_HCSL}	Output Low Voltage (Note 9)	VDDO = 3.3 V, 2.5 V, 1.8 V		0		mV
V_{CROSS}	Crossing Point Voltage (Notes 10 and 11)	VDDO = 3.3 V, 2.5 V	250	350	450	mV
Delta V_{cross}	Change in Magnitude of V_{cross} for HCSL Output (Notes 10 and 12)	VDDO = 3.3 V, 2.5 V			150	mV
I_{DDO_HCSL}	Measured on VDDO0 = 2.5 V & 3.3 V with	f_{out} = 100 MHz, CL = 2 pF f_{out} = 200 MHz, CL = 2 pF		22		mA
LVDS OUTPUTS (Notes 10 and 13)						
V_{OD_LVDS}	Differential Output Voltage		250		450	mV
DeltaV_{OD_LVDS}	Change in Magnitude of V_{OD} for Complementary Output States		0		25	mV
V_{OS_LVDS}	Offset Voltage	VDDO = 2.5 V / 3.3 V VDDO = 1.8 V		1200 900		mV
Delta V_{OS_LVDS}	Change in Magnitude of V_{OS} for Complementary Output States		0		25	mV
V_{OH_LVDS}	Output HIGH Voltage (Note 14)	VDDO = 2.5 V / 3.3 V VDDO = 1.8 V		1425 1100	1600 1250	mV
V_{OL_LVDS}	Output LOW Voltage (Note 15)	VDDO = 2.5 V / 3.3 V VDDO = 1.8 V	900 700	1075 800		mV
I_{DDO_LVDS}		f_{out} = 100 MHz f_{out} = 200 MHz		14		mA
LVPECL OUTPUTS (Notes 16 and 17)						
V_{OH_LVPECL}	Output HIGH Voltage	VDDO = 2.5 V VDDO = 3.3 V	VDDO−1450	VDDO−900 1600 2400	VDDO−825	mV
V_{OL_LVPECL}	Output LOW Voltage	VDDO = 2.5 V VDDO = 3.3 V	VDDO−2000	VDDO−1700 800 1600	VDDO−1500	mV
V_{SWING}	Peak−to−Peak output voltage swing		550	800	930	mV
Vcross	Crossover point voltage (Note 17)	VDDO = 2.5 V VDDO = 3.3 V	270		380	
I_{DDO_LVPECL}		f_{out} = 100 MHz f_{out} = 200 MHz		25		mA
CML OUTPUTS (Notes 17 and 18)						
V_{OH_CML}	Output HIGH Voltage	VDDO = 3.3 V VDDO = 2.5 V	VDDO −60 3240 2440	VDDO−10 3290 2490	VDDO 3300 2500	mV
V_{OL_CML}	Output LOW Voltage	VDDO = 3.3 V VDDO = 2.5 V	VDDO −1100 2200 1400	VDDO−800 2500 1700	VDDO − 640 2660 1860	mV
V_{OD_CML}	Differential Output Voltage Magnitude	VDDO = 3.3 V VDDO = 2.5 V	640	780	1000	mV
Vcross	Crossover point voltage (Note 17)	VDDO = 3.3 V VDDO = 2.5 V		VDDO−395		

DC ELECTRICAL CHARACTERISTICS (continued)
(V_{DD} = 3.3 V ±10%, 2.5 V ±10%, VDDO[2:0] = 3.3 V ± 10%, 2.5 V ± 10%, 1.8 V ± 0.1 V; GND = 0 V, T_A = −40°C to 85°C, Note 19)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
CML OUTPUTS (Notes 17 and 18)						
I_{DDO_CML}		f_{out} = 100 MHz f_{out} = 200 MHz		5.0		mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

7. Measurement taken with single ended clock outputs terminated with test load capacitance of 5 pF and 15 pF and differential clock terminated with test load of 2 pF. See Figures 6, 7 and 12. Specifications for LVTTL are valid for VDD and VDDO 3.3 V only.
8. Measurement taken with outputs terminated with RS = 0 Ω, RL = 50 Ω, with test load capacitance of 2 pF. See Figure 8. Guaranteed by characterization.
9. Measurement taken from single ended waveform.
10. Measured at crossing point where the instantaneous voltage value of the rising edge of CLKx+ equals the falling edge of CLKx−.
11. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
12. Defined as the total variation of all crossing voltage of rising CLKx+ and falling CLKx−. This is maximum allowed variance in the VCROSS for any particular system.
13. LVDS outputs require 100 Ω receiver termination resistor between differential pair. See Figure 9.
14. VOHmax = VOSmax + 1/2 VODmax.
15. VOLmax = VOSmin − 1/2 VODmax.
16. LVPECL outputs loaded with 50 Ω to VDDO1 − 2.0 V for proper operation.
17. Output parameters vary 1:1 with VDDO1.
18. CML outputs loaded with 50 Ω to VDDO1 for proper operation.
19. Parameter guaranteed by design verification not tested in production.

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3 V ±10%, 2.5 V ±10%, VDDO[2:0] = 3.3 V ± 10%, 2.5 V ± 10%, 1.8 V ± 0.1 V; $V_{DDO} \le V_{DD}$, GND = 0 V, T_A = −40°C to 85°C, Notes 19, 20, 23, 24 and 25)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{out}	Single Ended Output Frequency		0.008		200	MHz
f_{MOD}	Spread Spectrum Modulation Rate	fclkin ≥ 6.75 MHz	30		130	kHz
SS	Percent Spread Spectrum (deviation from nominal frequency)	Down Spread	0		−4	%
		Center Spread	0		±3	%
SSstep	Percent Spread Spectrum Change Step Size	Down Spread Step Size		0.25		%
		Center Spread Step Size		0.125		%
SSC_{RED}	Spectral Reduction, 3rd harmonic	@SS = −0.5%, f_{out} = 100 MHz, fclkin = 25 MHz Crystal, RES BW at 30 kHz, All Output Types		−10		dB
t_{PU}	Stabilization Time from Power−up	V_{DD} = 3.3 V, 2.5 V with Frequency Modulation ON		3.0		ms
t_{PD}	Stabilization Time from Power Down	Time from falling edge on PD pin to Tri−stated Outputs (Asynchronous)		3.0		ms
t_{SEL}	Stabilization Time from Change of Configuration	With Frequency Modulation ON		3.0		ms
t_{OE1}	Output Enable Time	Time from rising edge on OE pin to valid clock outputs (asynchronous)		$2/f_{out}$ (MHz)		μs
t_{OE2}	Output Disable Time	Time from falling edge on OE pin to valid clock outputs (asynchronous)		$2/f_{out}$ (MHz)		μs
Eppm	Synthesis Error	Configuration Dependent		0		ppm

AC ELECTRICAL CHARACTERISTICS (continued)(V_{DD} = 3.3 V ±10%, 2.5 V ±10%, VDDO[2:0] = 3.3 V ± 10%, 2.5 V ± 10%, 1.8 V ± 0.1 V; $V_{DDO} \le V_{DD}$, GND = 0 V, T_A = −40°C to 85°C, Notes 19, 20, 23, 24 and 25)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SINGLE ENDED OUTPUTS (V_{DD} = 3.3 V ±10%, 2.5 V ± 10%, VDDO[2:0] = 3.3 V ± 10%, 2.5 V ± 10%, 1.8 V ± 0.1V; $V_{DDO} \le V_{DD}$, T_A = −40 to 85°C) (Notes 19, 20, 23, 24 and 25)						
$t_{JITTER-3.3\ V}$	Period Jitter Peak−to−Peak	25 MHz xtal input, f_{out} = 100 MHz, SS off, Configuration Dependent (Note 25, see Figure 14)		100		ps
	Cycle−Cycle Jitter	25 MHz xtal input, f_{out} = 100 MHz, SS off, Configuration Dependent (Note 25, see Figure 14)		100		
$t_{JITTER-2.5\ V}$	Period Jitter Peak−to−Peak	25 MHz xtal input, f_{out} = 100 MHz, SS off, Configuration Dependent (Note 25, see Figure 14)		100		ps
	Cycle−Cycle Jitter	25 MHz xtal input, f_{out} = 100 MHz, SS off, Configuration Dependent (Note 25, see Figure 14)		100		
t_r / $t_{f\ 3.3\ V}$	Rise/Fall Time	Measured between 20% to 80% with 15 pF load, f_{out} = 100 MHz, V_{DD} = V_{DDO} = 3.3 V, Max Drive Min Drive		1 2		ns
t_r / $t_{f\ 2.5\ V}$	Rise/Fall Time	Measured between 20% to 80% with 15 pF load, f_{out} = 100 MHz, V_{DD} = V_{DDO} = 2.5 V, Max Drive Min Drive		1 2		ns
t_{DC}	Output Clock Duty Cycle	V_{DD} = 3.3 V, 2.5 V; $V_{DDO} \le V_{DD}$ Duty Cycle of Ref clock is 50% PLL Clock Reference Clock	 45 40	 50 50	 55 60	%
DIFFERENTIAL OUTPUT (CLK1, CLK0) (V_{DD} = 3.3 V ±10%, 2.5 V ± 10%, VDDO[2:0] = 3.3 V ± 10%, 2.5 V ± 10%, 1.8 V ± 0.1V; $V_{DDO} \le V_{DD}$, T_A = −40 to 85°C) (Notes 19, 20, 23, 24 and 25)						
$t_{JITTER-3.3\ V}$	Period Jitter Peak−to−Peak	Configuration Dependent. 25 MHz xtal input, f_{out} = 100 MHz, SS off, CLK2 = OFF (Note 21, 23 and 25, see Figure 14)		100		ps
	Cycle−Cycle Jitter	Configuration Dependent. 25 MHz xtal input, f_{out} = 100 MHz, SS off, CLK2 = OFF (Note 22, 23 and 25, see Figure 14)		100		
$t_{JITTER-2.5\ V}$	Period Jitter Peak−to−Peak	Configuration Dependent. 25 MHz xtal input, f_{out} = 100 MHz, SS off, CLK2 = OFF (Note 22 and 24, see Figure 9)		100		ps
	Cycle−Cycle Jitter	Configuration Dependent. 25 MHz xtal input, f_{out} = 100 MHz, SS off, CLK2 = OFF (Note 22, 23 and 25, see Figure 14)		100		
$t_{r\ 3.3\ V}$	Rise Time	Measured between 20% to 80%, V_{DD} = 3.3 V LVPECL LVDS HCSL CML	175		700	ps
$t_{r\ 2.5\ V}$	Rise Time	Measured between 20% to 80%, V_{DD} = 2.5 V LVPECL LVDS HCSL CML	175		700	ps

AC ELECTRICAL CHARACTERISTICS (continued)(V_{DD} = 3.3 V ±10%, 2.5 V ±10%, VDDO[2:0] = 3.3 V ± 10%, 2.5 V ± 10%, 1.8 V ± 0.1 V; $V_{DDO} \le V_{DD}$, GND = 0 V, T_A = −40°C to 85°C, Notes 19, 20, 23, 24 and 25)

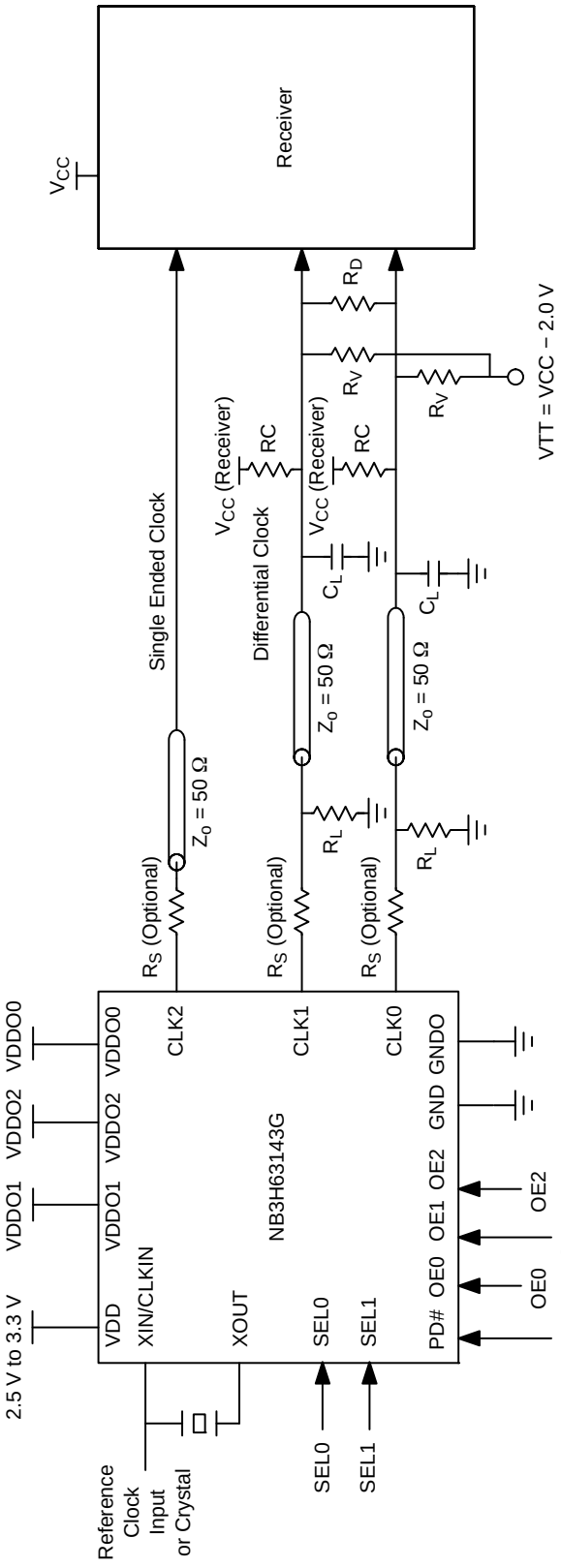
Symbol	Parameter	Condition	Min	Typ	Max	Unit
DIFFERENTIAL OUTPUT (CLK1, CLK0) (V_{DD} = 3.3 V ±10%, 2.5 V ± 10%, VDDO[2:0] = 3.3 V ± 10%, 2.5 V ± 10%, 1.8 V ± 0.1V; $V_{DDO} \le V_{DD}$, T_A = −40 to 85°C) (Notes 19, 20, 23, 24 and 25)						
$t_{f\ 3.3\ V}$	Fall Time	Measured between 20% to 80% with 2 pF load, V_{DD} = 3.3 V LVPECL LVDS HCSL CML	175		700	ps
$t_{f\ 2.5\ V}$	Fall Time	Measured between 20% to 80% with 2 pF load, V_{DD} = 2.5 V LVPECL LVDS HCSL CML	175		700	ps
t_{DC}	Output Clock Duty Cycle	V_{DD} = 3.3 V, 2.5 V; Duty Cycle of Ref clock is 50% PLL Clock Reference Clock	 45 40	 50 50	 55 60	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

20. Measurement taken from single ended clock terminated with test load capacitance of 5 pF and 15 pF and differential clock terminated with test load of 2 pF. See Figures 6, 7 and 12.
21. Measurement taken from single ended waveform.
22. Measurement taken from differential waveform.
23. AC performance parameters like jitter change based on the output frequency, spread selection, power supply and loading conditions of the output. For application specific AC performance parameters, please contact ON Semiconductor.
24. Measured at f_{out} = 100 MHz, No Frequency Modulation, f_{clkin} = 25 MHz fundamental mode crystal and output termination as described in Parameter Measurement Test Circuits
25. Period jitter Sampled with 10000 cycles, Cycle−cycle jitter sampled with 1000 cycles. Jitter measurement may vary. Actual jitter is dependent on Input jitter and edge rate, number of active outputs, inputs and output frequencies, supply voltage, temperature, and output load.

SCHEMATIC FOR OUTPUT TERMINATION



Differential Clock Termination							
Signaling Type	R_S	R_D	R_L	C_L	RC	R_V
LVCMOS	Optional	Open	Open	Open	Open	Open
LVPECL	Optional	Open	Open	Open	Open	50
LVDS	Optional	100	Open	Open	Open	Open
HCSL	Optional	Open	50	2 pF	Open	Open
CML	Optional	Open	Open	Open	50	Open

26. Receiver VCC must be at same supply potential as VDDO1 for differential clock outputs.
27. All resistor values are in ohms.
28. VDDO [2:0] <= VDD always

	Single Ended Signal		Differential Signal	
	MIN	MAX	MIN	MAX
VDD	2.5 V	3.3 V	2.5 V	3.3 V
VDDO2	1.8 V	VDD	–	–
VDDO1	1.8 V	VDD	2.5 V (LVPECL/CML) 1.8 V (LVDS/HCSL)	VDD
VDDO0	1.8 V	VDD	–	–

Figure 6. Typical Termination for Single Ended and Differential Signaling Device Load

PARAMETER MEASUREMENT TEST CIRCUITS

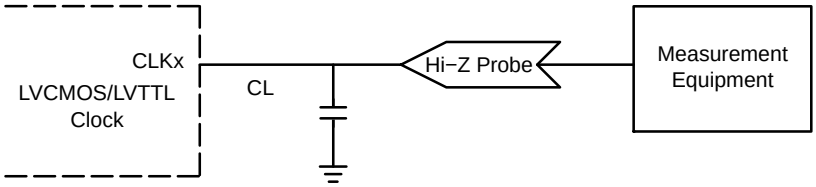


Figure 7. LVCMOS/LVTTL Parameter Measurement

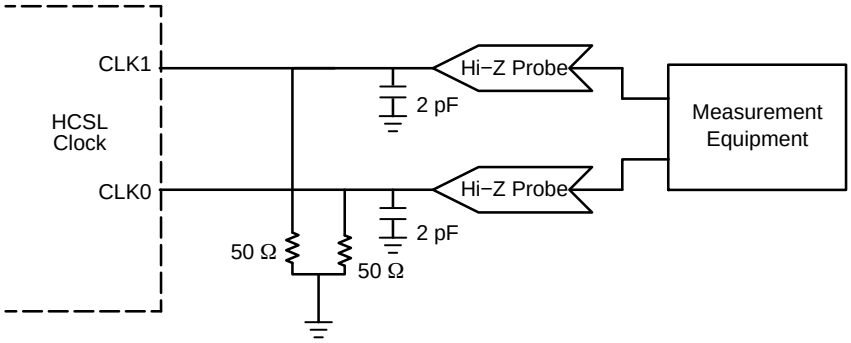


Figure 8. HCSL Parameter Measurement

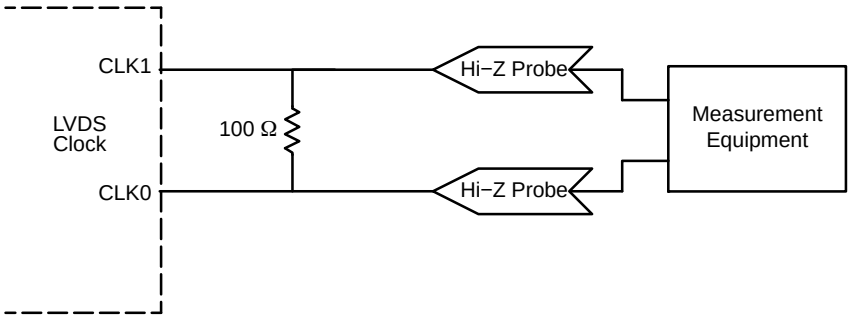


Figure 9. LVDS Parameter Measurement

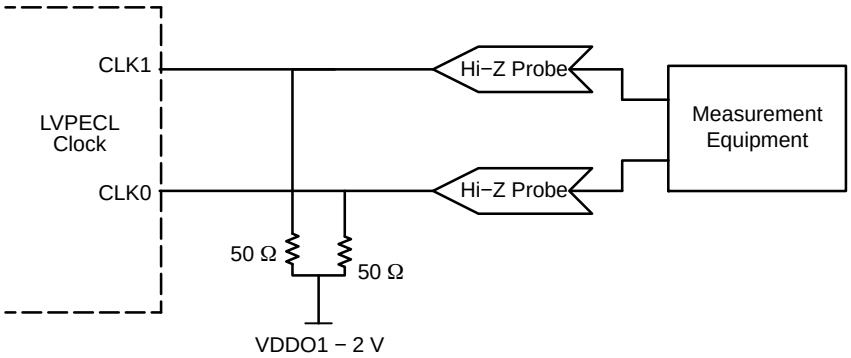


Figure 10. LVPECL Parameter Measurement

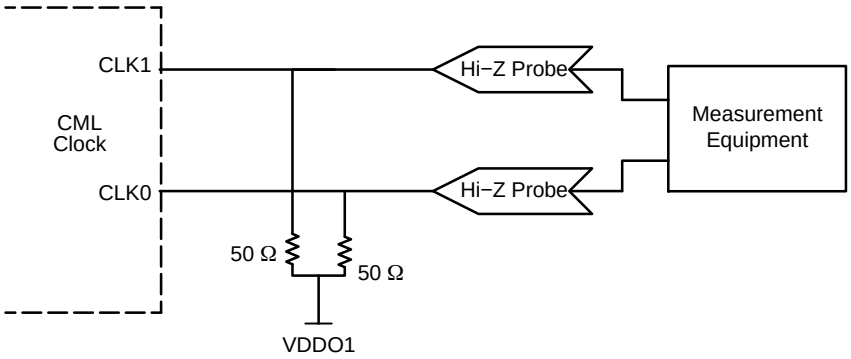


Figure 11. CML Parameter Measurement

TIMING MEASUREMENT DEFINITIONS

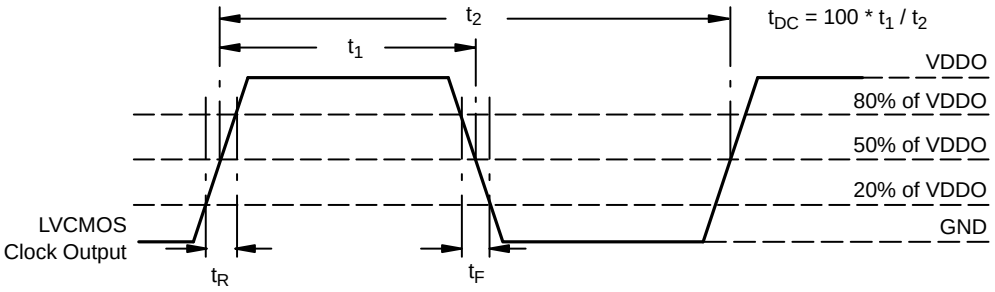


Figure 12. LVCMOS Measurement for AC Parameters

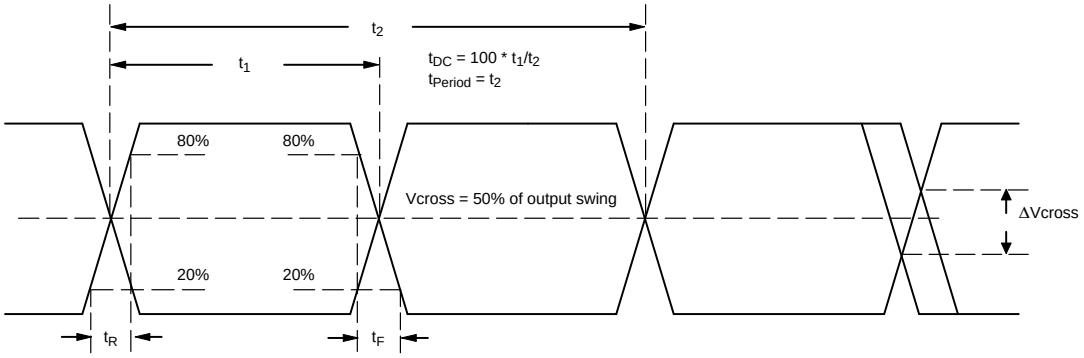


Figure 13. Differential Measurement for AC Parameters

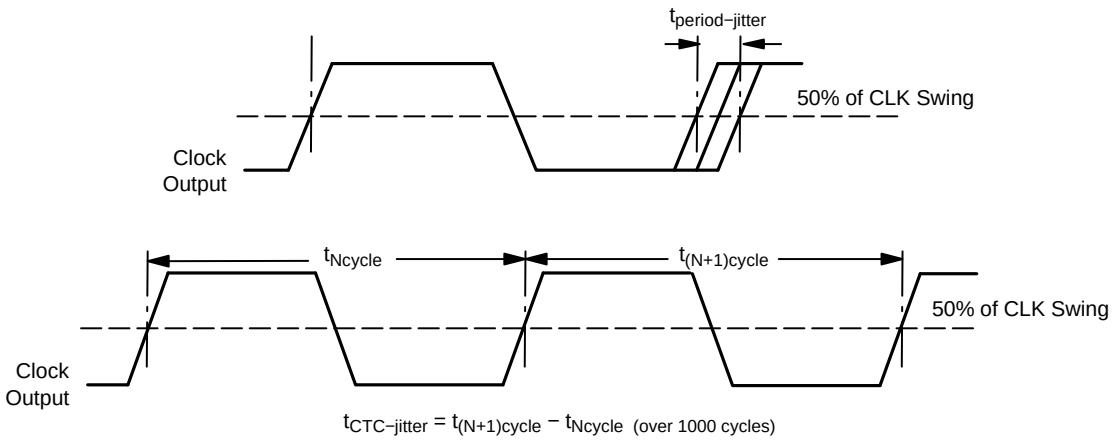


Figure 14. Period and Cycle−Cycle Jitter Measurement

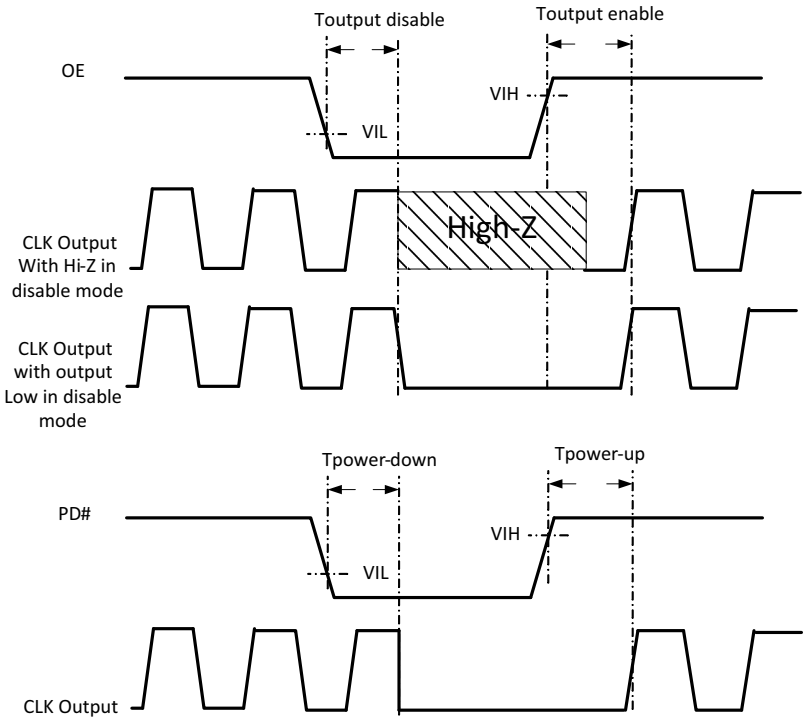


Figure 15. Output Enable/ Disable and Power Down Functions

APPLICATION GUIDELINES

Crystal Input Interface

Figure 16 shows the NB3H63143G device crystal oscillator interface using a typical parallel resonant fundamental mode crystal. A parallel crystal with loading capacitance CL = 18 pF would use C1 = 32 pF and C2 = 32 pF as nominal values, assuming 4 pF of stray capacitance per line.

$$C_L = (C1 + Cstray)/2;\ C1 = C2$$

The frequency accuracy and duty cycle skew can be fine−tuned by adjusting the C1 and C2 values. For example, increasing the C1 and C2 values will reduce the operational frequency. Note R1 is optional and may be 0 Ω.

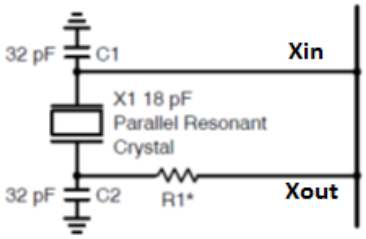


Figure 16. Crystal Interface Loading

Output Interface and Terminations

The NB3H63143G consists of a unique Multi Standard Output Driver to support LVCMOS/LVTTL, LVPECL, LVDS, HCSL and CML standards. Termination techniques required for each of these standards are different to ensure proper functionality. From the device it is possible to switch off one output driver and turn on another output driver using the SEL[1:0] pins as part of the Configuration Settings. The required termination changes must be considered and taken care of by the system designer.

LVCMOS/LVTTL Interface

LVCMOS/LVTTL output swings rail−to−rail up to VDDO supply (minimum 1.8 V) and can drive up to 15 pF load at higher drive stengths. The output buffer's drive is programmable up to four steps, though the drive current will depend on the step setting as well as the VDDO supply voltage. (See Figure 17 and Table 8). Drive strength must be configured high for driving higher loads. The slew rate of the clock signal increases with higher output current drive for the same load. The software lets the user choose the load drive current value per LVCMOS/LVTTL output based on the VDDO supply selected.

Table 8. LVCMOS/LVTTL DRIVE LEVEL SETTINGS

VDDO Supply	Load Current Setting 3 Max Load Current	Load Current Setting 2	Load Current Setting 1	Load Current Setting 0 Min Load Current
3.3 V	16 mA	12 mA	8 mA	4 mA
2.5 V	12 mA	8 mA	4 mA	2 mA
1.8 V	8 mA	4 mA	2 mA	1 mA

The IDDO current consists of the static current component (varies with drive) and dynamic current component. For any VDDO, the IDDO dynamic current range per LVCMOS output can be approximated by the following:

$$IDDO = f_{out} * C_{load} * VDDO$$

C_{load} includes the load capacitor connected to the output, the pin capacitor posed by the output pin (typically 5 pF) and the cap load posed by the receiver input pin. C_{load} = (CL + C_{pin}+ C_{in})

An optional series resistor Rs can be connected at the output for impedance matching, to limit the overshoots and ringings.

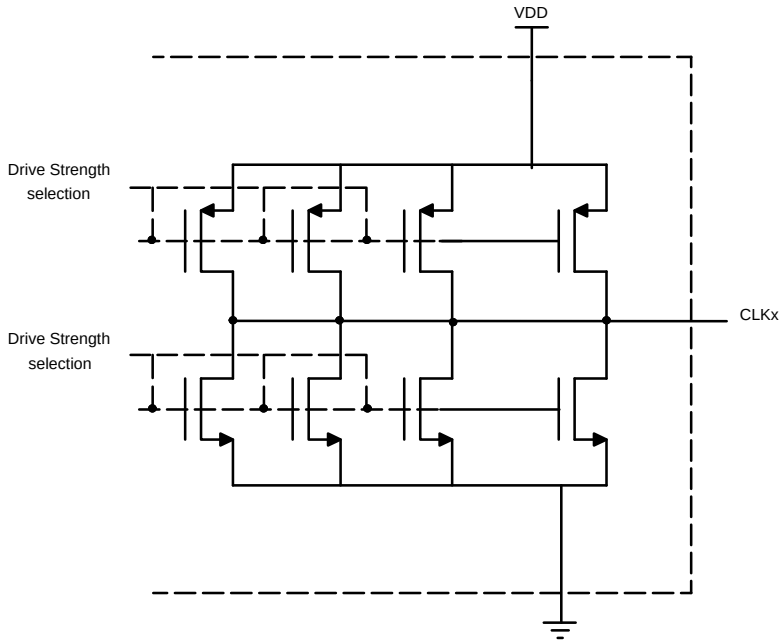


Figure 17. Simplified LVCMOS Output Structure

LVDS Interface

Differential signaling like LVDS has inherent advantage of common mode noise rejection and low noise emission, and thus a popular choice for clock distribution in systems. TIA/EIA−644 or LVDS is a standard differential, point−to−point bus topology that supports fast switching speeds and has the benefit of low power consumption. The driver consists of a low swing differential with constant current of 3.5 mA through the differential pair, and generates switching output voltage across a 100 Ω terminating resistor (externally connected or internal to the receiver). Power dissipation in LVDS standard ($(3.5\ mA)^2$ x 100 Ω = 1.2 mW) is thus much lower than other differential signalling standards.

A fan−out LVDS buffer (like ON Semiconductor's NB6N1xS and NB6L1xS) can be used as an extension to provide clock signal to multiple LVDS receivers to drive multiple point−to−point links to receiving node.

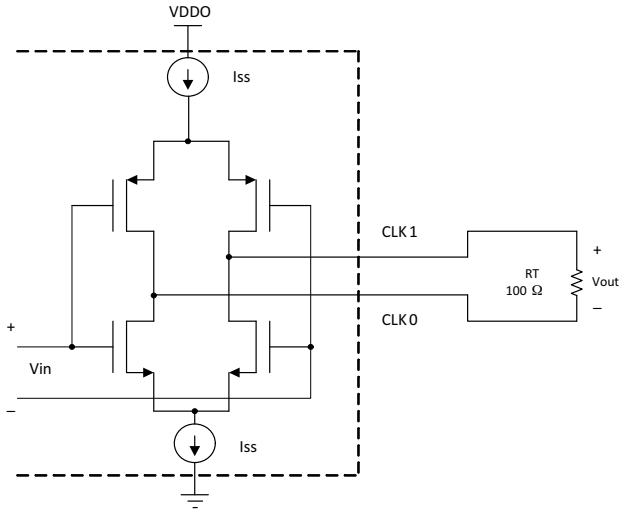


Figure 18. Simplified LVDS Output Structure with Termination

LVPECL Interface

The LVPECL driver is designed to drive a 50 Ω transmission line from a constant current differential and a low impedance emitter follower. On the NB3H63143G, this differential standard is supported for VDDO supply voltage of 2.5 V and above. In the system, the clock receiver must be referenced at the same supply voltage as VDDO for reliable functionality. The termination to receiver V_{CC} − 2 V (1.3 V for a 3.3 V VDDO supply, and 0.5 V for a 2.5 V VDDO supply) used in evaluation boards, is rarely used in system boards as it adds another power supply on the system board. Thus, Thevenin's equivalent circuit (Figure 20) for this termination or a Y−type termination (Figure 21) is often used in systems. Termination techniques for LVPECL are detailed in the application note "Termination of ECL Devices with EF (Emitter Follower) OUTPUT Structure − AND8020".

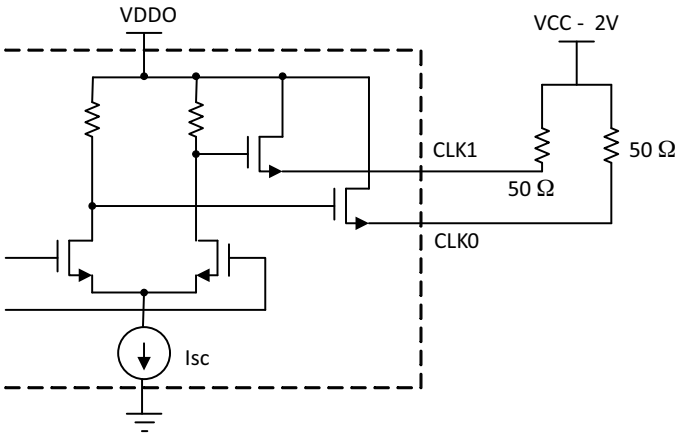


Figure 19. Simplified LVPECL Output Structure with Termination

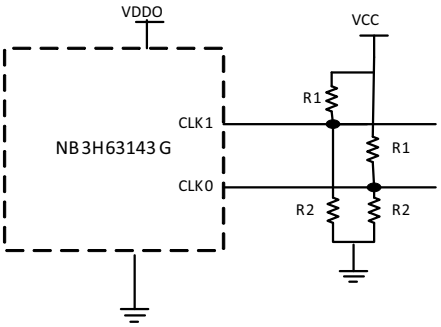


Figure 20. LVPECL Thevenin Termination

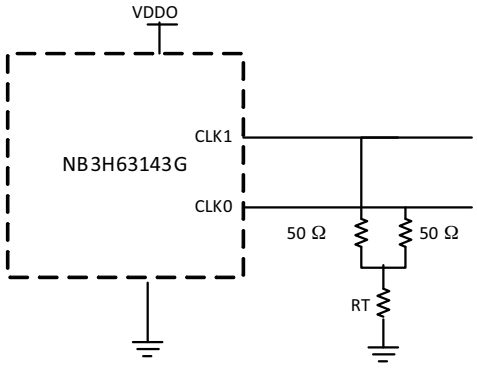


Figure 21. LVPECL Y−Termaination

System Supply	Practical R2 (Ω)	Practical R1 (Ω)
2.5 V System	62(5%)	240(5%)
3.3 V system	82(5%)	130(5%)

Y−Termination	RT (Ω)
2.5 V System	50
3.3 V system	18

The termination should be placed as close to the receiver as possible to avoid unterminated stubs that can cause signal integrity issues.

CML Interface

A CML driver consists of an NMOS open drain constant current differential driving 16 mA current into a 50 Ω load terminated to the supply voltage at the receiver. This termination resistor can be external or internal to the receiver and needs to be as close as possible to the receiver. On the NB3H63143G, this differential standard is supported for VDDO supply voltage 2.5 V and above. The termination techniques used for a CML driver are detailed in application note "Termination and Interface of ON Semiconductor ECL Devices With CML (Current Mode Logic) OUTPUT Structure − AND8173"

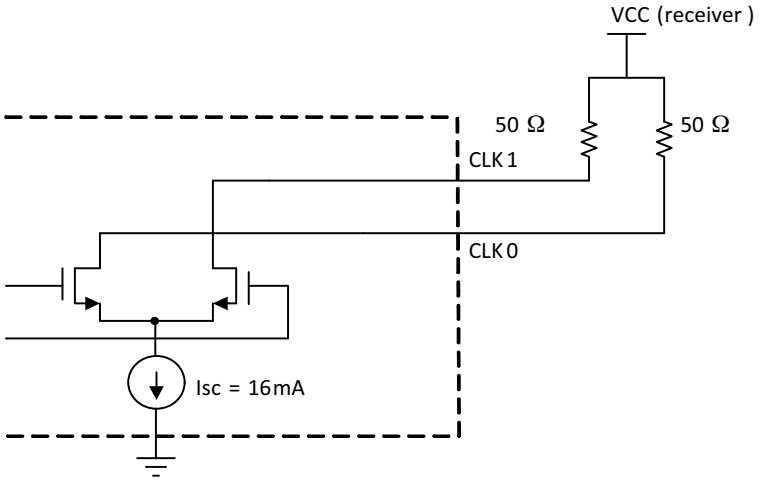


Figure 22. Simplified CML Output Structure with Termination

HCSL Termination

HCSL is a differential signaling standard commonly used in PCIe systems. The HCSL driver is typical 14.5 mA switched current open source output that needs a 50 Ω termination resistor to ground near the source, and generates 725 mV of signal swing. A series resistor (10 Ω to 33 Ω) is optionally used to achieve impedance matching by limiting overshoot and ringing due to the rapid rise of current from the output driver. The open source driver has high internal impedance; thus a series resistor up to 33 Ω does not affect the signal integrity. This resistor can be avoided for low VDDO supply (1.8 V) of operation, unless impedance matching requires it.

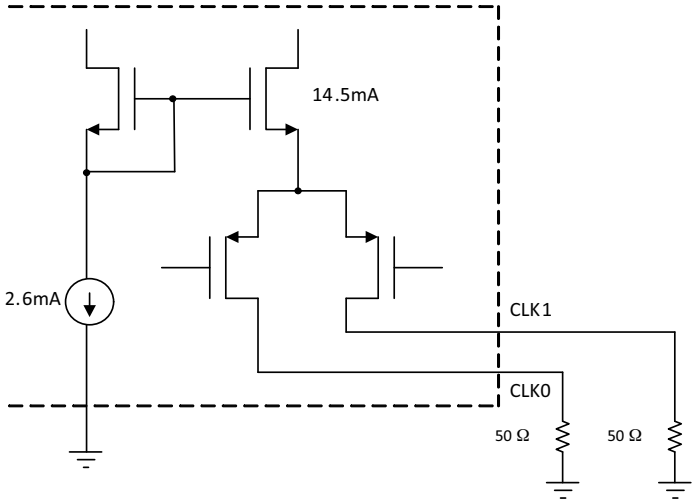


Figure 23. Simplified HCSL Output Structure with Termination

Field Programming Kit and Software

The NB3H63143G can be programmed by the user using the ‘Clock Cruiser Programmable Clock Kit’. This device uses the 16L daughter card on the hardware kit. To design a new clock, ‘Clock Cruiser Software’ is required to be installed from the ON Semiconductor website. The user manuals for the hardware kit Clock Cruiser Programmable Clock Kit and Clock Cruiser Software can be found following this link www.onsemi.com.

Recommendation for Clock Performance

Clock performance is specified in terms of Jitter in the time domain. Details and measurement techniques of Cycle−cycle jitter, period jitter, TIE jitter and Phase Noise are explained in application note AND8459/D.

In order to have a good clock signal integrity for minimum data errors, it is necessary to reduce the signal reflections. The reflection coefficient can be zero only when the source impedance equals the load impedance. Reflections are based on signal transition time (slew rate) and due to impedance mismatch. Impedance matching with proper termination is required to reduce the signal reflections. The amplitude of overshoots is due to the difference in impedance and can be minimized by adding a series resistor (Rs) near the output pin. Greater the difference in impedance, greater is the

amplitude of the overshoots and subsequent ripples. The ripple frequency is dependant on the signal travel time from the receiver to the source. Shorter traces results in higher ripple frequency, as the trace gets longer the travel time increases, reducing the ripple frequency. The ripple frequency is independent of signal frequency, and only depends on the trace length and the propogation delay. For eg. On an FR4 PCB with approximately 150 ps/inch of propogation rate on a 2 inch trace, the ripple frequency = 1 / (150 ps * 2 inch * 5) = 666.6 MHz; [5 = number of times the signal travels, 1 trip to receiver plus 2 additional round trips].

PCB traces should be terminated when trace length >= tr/f / (2* tprate); tf/t = rise/ fall time of signal, tprate = propagation rate of trace.

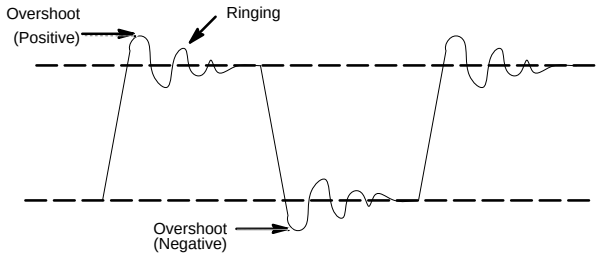


Figure 24. Signal Reflection Components

PCB Design Recommendation

For a clean clock signal waveform it is necessary to have a clean power supply for the device. The device must be isolated from system power supply noise. A 0.1 μF and a 2.2 μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin and the ground via should be kept as thick and as short as possible. All the VDD pins should have decoupling capacitors.

Stacked power and ground planes on the PCB should be large. Signal traces should be on the top layer with minimum vias and discontinuities and should not cross the reference planes. The termination components must be placed near the source or the receiver. In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

Device Applications

The NB3H63143G is targeted mainly for the Consumer market segment and can be used as per the examples below.

Clock Generator

Consumer applications like a Set top Box, have multiple sub−systems and standard interfaces and require multiple reference clock sources at various locations in the system. This part can function as a clock generating IC for such applications generating a reference clock for interfaces like USB, Ethernet, Audio/Video, ADSL, PCI etc.

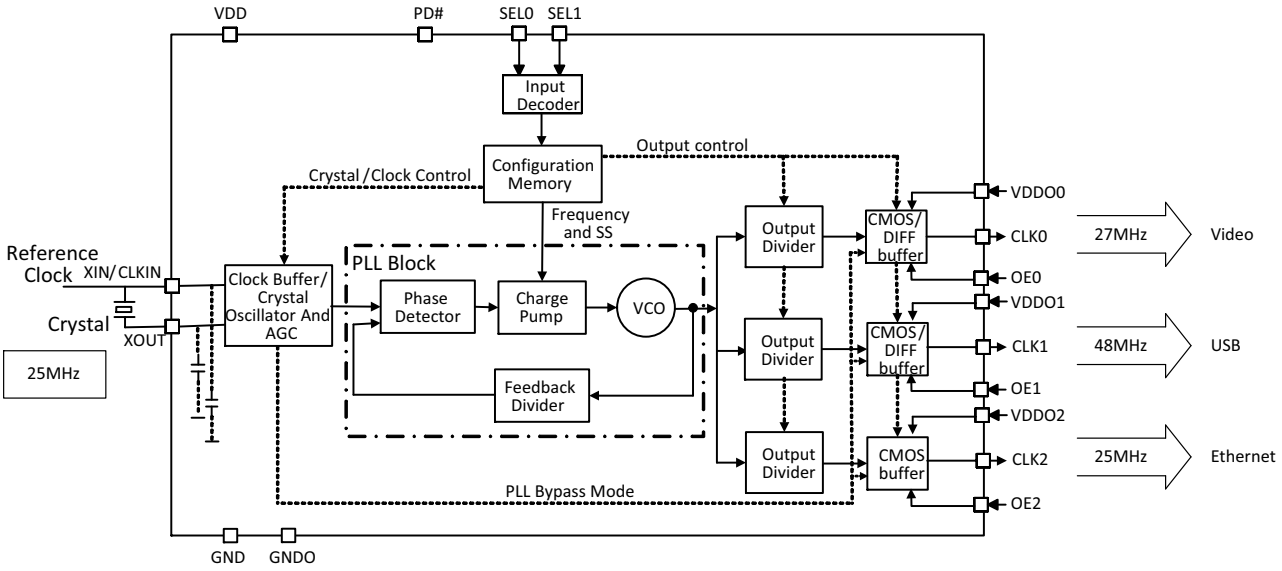


Figure 25. Application as Clock Generator

Buffer and Logic/Level Translator

The NB3H63143G is useful as a simple CMOS Buffer in PLL bypass mode. One or more outputs can use the PLL Bypass mode to generate the buffered outputs. If the PLL is configured to use spread spectrum, all outputs using PLL Bypass feature will not be subjected to the spread spectrum. The device can be simultaneously used as logic translator for converting the LVCMOS input clock to LVPECL, LVDS, HCSL, CML, or LVCMOS (with different output voltage level).

For instance in applications like an LCD monitor, for converting the LVCMOS input clock to LVDS output.

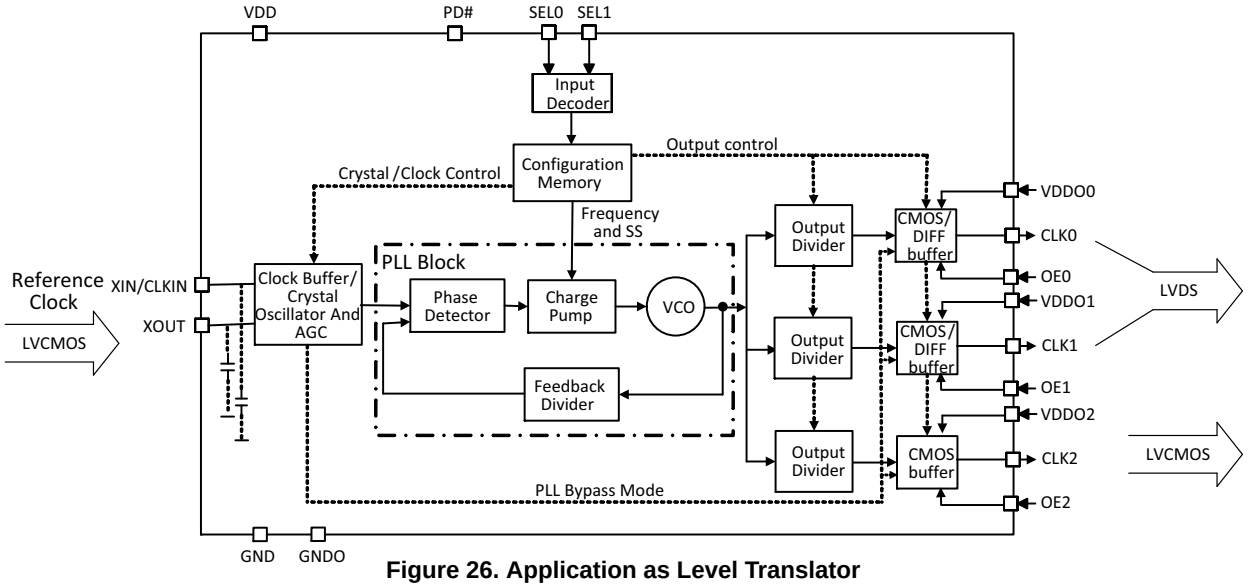


Figure 26. Application as Level Translator

NOTE: Since the device requirement is VDDO ≤ VDD, LVCMOS signal level cannot be translated to a higher level of LVCMOS voltage.

EMI Attenuator

Spread spectrum through frequency modulation technique enables the reduction of EMI radiated from the high frequency clock signals by spreading the spectral energy to the nearby frequencies. While using frequency modulation, the same selection is applied to all the PLL clock outputs (not bypass outputs) even if they are at different frequencies. In Figure 27, CLK0 uses the PLL and hence is subjected to the spread spectrum modulation while CLK1 and CLK2 use the PLL Bypass mode and hence are not subjected to the spread spectrum modulation.

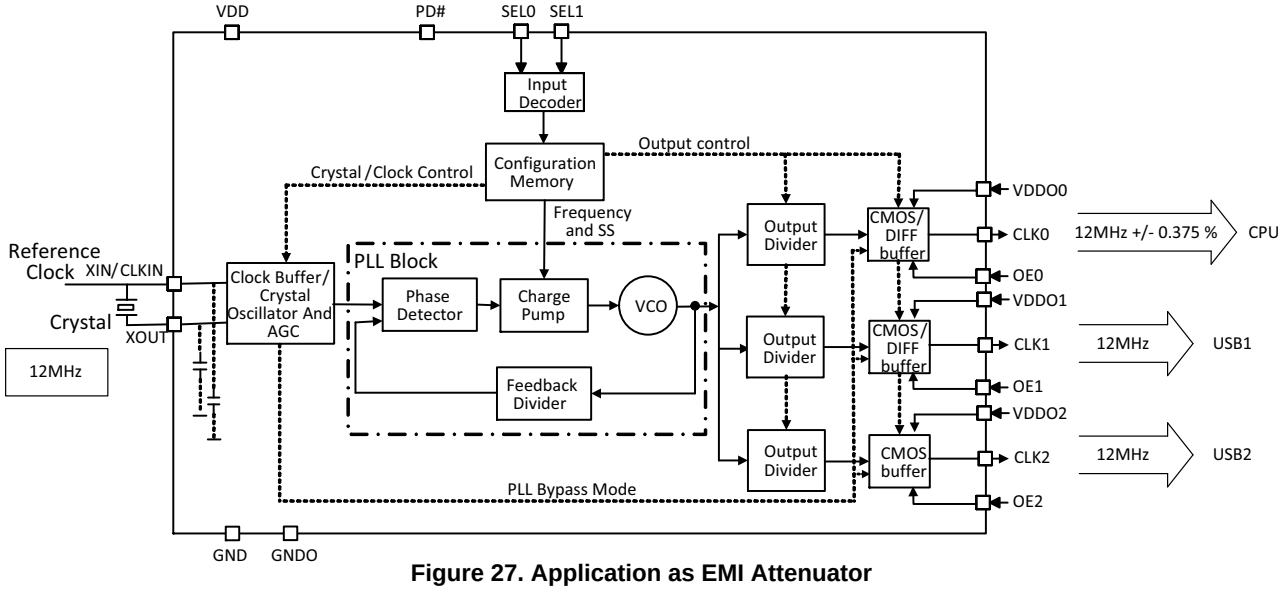


Figure 27. Application as EMI Attenuator

ORDERING INFORMATION

Device	Case	Package	Type	Shipping†
NB3H63143G00MNR2G	485AE	QFN−16 (Pb−Free)	Blank Device	3000 / Tape & Reel
NB3H63143GxxMNR2G	485AE	QFN−16 (Pb−Free)	Factory Pre−programmed Device	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

†Note: Please contact your ON Semiconductor sales representative for availability in tube.

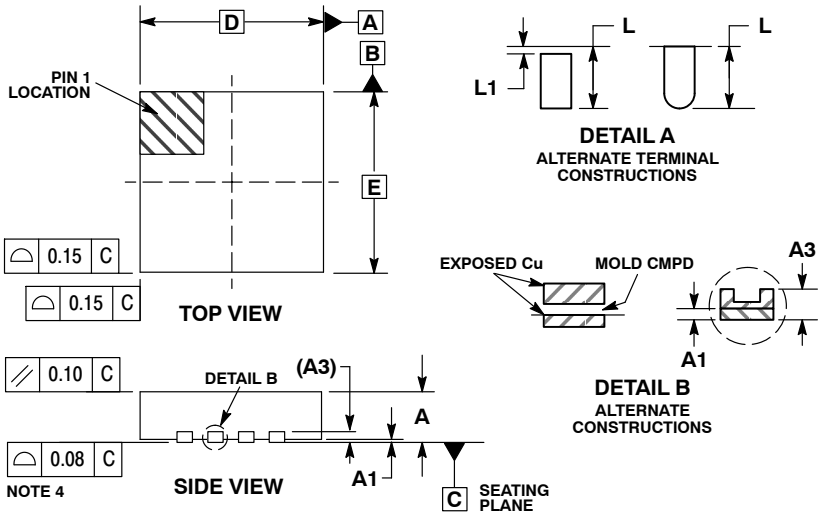
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

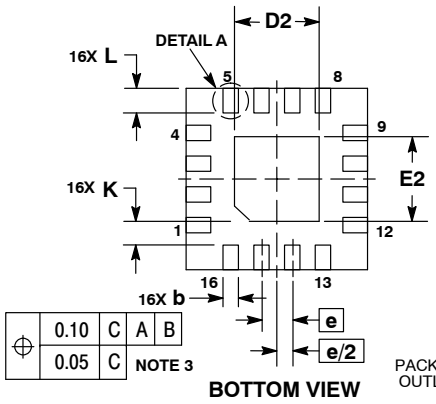
ON Semiconductor®

QFN16 3x3, 0.5P
CASE 485AE
ISSUE C

DATE 24 JUN 2016

1
SCALE 2:1

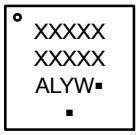




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. OUTLINE MEETS JEDEC DIMENSIONS PER MO−220, VARIATION VEED−6.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.25	1.55
E	3.00 BSC	
E2	1.25	1.55
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.15

GENERIC MARKING DIAGRAM*

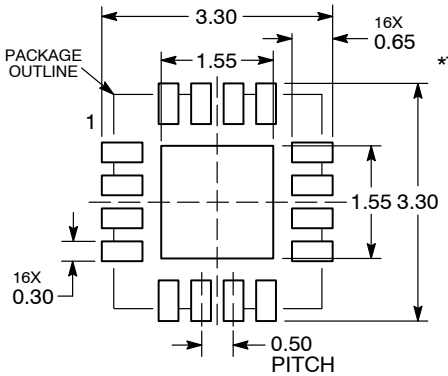


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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