NB4N840MMNEVB

Evaluation Board User's Manual for NB4N840M

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EVAL BOARD USER'S MANUAL

Description

The NB4N840M Evaluation Board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the performance and operation of the NB4N840M dual 2 x 2 Crosspoint Switch. This user's manual provides detailed information on the board's contents, layout and use. The manual should be used in conjunction with the NB4N840M data sheet which contains full technical details on device specifications and operation.

The NB4N840M is a high−bandwidth fully differential dual 2 x 2 crosspoint switch with CML inputs/outputs that is suitable for applications such as SDH/SONET DWDM and high speed switching. Fully differential design techniques are used to minimize jitter accumulation, crosstalk, and signal skew, which make this device ideal for loop−through and protection channel switching applications. Each 2 x 2 crosspoint switch can fan−out and/or multiplex up to 3.2 Gb/s data and 2.7 GHz clock signals.

Internally terminated differential CML inputs accept AC−coupled LVPECL (Positive ECL) or direct coupled CML signals. By providing internal 50 Ω input and output termination resistor, the need for external components is eliminated and interface reflections are minimized. Differential 16 mA CML outputs provide matching internal 50 Ω terminations, and 400 mV output swings when externally terminated, 50 Ω to V_{CC}.

Single−ended LVCMOS/LVTTL SEL inputs control the routing of the signals through the crosspoint switch which makes this device configurable as 1:2 fan−out, repeater or 2 x 2 crosspoint switch. The device is housed in a low profile 5 x 5 mm 32−pin QFN package.

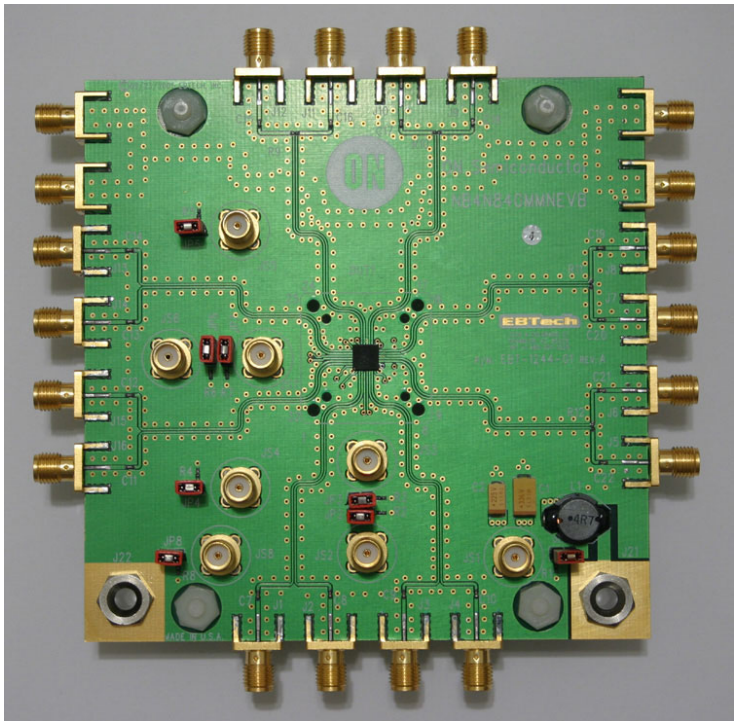

Figure 1. NB4N840M Evaluation Board

Board Features

- Fully assembled evaluation board
- Accommodates the electrical characterization of the NB4N840M in the QFN32 package
- Equal length input and output data lines to minimize skew
- Selectable jumpers
- Single + 3.3 V supply

This Evaluation Board Manual Contains

- Information on the NB4N840M Evaluation Board
- Appropriate Lab Setup Details
- Evaluation Board Layout
- Bill of Materials

Setup for Measurements

Step 1: Basic Equipment

- Signal Generator
- Oscilloscope
- Power Supply
- Voltmeter
- Matched High−Speed Cables with SMA Connectors

Step 2: Power Supply Connections

+ 3.3 V must be provided to the board for V_{CC}.

Table 1. Power Supply Connections

Supply	Value	Connector
V_{CC}	+ 3.3 V	J21
GND	0 V	J22

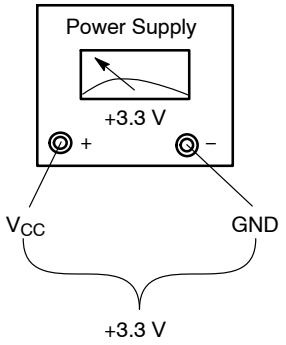

Figure 2. Power Supply Connections

Step 3: Input Connections

DAn and DBn require CML drive levels and provide internal 50 Ω to V_{CC} termination resistors to eliminate external components and minimize reflections. Ensure that the CML devices driving these inputs are not redundantly terminated.

Table 2. Input Connectors

Inputs	Board Connector
DA0	J13
$\overline{DA0}$	J14
DA1	J15
$\overline{DA1}$	J16
DB0	J3
$\overline{DB0}$	J4
DB1	J1
$\overline{DB1}$	J2

Step 4: Control and Select Pins

Jumpers JP1, JP2, JP5, and JP6 select the input signals for channel A and B outputs. Jumpers JP3, JP4, JP7, and JP8 enable the output drivers for channel A and B (refer to Table 3 for output routing).

Table 3. Output Routing

ROUTING CONTROLS		OUTPUT CONTROLS		OUTPUT SIGNALS	
SELA0 / **SELB0** JP6 / JP2	**SELA1** / **SELB1** JP5 / JP1	**ENA0** / **ENA1** JP7 / JP8	**ENB0** / **ENB1** JP3 / JP4	**Signal at QA0** / **QB0**	**Signal at QA1** / **QB1**
L	L	H	H	DA0 / DB0	DA0 / DB0
L	H	H	H	DA0 / DB0	DA1 / DB1
H	L	H	H	DA1 / DB1	DA0 / DB0
H	H	H	H	DA1 / DB1	DA1 / DB1
X	X	L	L	Power Down	Power Down

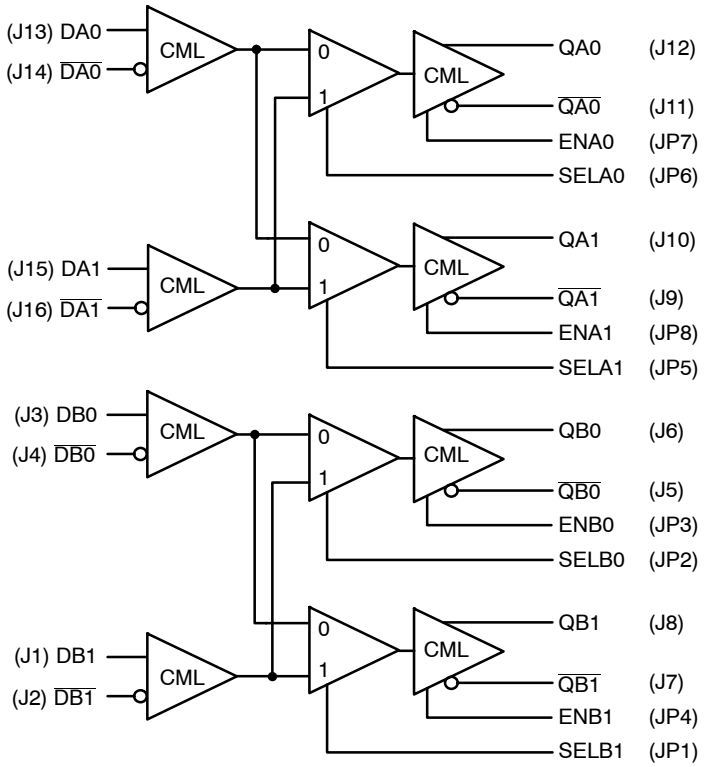

Figure 3. NB4N840M Evaluation Board Connector Configuration

Step 5: Output Connections

The CML outputs, QAn and QBn, must be AC−coupled to a 50 Ω termination (100 Ω differential) load. On−board 100−Ω differential terminations are provided to reduce noise on outputs that are not used. Connect the QAn/QBn CML outputs to the oscilloscope with equally matched cables.

1. Monitoring One or More CML Outputs with 50 Ω Oscilloscope Inputs

a. Leave the coupling capacitors in series with the outputs.

b. Remove the associated 100 Ω differential load resistors from the evaluation board on the outputs (R9–R12).

c. It is important to remove the 100 Ω resistor on the output monitored, otherwise the load impedance will not match the characteristic impedance of the line and the resulting reflections will cause a degradation in the output signal quality.

d. If you are observing a single−ended output, balance the other half with a 50 Ω termination to ground (through the AC−coupling capacitor).

2. Monitoring CML Outputs with High−Impedance Oscilloscope Inputs

a. Leave the coupling capacitors in series with the outputs.

b. Make sure the differential load resistors are on all the outputs (R9–R12).

Table 4. Output Connectors

Outputs	Board Connector
QA0	J12
$\overline{\text{QA0}}$	J11
QA1	J10
$\overline{\text{QA1}}$	J9
QB0	J6
$\overline{\text{QB0}}$	J5
QB1	J8
$\overline{\text{QB1}}$	J7

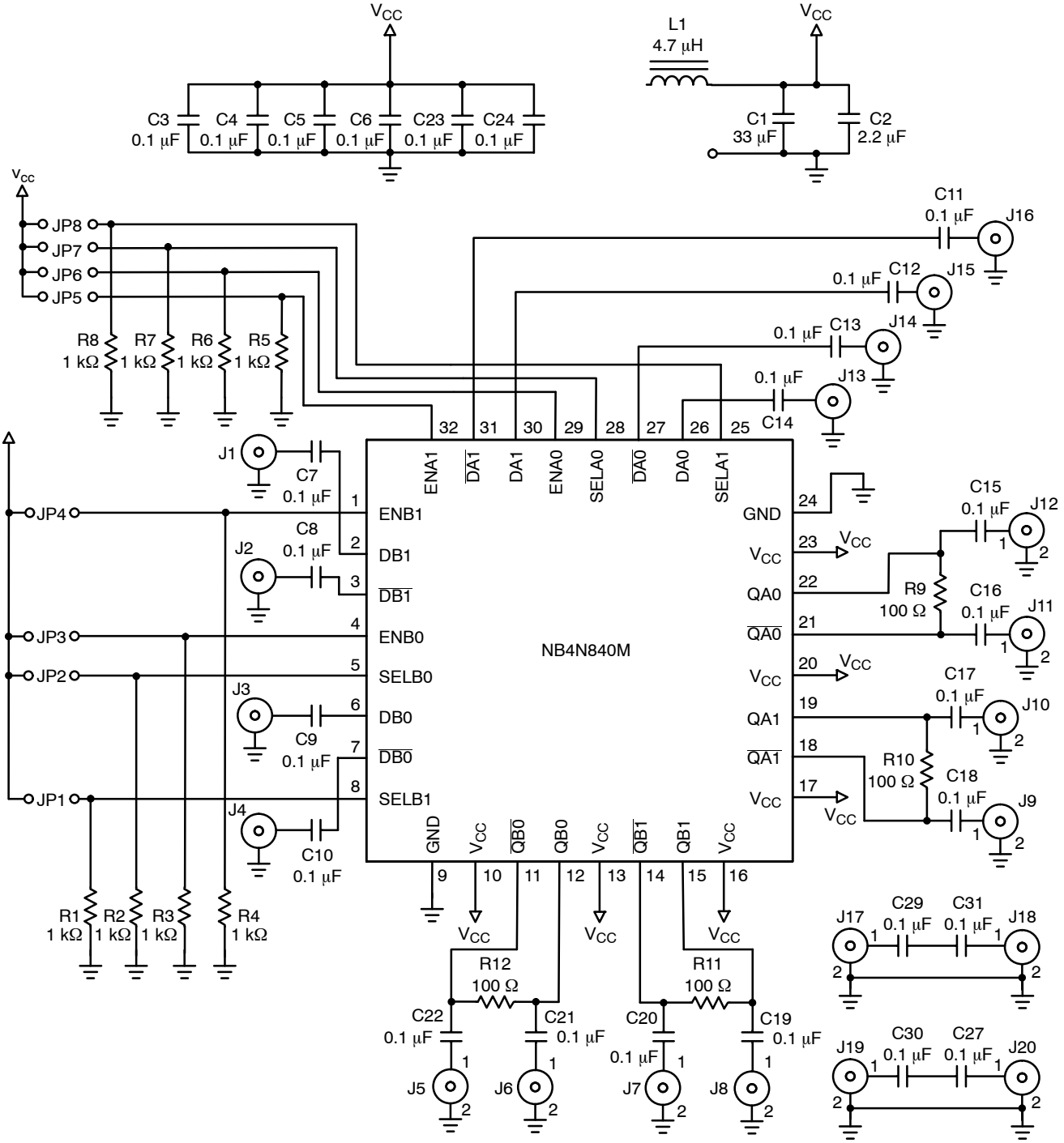

Figure 4. Evaluation Board Schematic

Table 5. BILL OF MATERIALS

Ref. Number	Qty	Description	Manufacturer	Manufacturer Part No. (Notes 1, 2)
R1 – R8	8	1 kΩ ±1%, 0402, Resistors	Multicomp	MC0402WGF1001TCE−TR
R9 – R12	4	100 Ω ±1%, 0402, Resistors	Multicomp	MC0402WGF1000TCE−TR
C1	1	33 μF ±10%, size “D”, Tantalum Capacitor	Kemet	T491D336K016AT
C2	1	2.2 μF ±10%, size “C”, Tantalum Capacitor	Kemet	T491C225K035AT
C3 – C24, C27, C29 – C31	26	0.1 μF ±10%, 0402, Ceramic Capacitors	Kemet	C0402C104K4RAC−TU
L1	1	4.7 μH Inductor	Coilcraft	DT3316P−472MLB
U1	1	32 pin QFN	ON Semiconductor	NB4N840MMNG
J1 – J20	20	SMA Edge Mount Connectors	Johnson	142−0701−851
JS1 – JS8	8	SMA Connectors	Johnson	142−0701−201
J21, J22	2	Test Point Jacks		
JP1 – JP8	8	1x2 Pin Headers, (0.1 inch pitch)	SPC	SPC20485
JP1 – JP8	8	Shunts	SPC	SPC19809

1. Specified parts are RoHS−compliant.
2. Only RoHS−compliant equivalent parts may be substituted.

Board Lay−Up

This board is implemented in four layers and provides a high bandwidth 50 Ω controlled impedance environment. The pictures in Figures 5 through 9 show views of the four layers of the evaluation board. Board material is FR4.

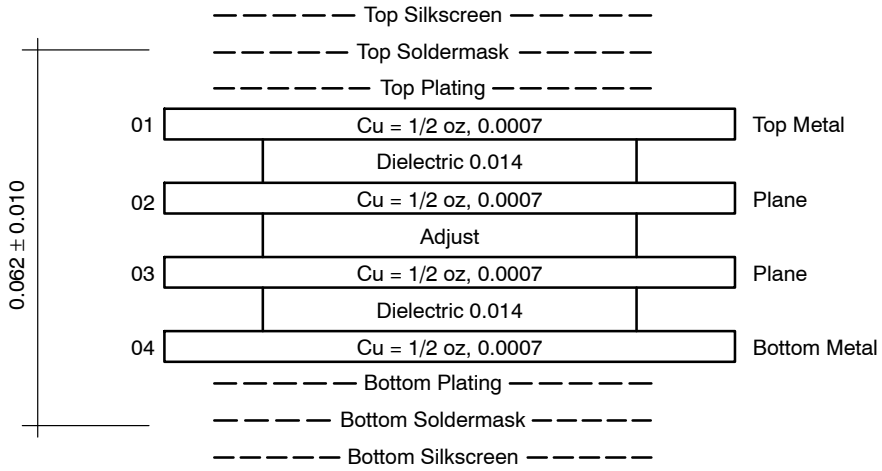

Figure 5. Evaluation Board Lay−Up

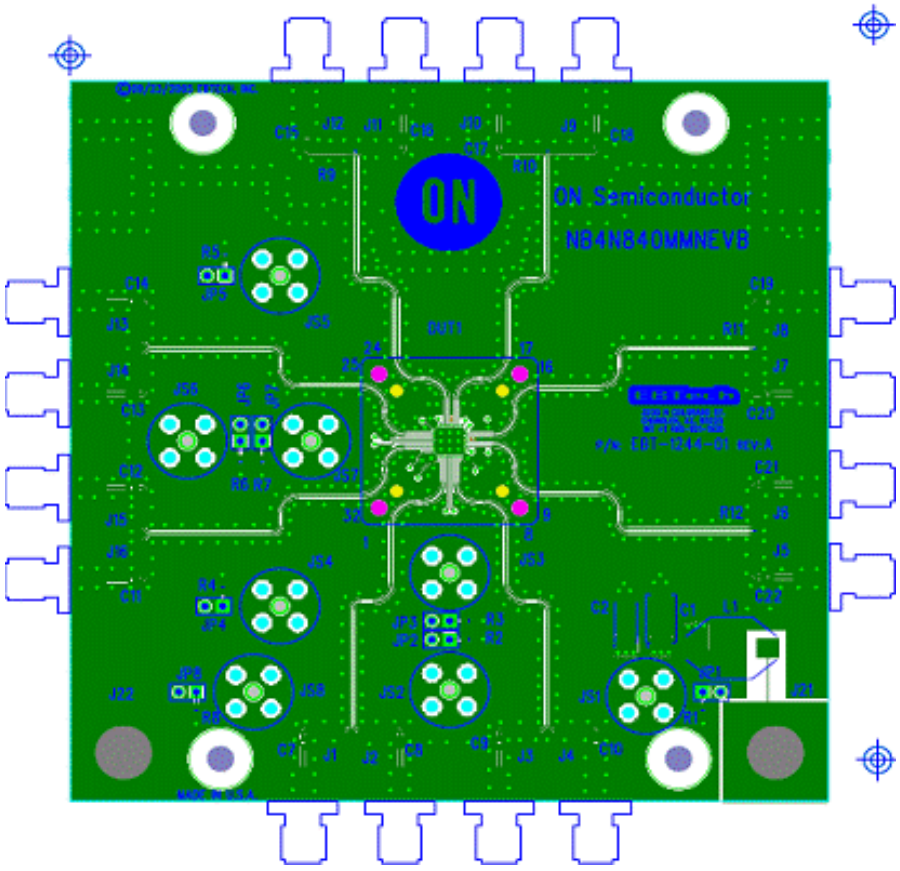

Figure 6. NB4N840MMN Evaluation Board Top (Component) Layer

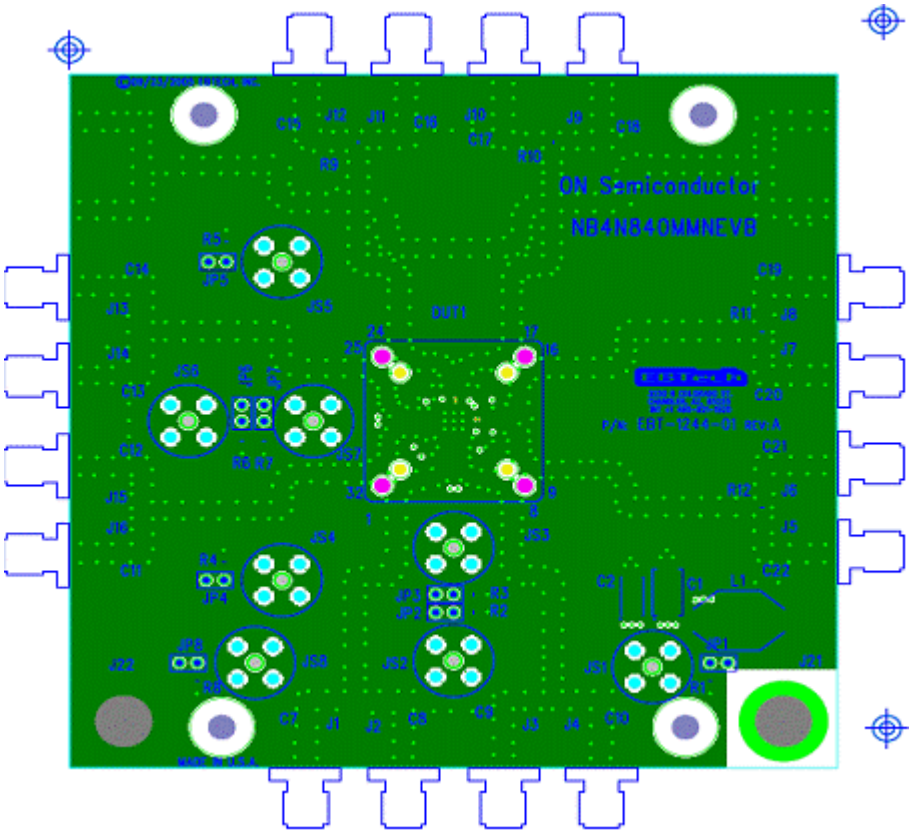

Figure 7. Ground Layer

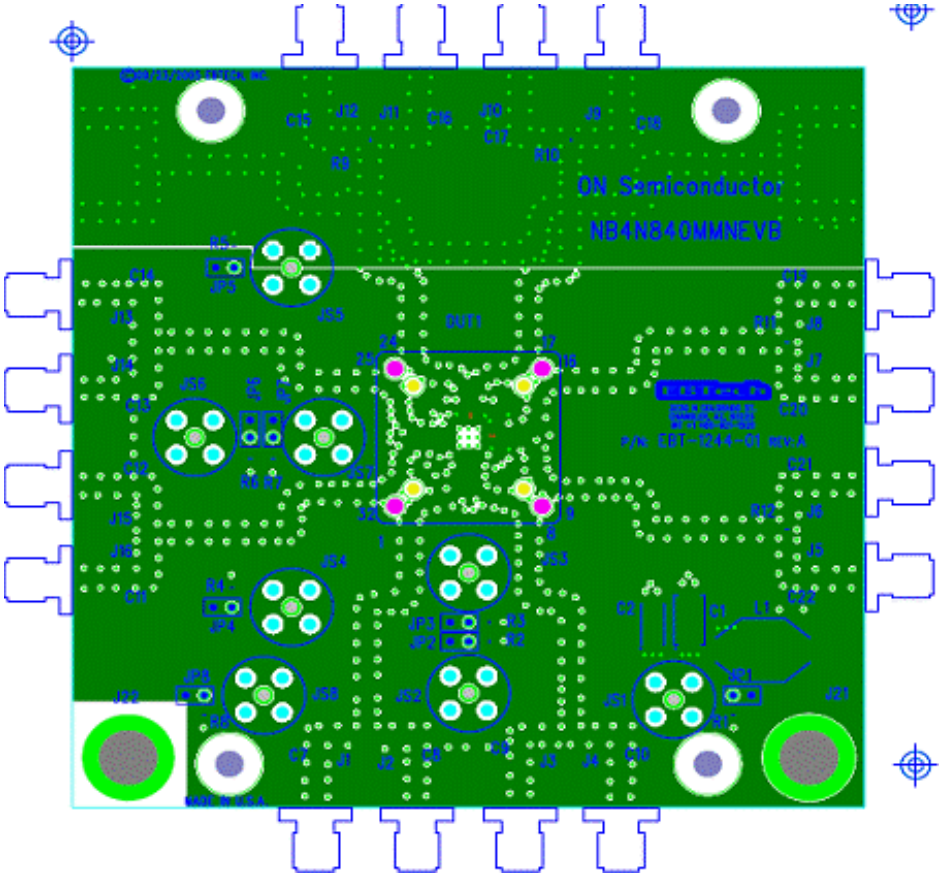

Figure 8. Power Layer

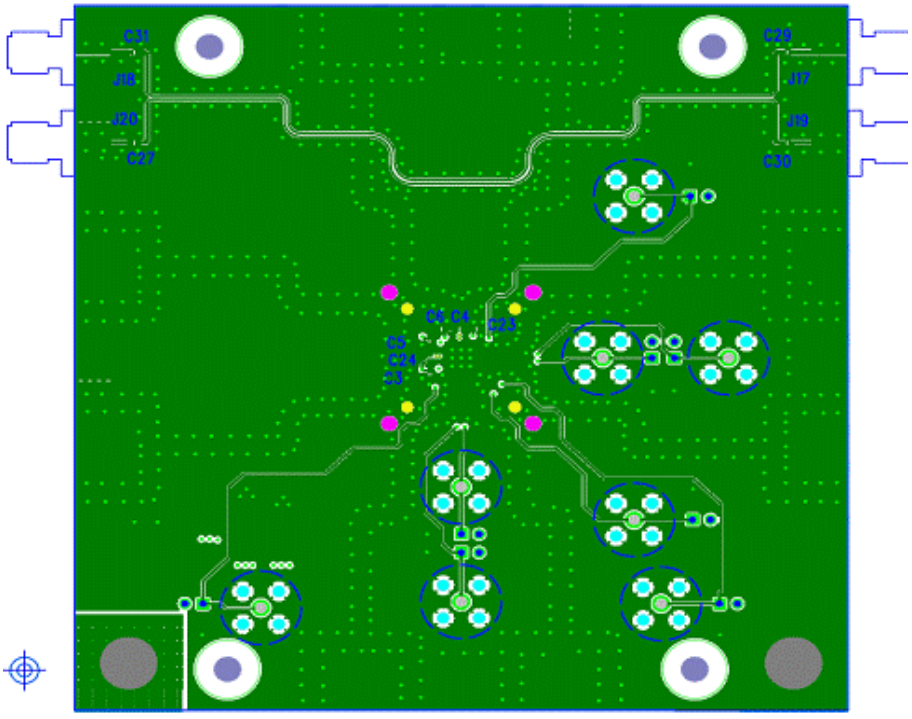

Figure 9. Bottom Layer

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