NB6L611

2.5V / 3.3V 1:2 Differential LVPECL Clock / Data Fanout Buffer

Multi−Level Inputs with Internal Termination

Description

The NB6L611 is a differential 1:2 clock or data fanout buffer. The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VTD pins and will accept LVPECL, CML, LVDS, LVCMOS or LVTTL logic levels.

The V_{REFAC} reference output can be used to rebias capacitor−coupled differential or single−ended input signals. When used, decouple V_{REFAC} with a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When used, decouple V_{REFAC} with a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{REFAC} output should be left open.

The device is housed in a small 3x3 mm 16 pin QFN package.

The NB6L611 is a member of the ECLinPS MAX™ family of high performance clock and data management products.

Features

- Input Clock Frequency > 4.0 GHz
- 280 ps Typical Propagation Delay
- 100 ps Typical Rise and Fall Times
- 0.5 ps maximum RMS Clock Jitter
- Differential LVPECL Outputs, 780 mV Amplitude, typical
- LVPECL Operating Range: V_{CC} = 2.375 V to 3.63 V with V_{EE} = 0 V
- NECL Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.63 V
- Internal Input Termination Resistors, 50 Ω
- V_{REFAC} Reference Output Voltage
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- −40°C to +85°C Ambient Operating Temperature
- These are Pb−Free Devices

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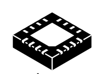
MARKING DIAGRAM*



QFN−16
MN SUFFIX
CASE 485G

16

1

NB6L
611
ALYW▪
▪

A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

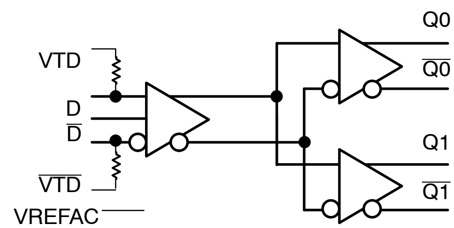


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

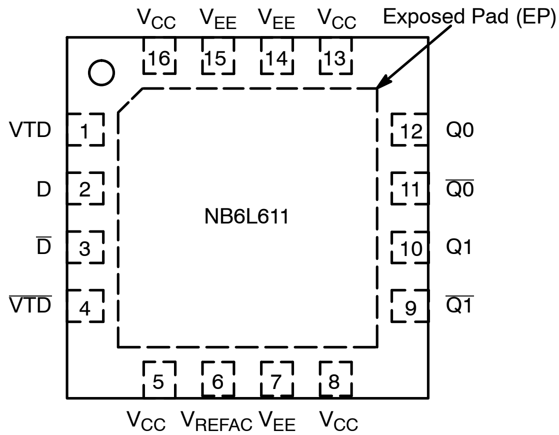


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	VTD	–	Internal 50 Ω Termination Pin for D input.
2	D	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted Differential Input. Note1. Internal 50 Ω Resistor to Termination Pin, VTD.
3	$\overline{D}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input. Note 1. Internal 50 Ω Resistor to Termination Pin, $\overline{VTD}$.
4	$\overline{VTD}$	–	Internal 50 Ω Termination Pin for $\overline{D}$ input.
5	V_{CC}	–	Positive Supply Voltage
6	V_{REFAC}		Output Reference Voltage for direct or capacitor coupled inputs
7	V_{EE}	–	Negative Supply Voltage
8	V_{CC}	–	Positive Supply Voltage
9	$\overline{Q1}$	LVPECL Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC} – 2.0 V.
10	Q1	LVPECL Output	Noninverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC} – 2.0 V.
11	$\overline{Q0}$	LVPECL Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC} – 2.0 V.
12	Q0	LVPECL Output	Noninverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC} – 2.0 V.
13	V_{CC}	–	Positive Supply Voltage
14	V_{EE}	–	Negative Supply Voltage
15	V_{EE}	–	Negative Supply Voltage
16	V_{CC}	–	Positive Supply Voltage
–	EP	–	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to V_{EE} on the PC board.

1. In the differential configuration when the input termination pins (VTD, $\overline{VTD}$) are connected to a common termination voltage or left open, and if no signal is applied on D/$\overline{D}$ input, then, the device will be susceptible to self−oscillation.
2. All V_{CC} and V_{EE} pins must be externally connected to a power supply for proper operation.

Table 2. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200V
Moisture Sensitivity	16−QFN	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	V_{EE} = 0 V		4.0	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		−4.0	V
V_{IO}	Positive Input/Output Voltage Negative Input/Output Voltage	V_{EE} = 0 V V_{CC} = 0 V	$-0.5 \le V_{Io} \le V_{CC} + 0.5$ $+0.5 \ge V_{Io} \ge V_{EE} - 0.5$	4.5 −4.5	V V
V_{INPP}	Differential Input Voltage $\lvert D - \overline{D} \rvert$			$V_{CC}-V_{EE}$	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{OUT}	Output Current (LVPECL Output)	Continuous Surge		50 100	mA mA
I_{VREFAC}	V_{REFAC} Sink/Source Current			± 2.0	mA
T_A	Operating Temperature Range	16 QFN		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 lfpm 500 lfpm	QFN−16 QFN−16	42 35	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	QFN−16	4	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 4. DC CHARACTERISTICS, Multi−Level Inputs V_{CC} = 2.375 V to 3.63 V, V_{EE} = 0 V, or V_{CC} = 0 V, V_{EE} = −2.375 V to −3.63 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY CURRENT					
I_{CC}	Power Supply Current (Inputs and Outputs Open)	30	45	60	mA
LVPECL OUTPUTS (Notes 4 and 5)					
V_{OH}	Output HIGH Voltage V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 1075 2225 1425	V_{CC} − 950 2350 1550	V_{CC} − 825 2475 1675	mV
V_{OL}	Output LOW Voltage V_{CC} = 3.3V V_{CC} = 2.5V	V_{CC} − 1875 1475 675	V_{CC} − 1725 1575 775	V_{CC} − 1625 1675 875	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (see Figures 9 and 10) (Note 6)					
V_{th}	Input Threshold Reference Voltage Range (Note 7)	V_{EE} + 1050		V_{CC} − 150	mV
V_{IH}	Single−ended Input HIGH Voltage	V_{th} + 150		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage	V_{EE}		V_{th} − 150	mV
V_{ISE}	Single−ended Input Voltage Amplitude (V_{IH} − V_{IL})	300		V_{CC}−V_{EE}	mV
V_{REFAC}					
V_{REFAC}	Output Reference Voltage (V_{CC} ≥ 25 V)	V_{CC} – 1.525	V_{CC} – 1.425	V_{CC} – 1.325	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 11, 12 and 13) (Note 8)					
V_{IHD}	Differential Input HIGH Voltage	V_{EE} + 1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{CC} − 150	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	V_{EE} + 150		V_{CC}−V_{EE}	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note9)	V_{EE} + 950		V_{CC} − 75	mV
I_{IH}	Input HIGH Current D/$\overline{D}$, (VTD/$\overline{VTD}$ Open)	−150		150	μA
I_{IL}	Input LOW Current D/$\overline{D}$, (VTD/$\overline{VTD}$ Open)	−150		150	μA
TERMINATION RESISTORS					
R_{TIN}	Internal Input Termination Resistor (Measured from D to VTD)	40	50	60	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. LVPECL outputs loaded with 50 Ω to V_{CC} − 2.0 V for proper operation.
5. Input and output parameters vary 1:1 with V_{CC}.
6. V_{th}, V_{IH}, $V_{IL,}$, and V_{ISE} parameters must be complied with simultaneously.
7. V_{th} is applied to the complementary input when operating in single−ended mode.
8. V_{IHD}, $V_{ILD,}$ V_{ID} and V_{CMR} parameters must be complied with simultaneously.
9. V_{CMR} minimum varies 1:1 with V_{EE}, V_{CMR} maximum varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 5. AC CHARACTERISTICS V_{CC} = 2.375 V to 3.63 V, V_{EE} = 0 V, or V_{CC} = 0 V, V_{EE} = −2.375 V to −3.63 V, T_A = −40°C to +85°C; (Note 10)

Symbol	Characteristic		Min	Typ	Max	Unit
V_{OUTPP}	Output Voltage Amplitude (@ V_{INPP}) (Note 14) (See Figure 3)	$f_{in} \le$ 1.5 GHz f_{in} = 2.0 GHz f_{in} = 3.0 GHz f_{in} = 4.0 GHz	725 520 320 170	780 680 500 400		mV
t_{PD}	Propagation Delay	D to Q	225	280	375	ps
t_{SKEW}	Duty Cycle Skew (Note 11) Within Device Skew Device to Device Skew (Note 12)			 3 	15 15 80	ps
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	$f_{in} \le$ 4.0 GHz	40	50	60	ps
t_{JITTER}	RMS Random Clock Jitter (Note 13)	$f_{in} \le$ 4.0 GHz		0.2	0.5	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 14)		150		$V_{CC} - V_{EE}$	mV
t_r,t_f	Output Rise/Fall Times @ 0.5 GHz (20% − 80%)	Q, $\overline{Q}$		100	170	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Measured by forcing V_{INPP} (MIN) from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{CC} − 2.0 V. Input edge rates 40 ps (20% − 80%).
11. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw}− and T_{pw}+ @ 0.5GHz.
12. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.
13. Additive RMS jitter with 50% duty cycle clock signal.
14. Input and output voltage swing is a single−ended measurement operating in differential mode.

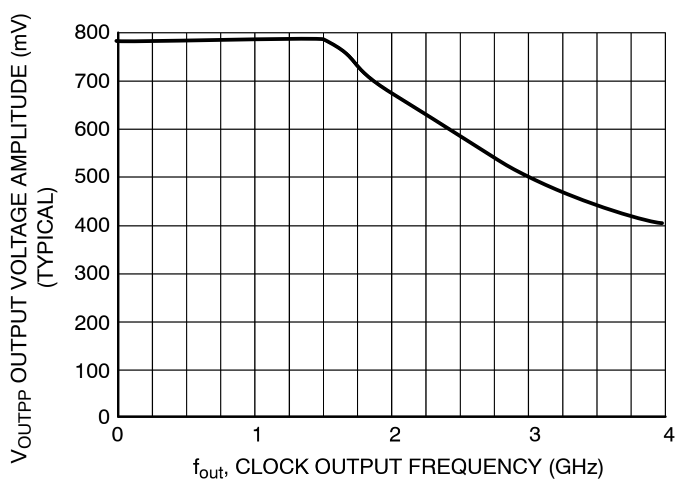


Figure 3. Output Voltage Amplitude (V_{OUTPP}) versus Output Frequency at Ambient Temperature (Typical)

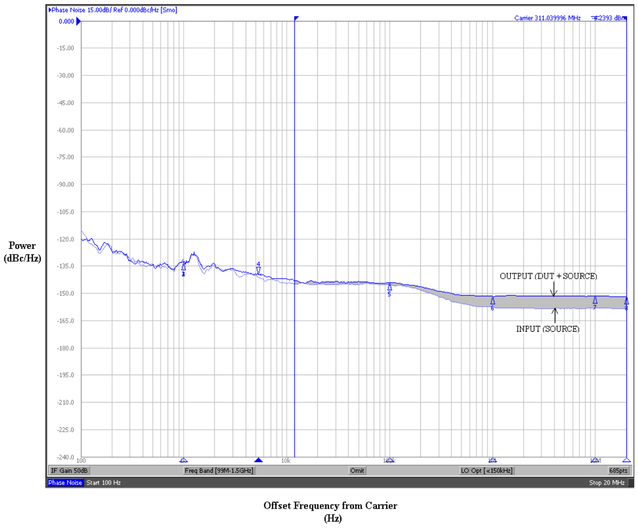


Figure 4. Typical Phase Noise Plot at $f_{carrier}$ = 311.04 MHz

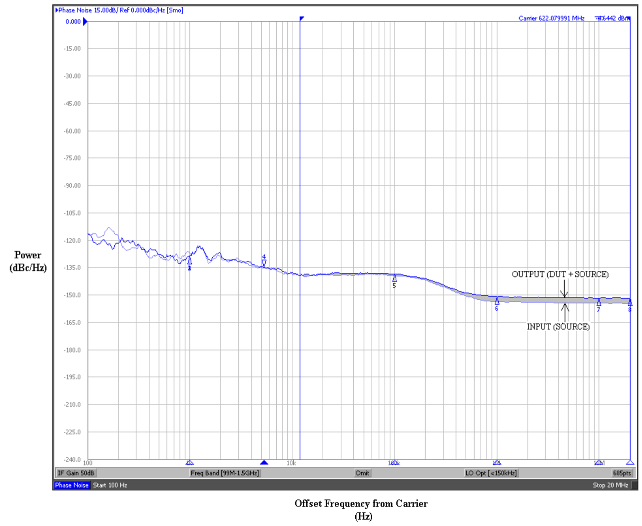


Figure 5. Typical Phase Noise Plot at $f_{carrier}$ = 622.08 MHz

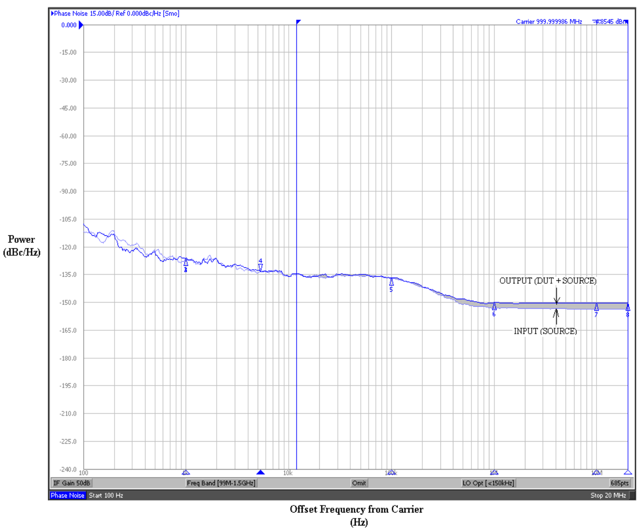


Figure 6. Typical Phase Noise Plot at $f_{carrier}$ = 1 GHz

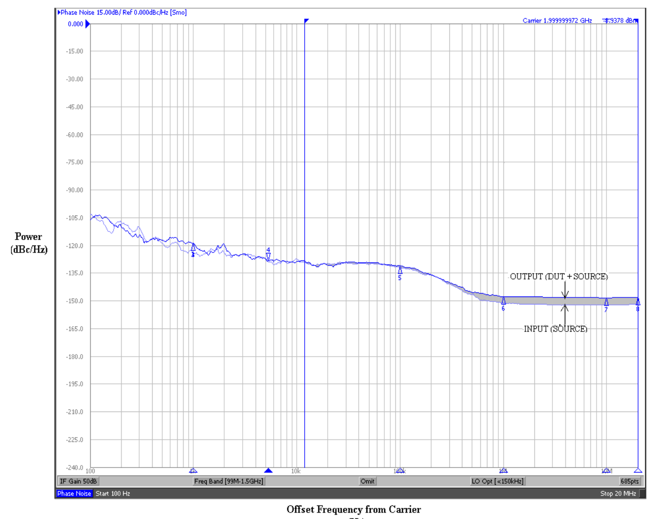


Figure 7. Typical Phase Noise Plot at $f_{carrier}$ = 2 GHz

The above phase noise plots captured using Agilent E5052A show additive phase noise of the NB6L611 device at frequencies 311.04 MHz, 622.08 MHz, 1 GHz and 2 GHz respectively at an operating voltage of 3.3 V in room temperature. The RMS Phase Jitter contributed by the device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 44 fs, 11 fs, 8 fs and 6 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.

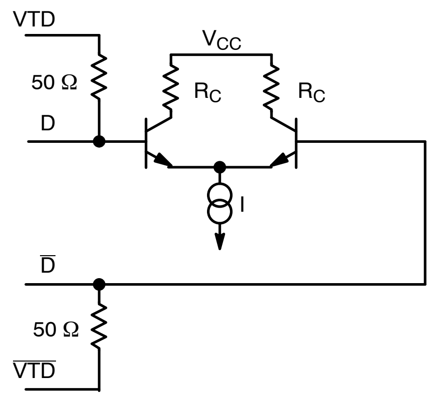


Figure 8. Input Structure

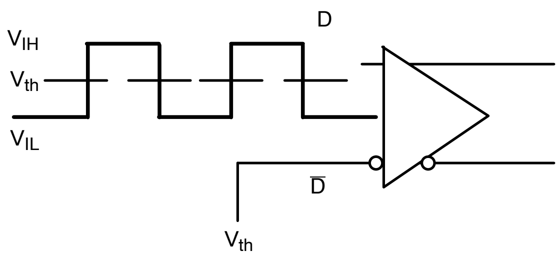


Figure 9. Differential Input Driven Single−Ended

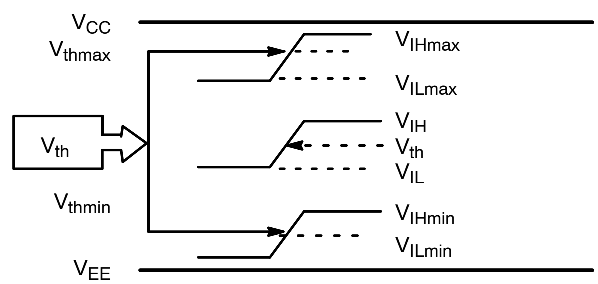


Figure 10. V_{th} Diagram

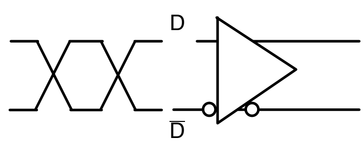


Figure 11. Differential Inputs Driven Differentially

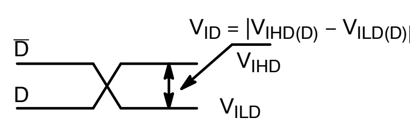


Figure 12. Differential Inputs Driven Differentially

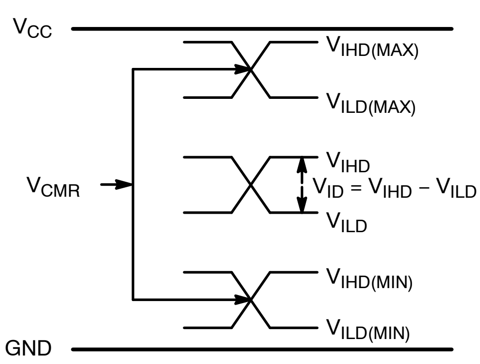


Figure 13. V_{CMR} Diagram

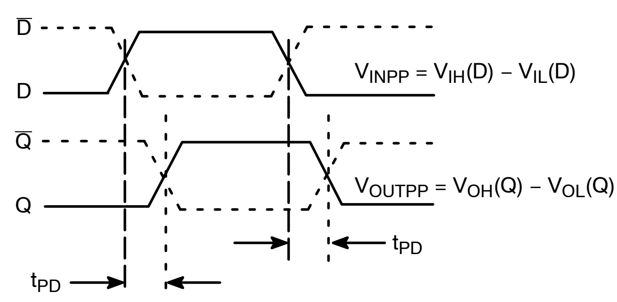


Figure 14. AC Reference Measurement

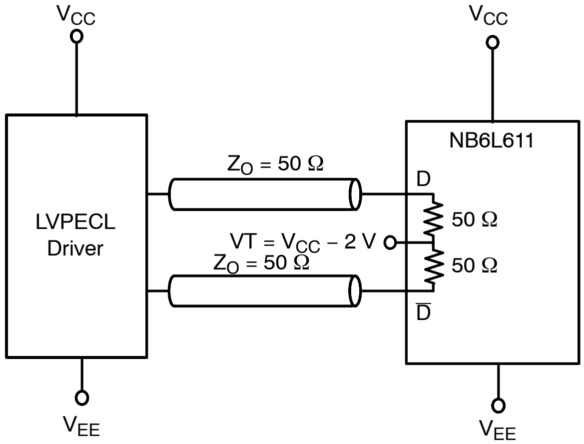


Figure 15. LVPECL Interface

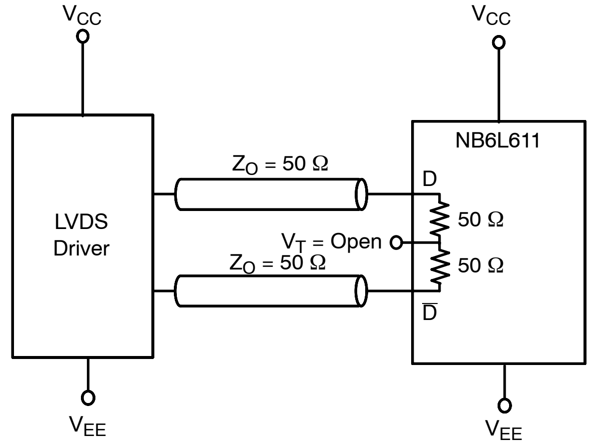


Figure 16. LVDS Interface

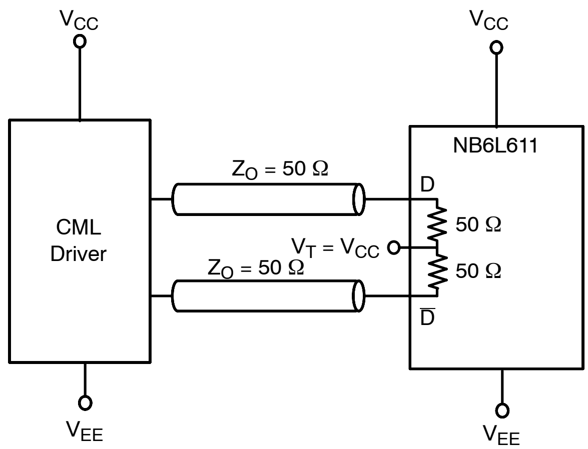


Figure 17. Standard 50 Ω Load CML Interface

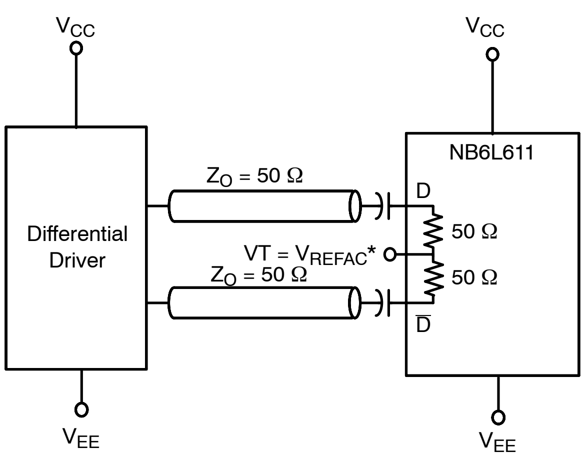


Figure 18. Capacitor−Coupled Differential Interface (VT Connected to V_{REFAC})

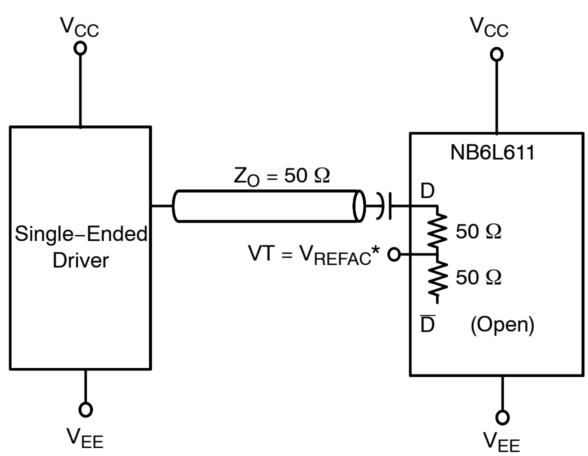


Figure 19. Capacitor−Coupled Single−Ended Interface (VT Connected to V_{REFAC})

*V_{REFAC} bypassed to ground with a 0.01 μF capacitor

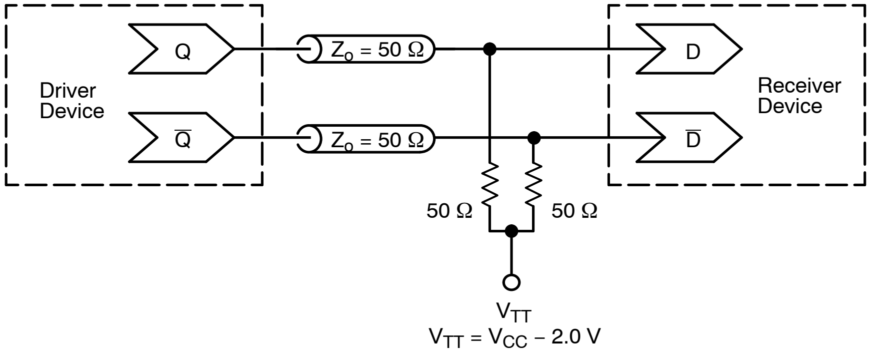


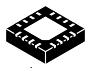
Figure 20. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
NB6L611MNG	QFN−16 (Pb−free)	123 Units / Rail
NB6L611MNR2G	QFN−16 (Pb−free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

The products described herein (NB6L611), may be covered by U.S. patents including 6,362,644. There may be other patents pending.



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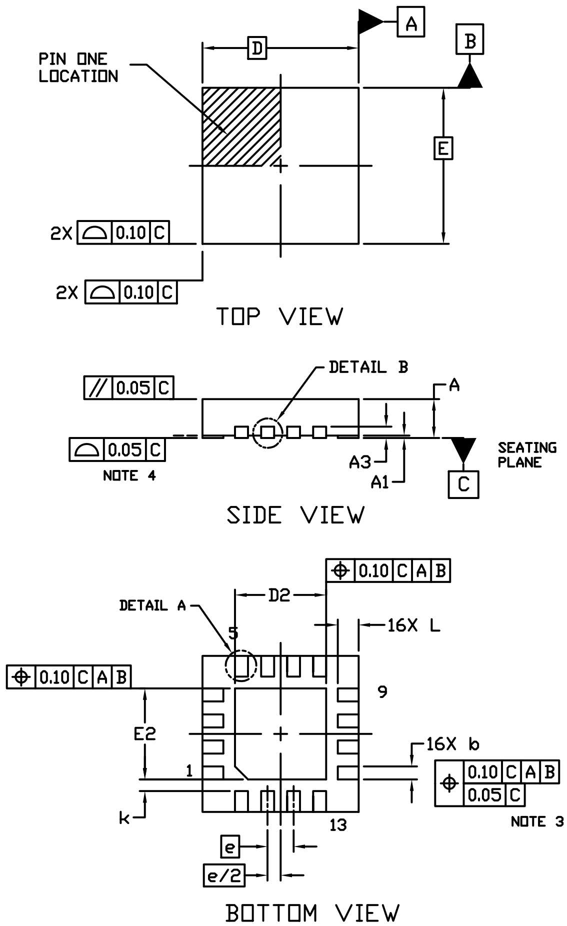
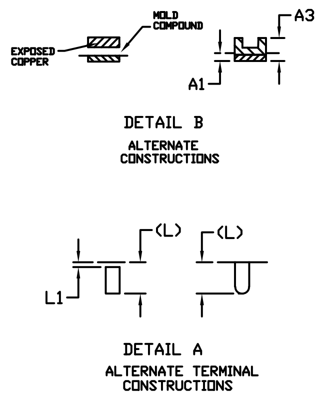
SCALE 2:1

QFN16 3x3, 0.5P
CASE 485G
ISSUE G

DATE 08 OCT 2021

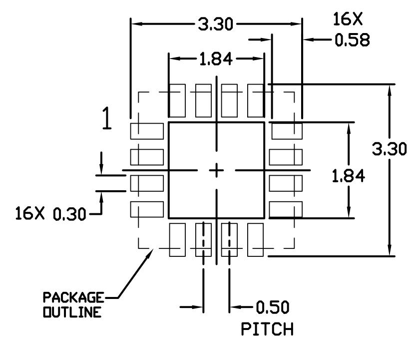


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



DIM	MILLIMETERS MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
k	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM*

XXXXX
XXXXX
ALYW▪
▪

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	QFN16 3X3, 0.5P	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
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Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative