NB7L32M

2.5V/3.3V, 14GHz ÷2 Clock Divider w/CML Output and Internal Termination

ON Semiconductor®

http://onsemi.com

Description

The NB7L32M is an integrated ÷2 divider with differential clock inputs and asynchronous reset.

Differential clock inputs incorporate internal 50 Ω termination resistors and accept LVPECL (Positive ECL), CML, or LVDS. The high frequency reset pin is asserted on the rising edge. Upon power−up, the internal flip−flops will attain a random state; the reset allows for the synchronization of multiple NB7L32M's in a system.

The differential 16 mA CML output provides matching internal 50 Ω termination which guarantees 400 mV output swing when externally receiver terminated 50 Ω to V_{CC} (See Figure 15).

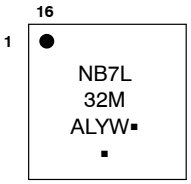
The device is housed in a small 3x3 mm 16 pin QFN package.

Features

- Maximum Input Clock Frequency 14 GHz Typical
- 200 ps Max Propagation Delay
- 30 ps Typical Rise and Fall Times
- < 0.5 ps Maximum (RMS) Random Clock Jitter
- Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- CML Output Level (400 mV Peak−to−Peak Output), Differential Output Only
- 50 Ω Internal Input and Output Termination Resistors
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- These are Pb−Free Devices

QFN−16
MN SUFFIX
CASE 485G

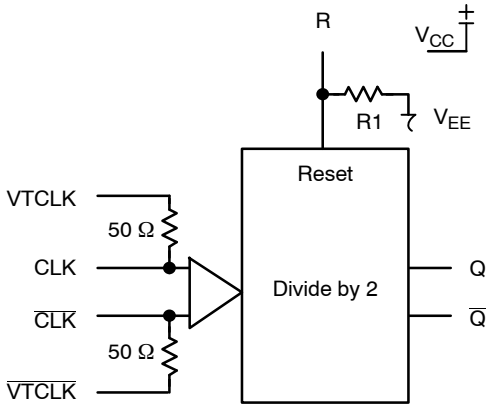
MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

CLK	$\overline{CLK}$	R	Q	$\overline{Q}$
x	x	H	L	H
Z	W	L	÷2	÷2

Z = LOW to HIGH Transition
W = HIGH to LOW Transition
x = Don't Care

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

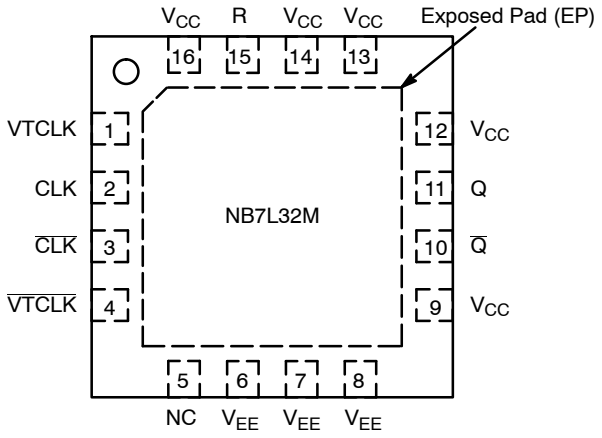


Figure 1. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	VTCLK	–	Internal 50 Ω termination pin. In the differential configuration when the input termination pin (VTCLK, VT$\overline{\text{CLK}}$) are connected to a common termination voltage or left open, and if no signal is applied on CLK/$\overline{\text{CLK}}$ input then the device will be susceptible to self−oscillation.
2	CLK	ECL, CML, LVDS Input	Noninverted differential input. In the differential configuration when the input termination pin (VTCLK, VT$\overline{\text{CLK}}$) are connected to a common termination voltage or left open and if no signal is applied on CLK/$\overline{\text{CLK}}$ input, then the device will be susceptible to self−oscillation.
3	$\overline{\text{CLK}}$	ECL, CML, LVDS Input	Inverted differential input. In the differential configuration when the input termination pin (VTCLK, VT$\overline{\text{CLK}}$) are connected to a common termination voltage or left open and if no signal is applied on CLK/$\overline{\text{CLK}}$ input, then the device will be susceptible to self−oscillation.
4	$\overline{\text{VTCLK}}$	–	Internal 50 Ω termination pin. In the differential configuration when the input termination pin (VTCLK, VT$\overline{\text{CLK}}$) are connected to a common termination voltage or left open and if no signal is applied on CLK/$\overline{\text{CLK}}$ input, then the device will be susceptible to self−oscillation.
5	NC	–	No connect. NC pin must be left open.
6, 7, 8	V_{EE}	–	Negative supply voltage.
9, 12, 13, 14, 16	V_{CC}	–	Positive supply voltage.
10	$\overline{\text{Q}}$	CML Output	Inverted differential output. Typically terminated with 50 Ω resistor to V_{CC}.
11	Q	CML Output	Noninverted differential output. Typically terminated with 50 Ω resistor to V_{CC}.
15	R	LVTTL/LVCMOS	Reset Input. Internal pulldown to 75 kΩ to V_{EE}.
–	EP	–	Exposed Pad. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a heat−sinking conduit. EP is electrically isolated from V_{CC} and V_{EE}.

Table 2. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor	R1	75 kΩ
ESD Protection	Human Body Model Machine Model	> 500 V > 30 V
Moisture Sensitivity (Note 1)	QFN−16	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		349
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		−3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 −3.6	V V
V_{INPP}	Differential Input Voltage			2.8	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{out}	Output Current	Continuous Surge		25 50	mA mA
T_A	Operating Temperature Range	QFN−16		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 2)	0 lfpm 500 lfpm	QFN−16 QFN−16	41.6 35.2	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	1S2P	QFN−16	4.0	°C/W
T_{sol}	Wave Solder Pb−Free	<3 sec @ 260°C		265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board − 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 4. DC CHARACTERISTICS, CLOCK INPUTS, CML OUTPUTS V_{CC} = 2.375 V to 3.465 V, V_{EE} = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Note 3)	50	65	80	mA
V_{OH}	Output HIGH Voltage (Note 4)	V_{CC} − 40	V_{CC} − 10	V_{CC}	mV
V_{OL}	Output LOW Voltage (Note 4)	V_{CC} − 500	V_{CC} − 400	V_{CC} − 300	mV
R_{TOUT}	Internal Output Termination Resistor	45	50	55	Ω
$R_{Temp\ Coef}$	Internal I/O Termination Resistor Temperature Coefficient		6.38		mΩ/°C
DIFFERENTIAL CLK/$\overline{CLK}$ INPUT DRIVEN SINGLE−ENDED (see Figure 9 and 11)					
V_{th}	Input Threshold Reference Voltage Range (Note 6)	1050		V_{CC}	mV
V_{IH}	Single−ended Input HIGH Voltage	V_{th} + 150		V_{CC} + 300	mV
V_{IL}	Single−ended Input LOW Voltage	V_{EE}		V_{th} − 150	mV
DIFFERENTIAL CLK/$\overline{CLK}$ INPUTS DRIVEN DIFFERENTIALLY (see Figure 10 and 12)					
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC} + 300	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{CC} − 75	mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 7)	1125		V_{CC}	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	150		2500	mV
I_{IH}	Input HIGH Current CLK/$\overline{CLK}$ (VTCLK/R/$\overline{VTCLK}$/$\overline{R}$ Open)	0	30	100	μA
I_{IL}	Input LOW Current CLK/$\overline{CLK}$(VTCLK/R/$\overline{VTCLK}$/$\overline{R}$ Open)	−50	0	50	μA
R_{TIN}	Internal Input Termination Resistor	45	50	55	Ω
LVTTL/LVCMOS RESET INPUT					
V_{IH}	Single−ended Input HIGH Voltage	2000		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage	V_{EE}		800	mV
I_{IH}	Input HIGH Current R	0	30	100	μA
I_{IL}	Input LOW Current R	0	10	100	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input termination pins open and all outputs loaded with external R_L = 50 Ω receiver termination resistor.
4. CML outputs require R_L = 50 Ω receiver termination resistors to V_{CC} for proper operation. (See Figure 8)
5. Input and output parameters vary 1:1 with V_{CC}.
6. V_{th} is applied to the complementary input when operating in single−ended mode.
7. $V_{CMR(MIN)}$ varies 1:1 with V_{EE}, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 6. AC CHARACTERISTICS V_{CC} = 2.375 V to 3.465 V, V_{EE} = 0 V (Note 8)

Symbol	Characteristic		−40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPP(MIN)}$)											mV
	(See Figures 2, 3, 4, 5, and 6)	$f_{in} \le 7$ GHz	190	330		190	330		190	330		
		$f_{in} \le 12$ GHz	160	320		160	320		160	320		
f_{IN}	Maximum Input Clock Frequency (See Figure 2)		12	14		12	14		12	14		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential (See Figure 7)	CLK to Q	130	155	200	130	155	200	130	155	200	ps
		R to Q	200	240	300	200	240	300	200	260	300	
t_{skew}	Duty Cycle Skew (Note 9)			2	20		2	20		2	20	
	Device−to−Device Skew (Note 12)			6	50		6	50		6	50	
t_{RR}	Reset Recovery (See Figure 7)		300	135		300	135		300	135		ps
t_{PW}	Minimum Pulse Width	R	500	210		500	210		500	210		ps
t_{JITTER}	Random Clock Jitter (RMS) (Note 11)	$f_{in} \le 7$ GHz		0.13	0.5		0.13	0.5		0.13	0.5	ps
		f_{in} = 12 GHz		0.14	0.5		0.14	0.5		0.14	0.5	
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 10)		150		2500	150		2500	150		2500	mV
t_r t_f	Output Rise/Fall Times @ 1 GHz (20% − 80%)			30	45		30	45		30	45	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Measured by forcing $V_{INPP(MIN)}$ from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{CC}. Input edge rates 40 ps (20% − 80%).
9. Duty cycle skew is measured between differential outputs using the deviations of the sum of Tpw− and Tpw+ 1 GHz.
10. $V_{INPP(MAX)}$ cannot exceed V_{CC} − V_{EE}. Input voltage swing is a single−ended measurement operating in differential mode.
11. Additive RMS jitter with 50% duty cycle input clock signal.
12. Device−to−device skew is measured between outputs under identical transition @ 1 GHz.

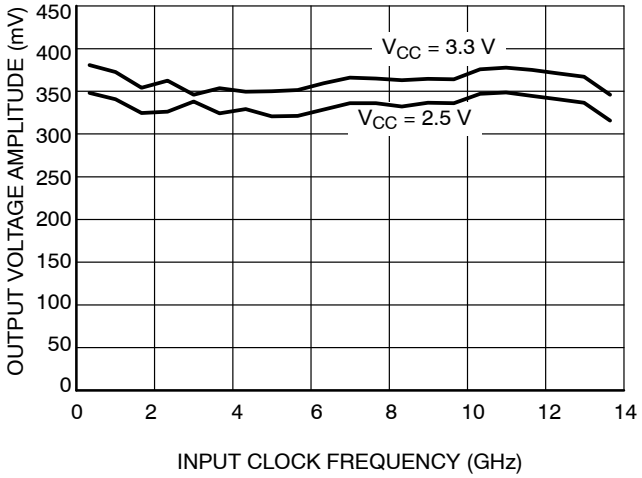


Figure 2. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{OUT}) at Ambient Temperature (V_{INPP} = 150 mV)

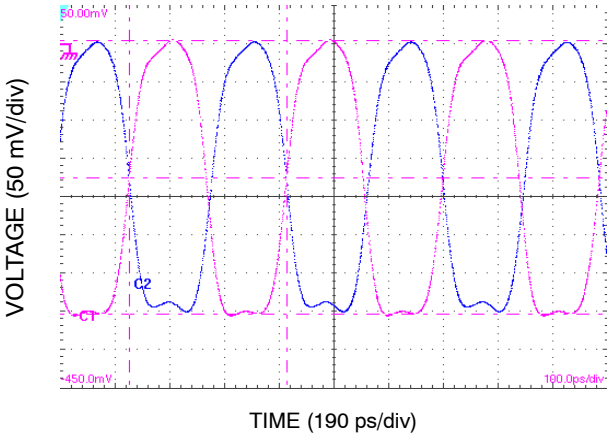


Figure 3. Typical Output Waveform with f_{IN} = 7 GHz(V_{CC} = 2.5 V, V_{INPP} = 400 mV, Room Temperature, V_{OUTPP} = 357 mV, t_r = 33 ps, t_f = 30 ps, f_{OUT} = 3.499 GHz)

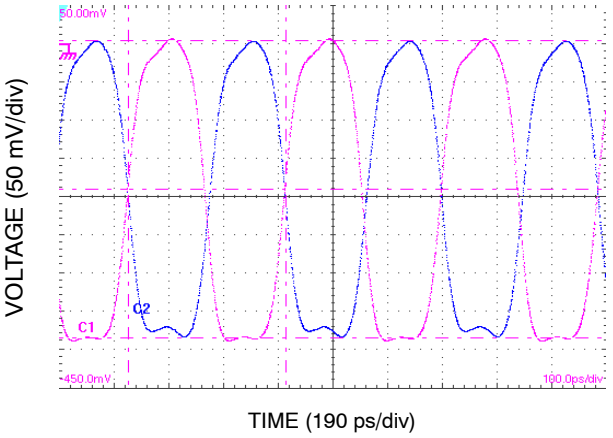


Figure 4. Typical Output Waveform with f_{IN} = 7 GHz(V_{CC} = 3.3 V, V_{INPP} = 400 mV, Room Temperature, V_{OUTPP} = 387 mV, t_r = 32 ps, t_f = 29.8 ps, f_{OUT} = 3.499 GHz)

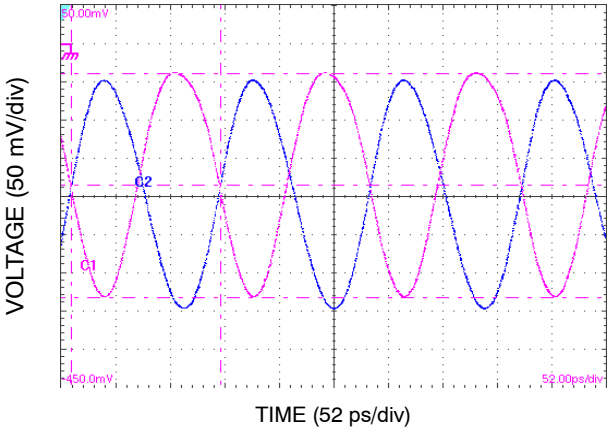


Figure 5. Typical Output Waveform with f_{IN} = 14 GHz(V_{CC} = 2.5 V, V_{INPP} = 400 mV, Room Temperature, V_{OUTPP} = 292 mV, t_r = 25 ps, t_f = 27 ps, f_{OUT} = 7.01 GHz)

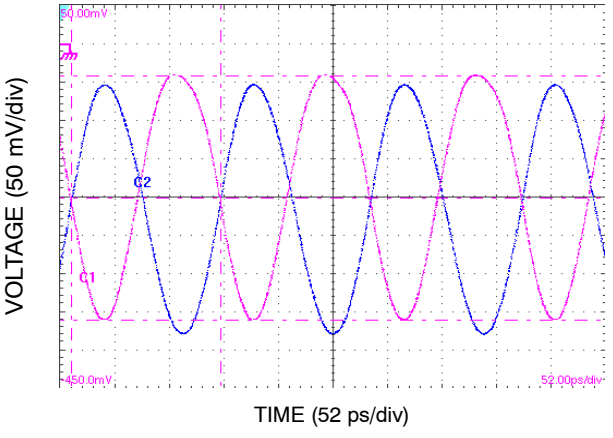


Figure 6. Typical Output Waveform with f_{IN} = 14 GHz(V_{CC} = 3.3 V, V_{INPP} = 400 mV, Room Temperature, V_{OUTPP} = 319 mV, tr = 25 ps, t_f = 26 ps, f_{OUT} = 7.01 GHz)

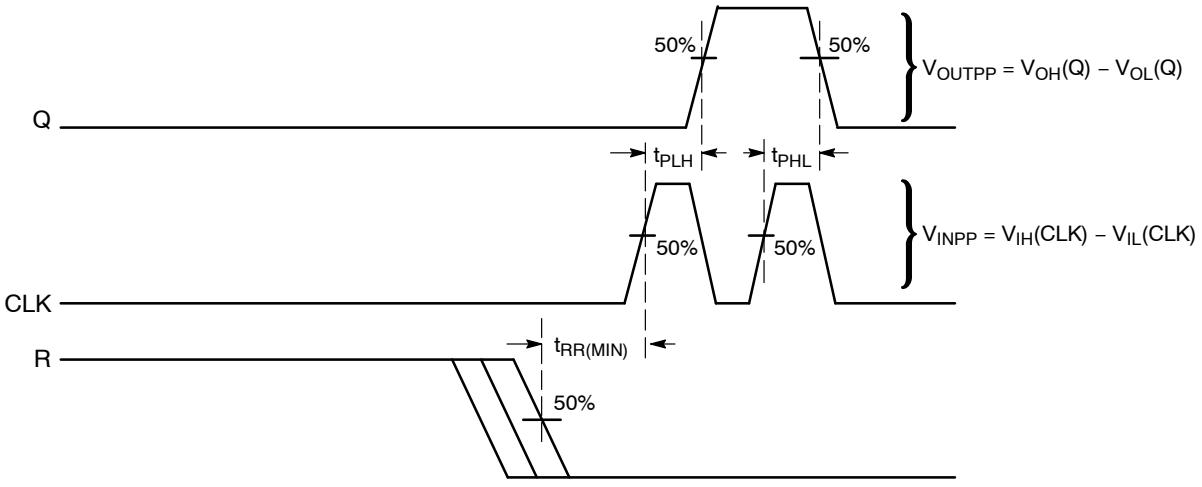


Figure 7. AC Reference Measurement (Timing Diagram)

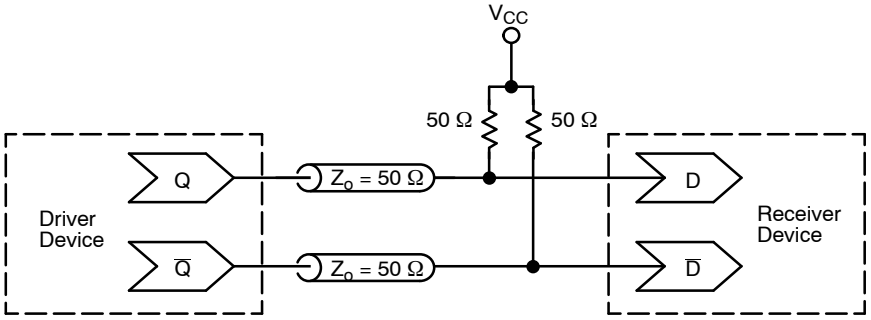


Figure 8. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8073/D – Termination of CML Logic Devices.)

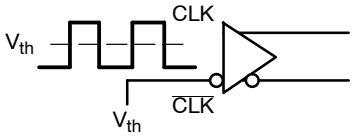


Figure 9. Differential Input Driven Single−Ended

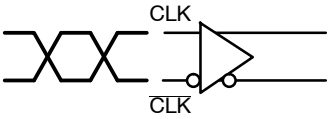


Figure 10. Differential Inputs Driven Differentially

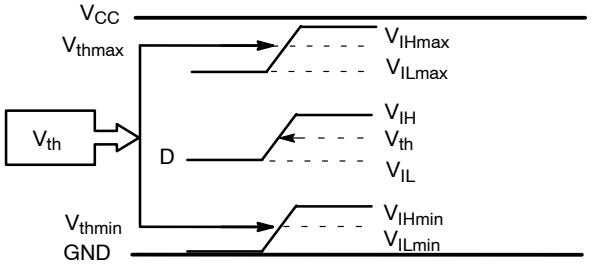
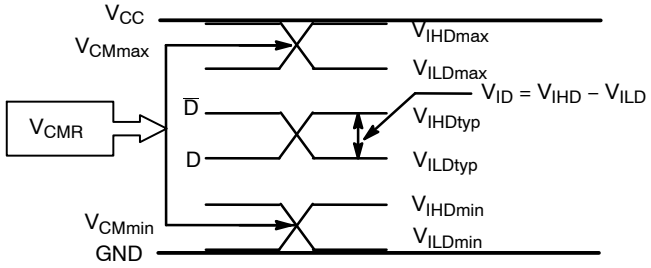


Figure 11. V_{th} Diagram



NOTE: $V_{EE} \le V_{IN} \le V_{CC} + 300$ mV; $V_{IH} > V_{IL}$

Figure 12. V_{CMR} Diagram

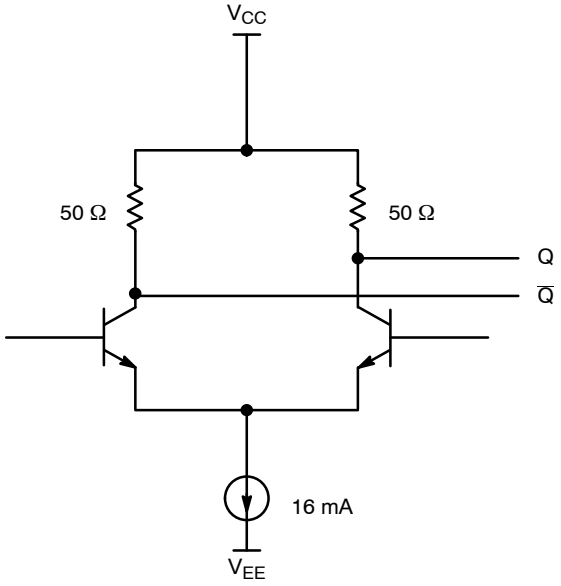


Figure 13. CML Output Structure

APPLICATION INFORMATION

All NB7L32M inputs can accept PECL, CML, and LVDS signal levels. The limitations for differential input signal (LVDS, PECL, or CML) are minimum input swing of 150 mV and the maximum input swing of 2500 mV. Within these conditions, the input voltage can range from V_{CC} to 1.2 V. Examples interfaces are illustrated below in a 50 Ω environment (Z = 50 Ω). For output termination and interface, refer to application note AND8020/D.

Table 5. INTERFACING OPTIONS

Interfacing Options	Connections
CML	Connect VTD and $\overline{VTD}$ to V_{CC} (See Figure 14)
LVDS	Connect VTD and $\overline{VTD}$ Together (See Figure 16)
AC−COUPLED	Bias VTD and $\overline{VTD}$ Inputs within Common Mode Range (V_{CMR}) (See Figure 15)
RSECL, PECL, NECL	Standard ECL Termination Techniques (See Figure 8)

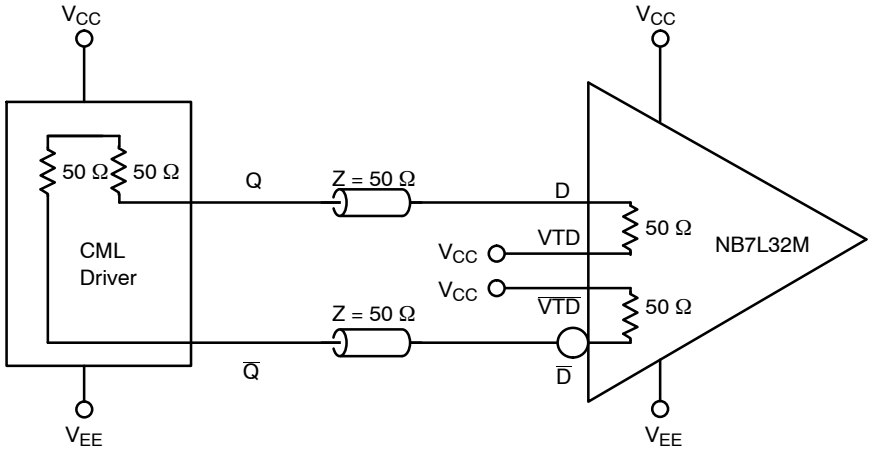
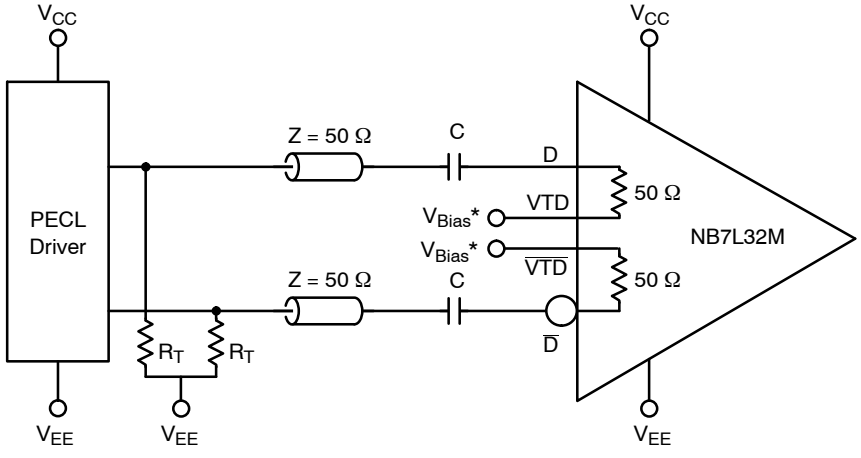


Figure 14. CML to NB7L32M Interface



Recommended R_T Values

V_{CC}	R_T
5.0 V	290 Ω
3.3 V	150 Ω
2.5 V	80 Ω

*V_{Bias} must be within common mode range limits (V_{CMR})

Figure 15. PECL to NB7L32M Interface

APPLICATION INFORMATION

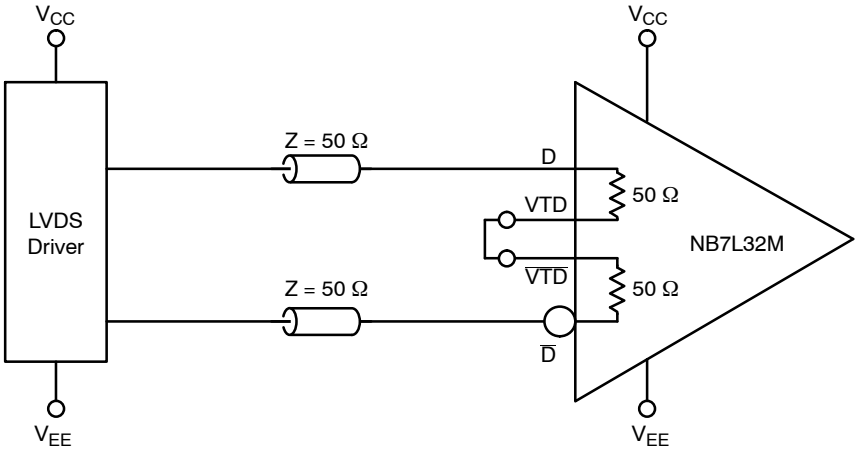


Figure 16. LVDS to NB7L32M Interface

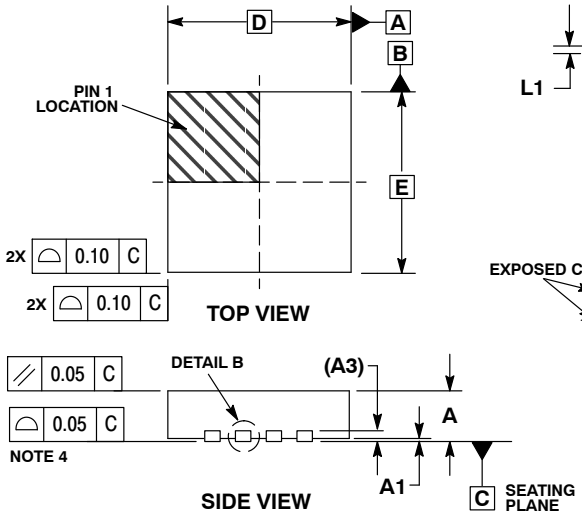
ORDERING INFORMATION

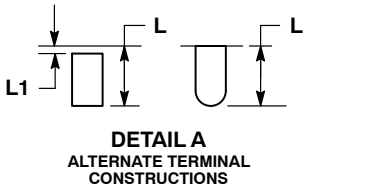
Device	Package	Shipping†
NB7L32MMNG	QFN−16 (Pb−Free)	123 Units / Rail
NB7L32MMNR2G	QFN−16 (Pb−Free)	3000 / Tape & Reel

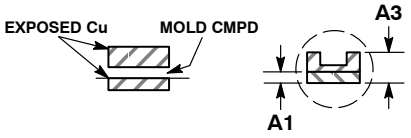
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485G−01
ISSUE F

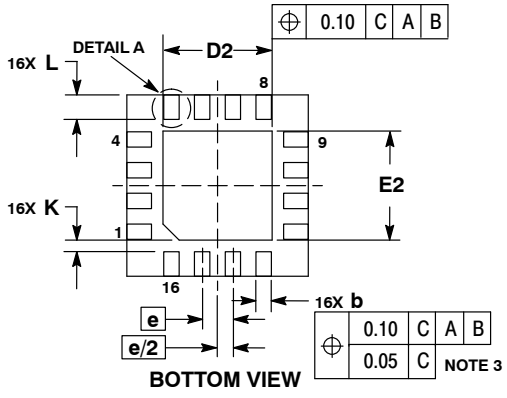




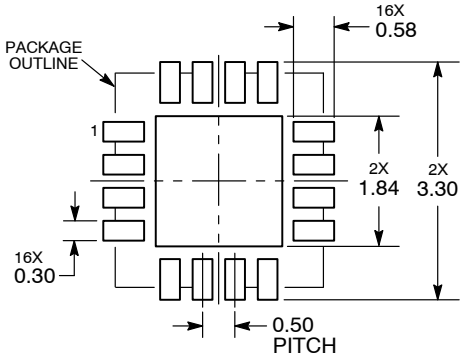


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	1.65	1.75	1.85
E		3.00 BSC	
E2	1.65	1.75	1.85
e		0.50 BSC	
K		0.18 TYP	
L	0.30	0.40	0.50
L1	0.00	0.08	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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