NB7N017M

3.3 V SiGe 8-Bit Dual Modulus Programmable Divider/Prescaler with CML Outputs

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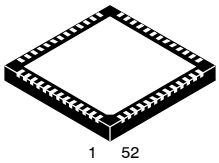


QFN−52
MN SUFFIX
CASE 485M−01

Description

The NB7N017M is a high speed 8-bit dual modulus programmable divider/prescaler with 16 mA CML outputs capable of switching at input frequencies greater than 3.5 GHz. The CML output structure contains internal 50 Ω source termination resistor to V_{CC}. The device generates 400 mV output amplitude with 50 Ω receiver resistor to V_{CC}. This I/O structure enables easy implementation of the NB7N017M in 50 Ω systems.

The differential inputs contain 50 Ω termination resistors to VT pads and all differential inputs accept RSECL, ECL, LVDS, LVCMOS, LVTTL, and CML.

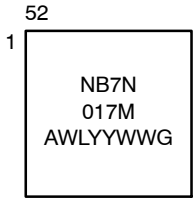
Internally, the NB7N017M uses a > 3.5 GHz 8-bit programmable down counter. A select pin, SEL, is used to select between two words, Pa[0:7] and Pb[0:7], that are stored in REGa and REGb respectively. Two parallel load pins, PLa and PLb, are used to load the level triggered programming registers, REGa and REGb, respectively. A differential clock enable, CE, pin is available.

The NB7N017M offers a differential output, TC. Terminal count output, TC, goes high for one clock cycle when the counter has reached the all zeros state. To reduce output phase noise, TC is retimed with the rising edge triggered latches.

Features

- Maximum Input Clock Frequency > 3.5 GHz Typical
- Differential CLK Clock Input
- Differential CE Clock Enable Input
- Differential SEL Word Select Input
- 50 Ω Internal Input and Output Termination Resistors
- Differential TC Terminal Count Output
- All Outputs 16 mA CML with 50 Ω Internal Source Termination to V_{CC}
- All Single-Ended Control Pins CMOS and PECL/NECL Compatible
- Counter Programmed Using One of Two Single-Ended Words, Pa[0:7] and Pb[0:7], Stored in REGa and REGb
- REGa and REGb Implemented with Level Triggered Latch
- Compatible with Existing 3.3 V LVEP, EP, and SG Devices
- Ability to Program the Divider without Disturbing Current Settings
- Positive CML Output Operating Range:
  - V_{CC} = 3.0 V to 3.465 V with V_{EE} = 0 V
- Negative CML Output Operating Range:
  - V_{CC} = 0 V with V_{EE} = –3.0 V to –3.465 V
- V_{BB} Reference Voltage Output
- CML Output Level: 400 mV Peak-Peak Output with 50 Ω Receiver Resistor to V_{CC}
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MARKING DIAGRAM*



A	= Assembly Site
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
NB7N017MMNG	QFN−52 (Pb-Free)	260 Tray JEDEC
NB7N017MMNR2G	QFN−52 (Pb-Free)	2000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

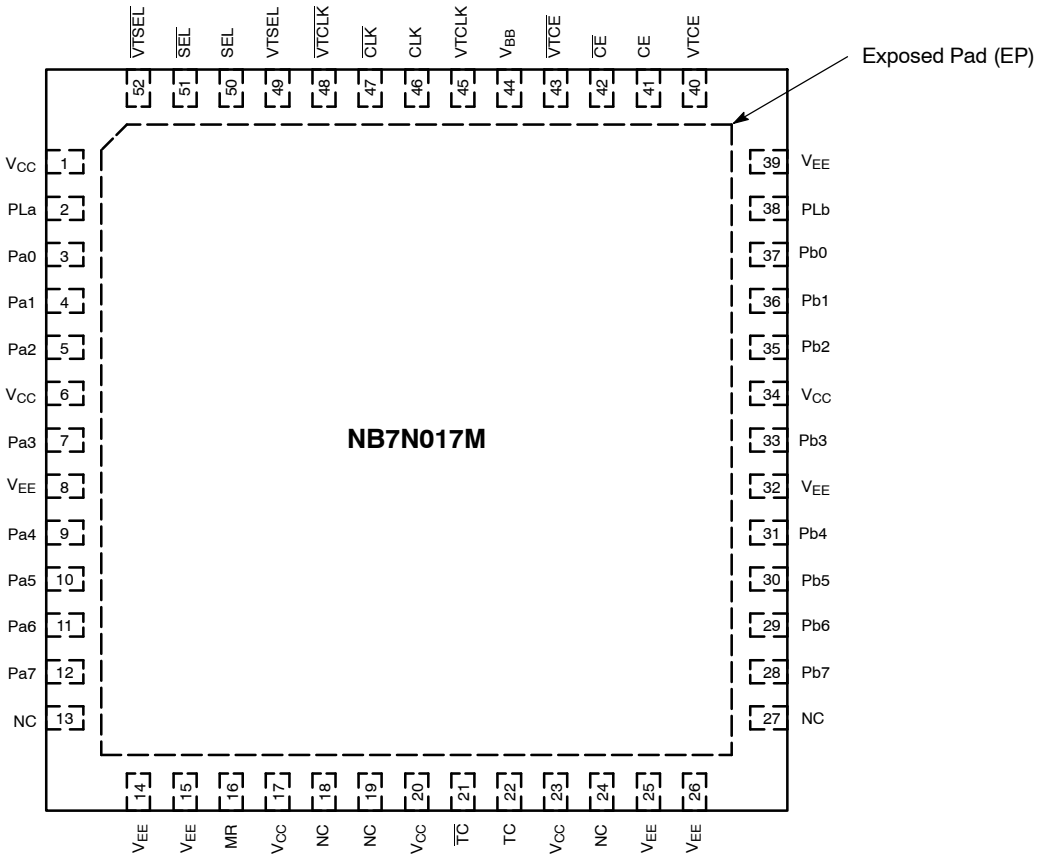


Figure 1. Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin Name	I/O	Default State	Single/Differential (Notes 1 and 2)	Description
CLK	ECL, CML, LVCMOS, LVDS, LVTTL Input	–	Differential	Clock
CE	ECL, CML, LVCMOS, LVDS, LVTTL Input	–	Differential	Clock Enable
MR	CMOS, ECL Input	Low	Single	Asynchronous Master Reset: Counter set to 0000 0000 to reload at next CLK pulse, REGa and REGb = 1111 1111 and TC = 1.
SEL	ECL, CML, LVCMOS, LVDS, LVTTL Input	–	Differential	Divide Select
PLa, PLb	CMOS, ECL Input	Low	Single	Parallel Load Counter Latch from Pa[0:7], Pb[0:7] (Level Triggered)
TC	CML Output	–	Differential	Terminal Count, 16 mA CML output with 50 Ω Source Termination to V_{CC} (Note 5)
Pa[0:7], Pb[0:7]	CMOS, ECL Input	High	Single	Counter Program Pins. CMOS and PECL/NECL compatible Pa7 = MSB, Pb7 = MSB
V_{CC}	Power	–	–	Positive Supply
V_{EE}	Power	–	–	Negative Supply
VTCLK, $\overline{\text{VTCLK}}$, VTSEL, $\overline{\text{VTSEL}}$ VTCE, $\overline{\text{VTCE}}$	Termination	–	Differential	50 Ω Internal Input Termination Resistor (Note 6)
V_{BB}	Output	–	–	CMOS/ECL Reference Voltage Output
NC	N/A	–	–	No Connect (Note 4)
EP	–	–	–	Exposed Pad (Note 3)

1. All high speed inputs and outputs are differential to improve performance.
2. All single-ended inputs are CMOS and NECL/ECL compatible.
3. All V_{CC} and V_{EE} pins must be externally connected to external power supply voltage to guarantee proper device operation. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a heat-sinking conduit. Exposed pad is bonded to the lowest voltage potential, V_{EE}.
4. The NC pins are electrically connected to the die and must be left open.
5. CML outputs require 50 Ω receiver termination resistor to V_{CC} for proper operation.
6. In the differential configuration when the input termination pins are connected to the common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.

Table 2. CE Truth Table

CE	Clock Status
LOW HIGH	Clock Disabled Clock Enabled

Table 3. SEL Truth Table

SEL	Active Register
LOW HIGH	REGa REGb

Table 4. Register Programming Values for Various Divide Ratios

Pa7/Pb7	Pa6/Pb6	Pa5/Pb5	Pa4/Pb4	Pa3/Pb3	Pa2/Pb2	Pa1/Pb1	Pa0/Pb0	Divide By
0	0	0	0	0	0	0	0	undefined
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

Table 5. Function Table

MR	Pla	PLb	SEL	CE	CLK	Function
H	X	X	X	X	X	Master Reset (Counter programmed to 0000 0000, REGa and REGb programmed to 1111 1111 and TC to 1)
L	H	L	X	X	X	REGa is transparent to Pa[0:7]
L	L	H	X	X	X	REGb is transparent Pb[0:7]
L	L	L	L	H	Z	Count; At TC pulse, load counter from REGa
L	L	L	H	H	Z	Count; At TC pulse, load counter from REGb
L	X	X	X	L	X	Hold

X – Don't Care
H – HIGH
L – LOW
Z – Rising Edge

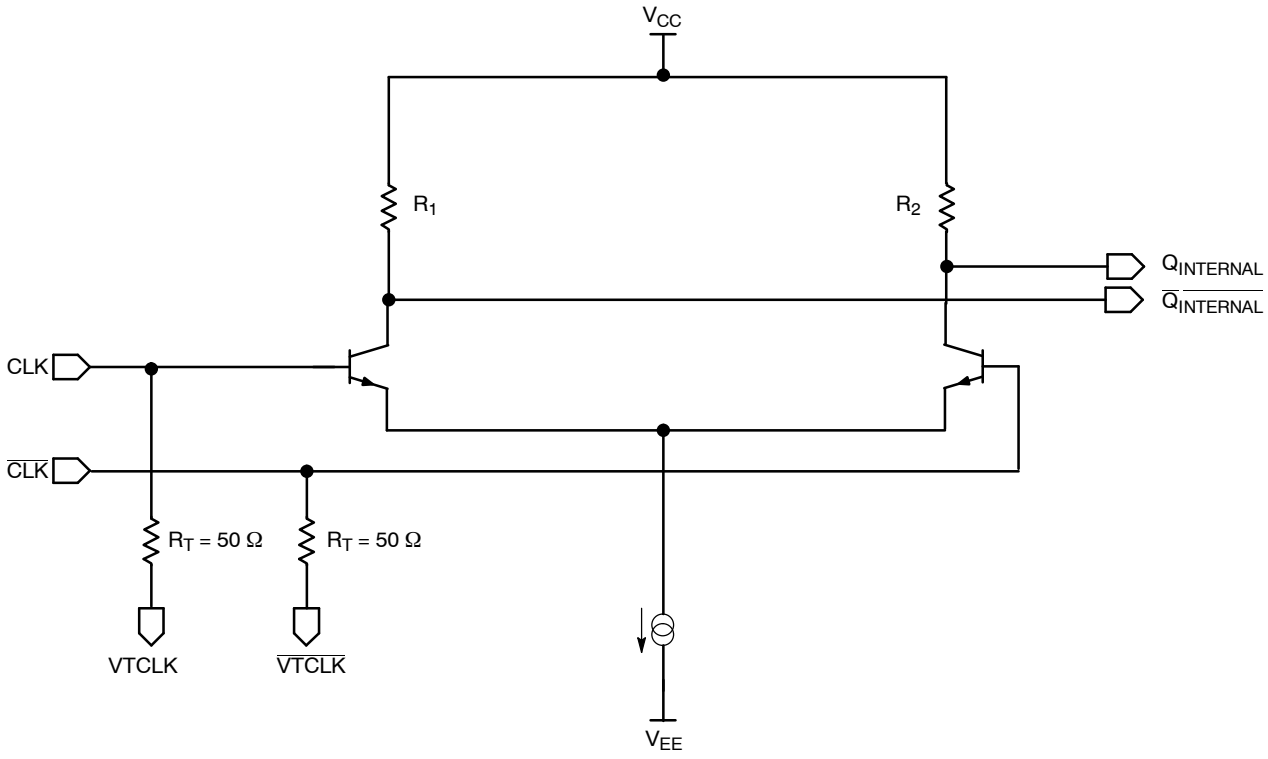


Figure 2. Input Structure

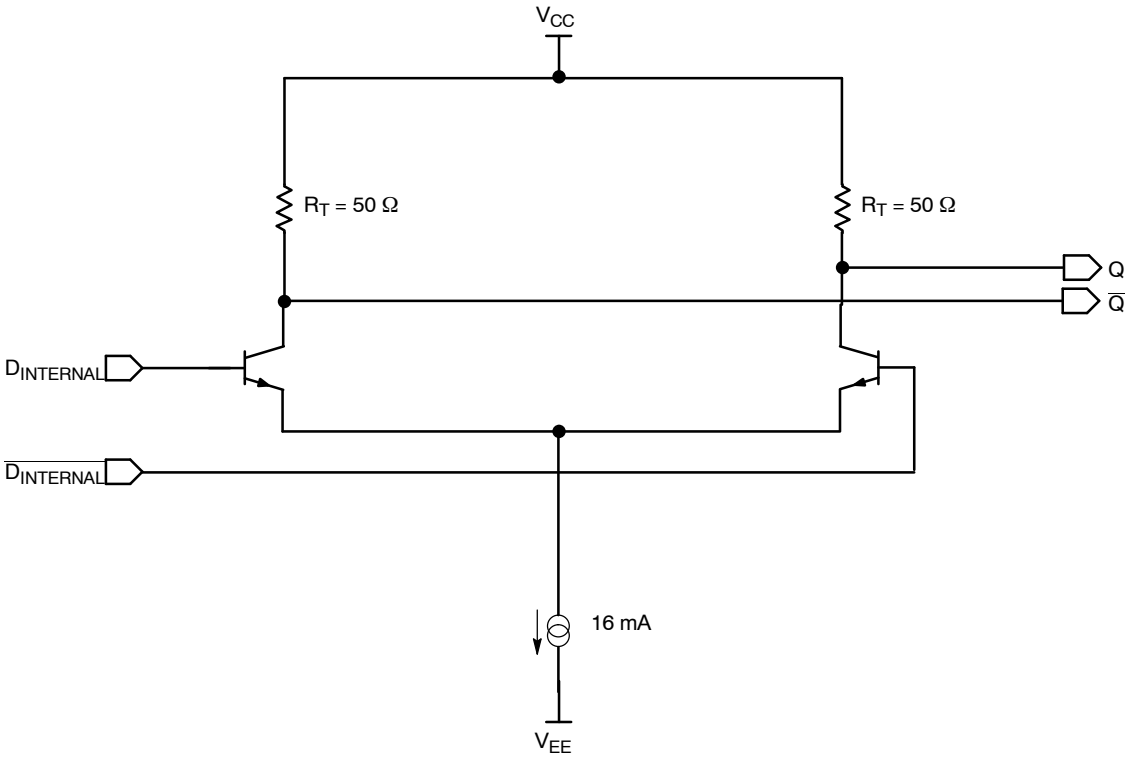


Figure 3. Output Structure

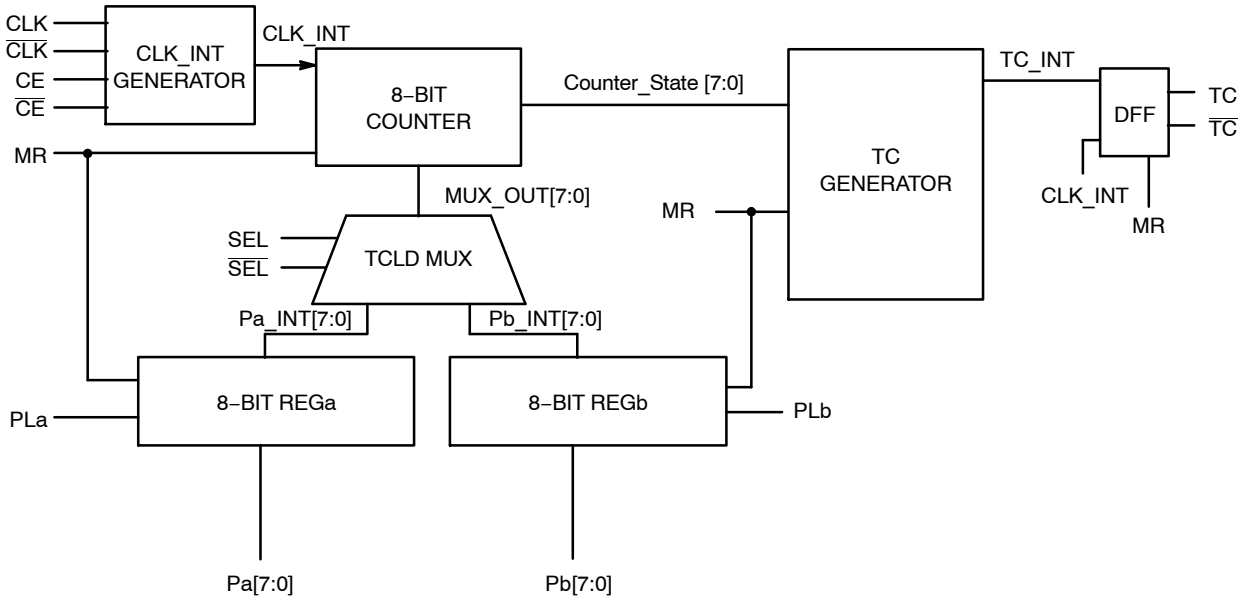


Figure 4. Block Diagram

Table 6. Interface Options

CLK INPUT interfacing options	CLK INPUT INTERFACING OPTIONS
CML	Connect VTCLK and $\overline{\text{VTCLK}}$ to V_{CC}
LVDS	Connect VTCLK and $\overline{\text{VTCLK}}$ together
AC-COUPLED	Bias VTCLK and $\overline{\text{VTCLK}}$ Inputs within (VIHCMR) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques or connect VTCLK and $\overline{\text{VTCLK}}$ to V_{TT}
LVTTL, LVCMOS	An Entered Voltage Should be Applied to the unused Complementary Differential Input. Nominal Voltage is 1.5 V for LVTTL and $V_{CC}/2$ for LVCMOS Inputs.

Table 7. ATTRIBUTES

Characteristic	Value
Internal Input Pulldown Resistor (MR, PLa, PLb)	75 k to V_{EE}
Internal Input Pullup Resistor (Pa[0:7], Pb[0:7])	75 k to V_{CC}
ESD Protection Human Body Model Machine Model Charged Device Model	 > 500 V > 10 V > 2 kV
Moisture Sensitivity (Note 1)	Pb-Free Pkg
QFN−52	Level 2
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	1914
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 8. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		-3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 -3.6	V
V_{INPP}	Differential Input Voltage |CLK – $\overline{CLK}$|	$V_{CC} - V_{EE} \ge 2.8$ V		2.8 V	V
I_{in}	Input Current through R_T (50 Ω Resistor)	Continuous Surge		25 50	mA
I_{out}	Output Current	Continuous Surge		25 50	mA
I_{BB}	V_{BB} Sink/Source			±0.5	mA
T_A	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 1)	0 lfpm 500 lfpm	QFN–52	25 – 32 20 – 27	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P (Note 1)	QFN–52	4 – 15	°C/W
T_{sol}	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 9. DC CHARACTERISTICS, POSITIVE CML OUTPUT (V_{CC} = 3.0 V to 3.465 V; V_{EE} = 0 V (Note 3))

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Positive Power Supply Current	170	200	230	170	200	230	170	200	230	mA
V_{OH}	Output HIGH Voltage (Note 4)	V_{CC} –40	V_{CC} –10	V_{CC}	V_{CC} –40	V_{CC} –10	V_{CC}	V_{CC} –40	V_{CC} –10	V_{CC}	mV
V_{OL}	Output LOW Voltage (Note 4)		V_{CC} –400	V_{CC} –330		V_{CC} –400	V_{CC} –330		V_{CC} –400	V_{CC} –330	mV
DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (Figures 19, 21) (Note 5)											
V_{th}	Input Threshold Reference Voltage Range (Note 1)	800		V_{CC} –75	800		V_{CC} –75	800		V_{CC} –75	mV
V_{IH}	Single-Ended Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Single-Ended Input LOW Voltage	V_{EE}		V_{CC} –150	V_{EE}		V_{CC} –150	V_{EE}		V_{CC} –150	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)	150		2500	150		2500	150		2500	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 20, 22) (Note 6)											
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{CC} –100	V_{EE}		V_{CC} –100	V_{EE}		V_{CC} –100	mV
V_{CMR}	Input Common Mode Range (Differential Cross-Point Voltage) (Note 2)	800		V_{CC} –50	800		V_{CC} –50	800		V_{CC} –50	mV
V_{ID}	Differential Input Voltage	100		2500	100		2500	100		2500	mV
V_{BB}	Output Voltage Reference @ –100 μA	1840	1970	2100	1840	1960	2100	1820	1970	2100	mV
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
R_{TOUT}	Internal Output Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current CLK, CE, SEL MR, PLa, PLb Pa[0:7], Pb[0:7]	 0 0 –50	 7 30 –10	 15 60 0	 0 0 –50	 7 30 –10	 15 60 0	 0 0 –50	 7 30 –10	 15 60 0	μA
I_{IL}	Input LOW Current CLK, CE, SEL MR, PLa, PLb Pa[0:7], Pb[0:7]	 –0.5 0 –50	 20 –20	 0.5 60 0	 –0.5 0 –50	 20 –20	 0.5 60 0	 –0.5 0 –50	 20 –20	 0.5 60 0	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL})/2$.
2. V_{CMR} minimum varies 1:1 with V_{EE}, V_{CMR} maximum varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.
3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to –0.165 V.
4. All loading with 50 Ω to V_{CC}.
5. V_{th}, V_{IH}, V_{IL} and V_{ISE} parameters must be complied with simultaneously.
6. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.

Table 10. DC CHARACTERISTICS, NEGATIVE CML OUTPUT (V_{CC} = 0 V; V_{EE} = −3.465 V to −3.0 V (Note 3))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Positive Power Supply Current	170	200	230	170	200	230	170	200	230	mA
V_{OH}	Output HIGH Voltage (Note 4)	V_{CC} −40	V_{CC} −10	V_{CC}	V_{CC} −40	V_{CC} −10	V_{CC}	V_{CC} −40	V_{CC} −10	V_{CC}	mV
V_{OL}	Output LOW Voltage (Note 4)		V_{CC} −400	V_{CC} −330		V_{CC} −400	V_{CC} −330		V_{CC} −400	V_{CC} −330	mV
DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (Figures 19, 21) (Note 5)											
V_{th}	Input Threshold Reference Voltage Range (Note 1)	V_{EE} +800		V_{CC} −75	V_{EE} +800		V_{CC} −75	V_{EE} +800		V_{CC} −75	mV
V_{IH}	Single-Ended Input HIGH Voltage	V_{EE} +1200		V_{CC}	V_{EE} +1200		V_{CC}	V_{EE} +1200		V_{CC}	mV
V_{IL}	Single-Ended Input LOW Voltage	V_{EE}		V_{CC} −150	V_{EE}		V_{CC} −150	V_{EE}		V_{CC} −150	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)	150		2500	150		2500	150		2500	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 20, 22) (Note 6)											
V_{IHD}	Differential Input HIGH Voltage	V_{EE} +1200		V_{CC}	V_{EE} +1200		V_{CC}	V_{EE} +1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{CC} −100	V_{EE}		V_{CC} −100	V_{EE}		V_{CC} −100	mV
V_{CMR}	Input Common Mode Range (Differential Cross-Point Voltage) (Note 2)	V_{EE} +800		V_{CC} −50	V_{EE} +800		V_{CC} −50	V_{EE} +800		V_C −50	mV
V_{ID}	Differential Input Voltage	100		2500	100		2500	100		2500	mV
V_{BB}	Output Voltage Reference @ −100 μA	−1460	−1330	−1200	−1460	−1330	−1200	−1460	−1330	−1200	mV
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
R_{TOUT}	Internal Output Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current CLK, CE, SEL MR, PLa, PLb Pa[0:7], Pb[0:7]	 0 0 −50	 7 30 −10	 15 60 0	 0 0 −50	 7 30 −10	 15 60 0	 0 0 −50	 7 30 −10	 15 60 0	μA
I_{IL}	Input LOW Current CLK, CE, SEL MR, PLa, PLb Pa[0:7], Pb[0:7]	 −0.5 0 −50	 20 −20	 0.5 60 0	 −0.5 0 −50	 20 −20	 0.5 60 0	 −0.5 0 −50	 20 −20	 0.5 60 0	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL})/2$.
2. V_{CMR} minimum varies 1:1 with V_{EE}, V_{CMR} maximum varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.
3. Input and output parameters vary 1:1 with V_{CC}.
4. All loading with 50 Ω to V_{CC}.
5. V_{th}, V_{IH}, V_{IL} and V_{ISE} parameters must be complied with simultaneously.
6. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.

Table 11. AC CHARACTERISTICS (V_{CC} = 0 V; V_{EE} = −3.465 V to −3.0 V or V_{CC} = 3.0 V to 3.465 V; V_{EE} = 0 V (Note 1))

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OUTPP}	Output Voltage Amplitude @ ÷ 2 Mode f_{in} = 3.5 GHz (See Figure 5)	300	400		300	400		300	400		mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	CLK to TC	435		555	455		575	475		595	
	MR to TC	100		500	100		500	100		500	
t_{JITTER}	RMS Random Clock Jitter (See Figure 5) f_{in} = 3.5 GHz			2.5			3.0			3.0	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 2)	100		2500	100		2500	100		2500	mV
t_r t_f	Output Rise/Fall Times (20% − 80%)	25	45	65	25	45	65	25	45	65	ps
t_s	Setup Time (Figure 23)										ps
	Pa[7:0] to PLa	3750	2500		3750	2500		3750	2500		
	Pb[7:0] to PLb	4500	2000		4500	2000		4500	2000		
	CE to CLK	400	30		400	30		400	30		
	SEL to CLK	300	120		300	120		300	120		
	PLa to CLK	2500	2000		2500	2000		2500	2000		
	PLb to CLK	3250	2750		3250	2750		3250	2750		
	Pa[7:0] to CLK	4750	3500		4750	3500		4750	3500		
	Pb[7:0] to CLK	3000	2500		3000	2500		3000	2500		
t_H	Hold Time (Figure 23)										ps
	PLa to Pa[7:0]	−1500	−2700		−1500	−2700		−1500	−2700		
	PLb to Pb[7:0]	−1250	−1900		−1250	−1900		−1250	−1900		
	CLK to CE	450	40		450	40		450	40		
	CLK to SEL	0	−110		0	−110		0	−110		
	CLK to PLa	−1750	−1900		−1750	−1900		−1750	−1900		
	CLK to PLb	−2250	−2700		−2250	−2700		−2250	−2700		
	CLK to PLb[7:0]	−2250	−3200		−2250	−3200		−2250	−3200		
	CLK to PLb[7:0]	−2000	−2500		−2000	−2500		−2000	−2500		
t_{SKEW}	Device-to-Device (Note 3)		40	75		40	75		40	75	ps
t_{PW}	Minimum Pulse Width MR	250	85		250	85		250	85		ps
t_{RR}	Reset Recovery MR to CLK/$\overline{CLK}$	3000	2500		3000	2500		3000	2500		ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Measured using a 400 mV source, 50% duty cycle clock source at f_{in} = 1 GHz unless stated otherwise. All loading with 50 Ω to V_{CC}. Input edge rates 40 ps (20% − 80%).
2. V_{INPP} (MAX) cannot exceed V_{CC} − V_{EE}.
3. Device-to-Device skew for identical transitions at identical V_{CC} levels.

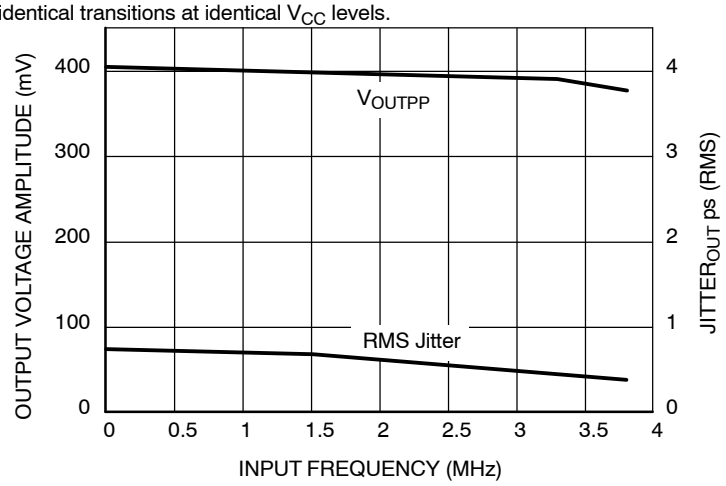


Figure 5. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) @ Ambient Temperature (Typical)

Application Information

The differential inputs can accepts LVPECL, CML, LVDS, LVCMOS and LVTTL signal levels. The differential input amplitude range is from 100 mV to 2500 mV, where the input high voltage, VIH, can range from 1.2 V to VCC; see DC Characteristics Table 9. Examples of input interfaces are illustrated below in a 50 Ω environment (Z = 50 Ω)

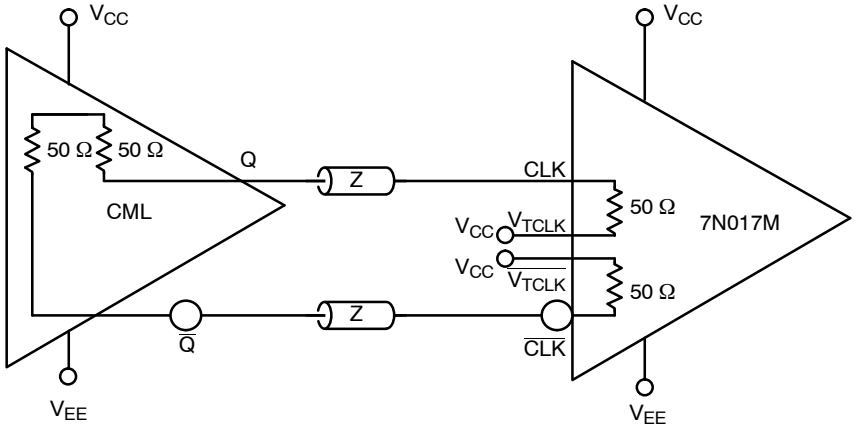
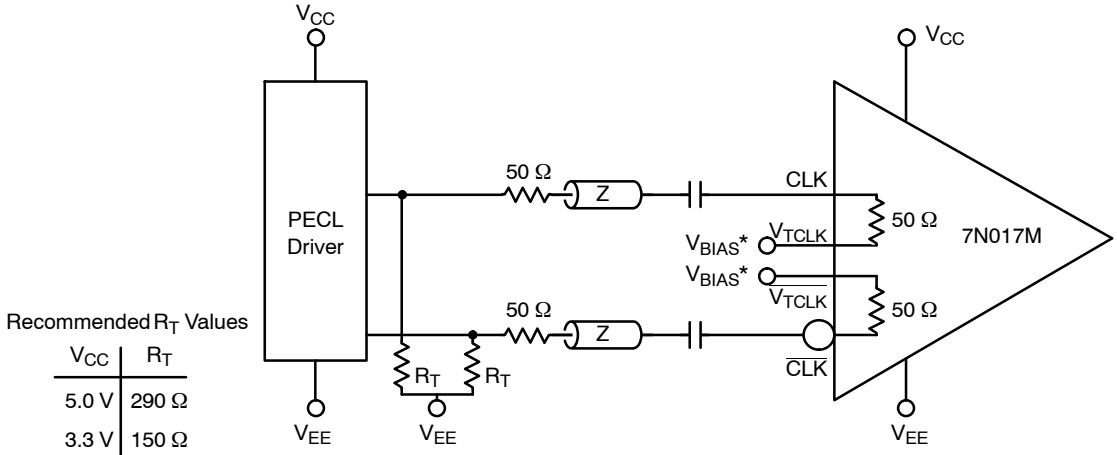


Figure 6. CML Interface



Recommended R_T Values

V_{CC}	R_T
5.0 V	290 Ω
3.3 V	150 Ω
2.5 V	80 Ω

Figure 7. PECL Capacitor-Coupled Interface

*V_{BIAS} is within V_{CMR} Range.

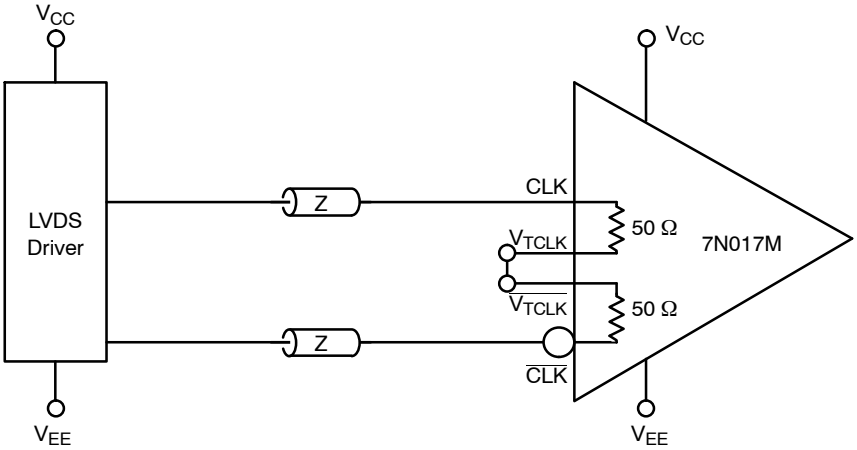


Figure 8. LVDS Interface

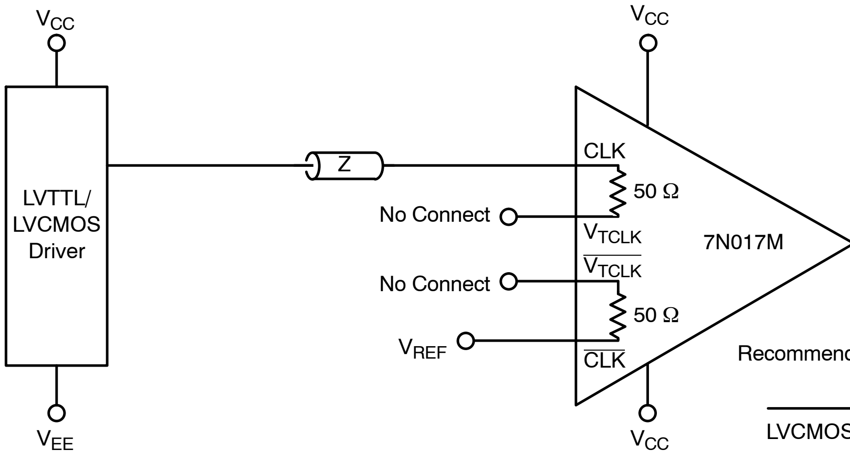


Figure 9. LVCMOS/LVTTL Interface

Recommended V_{REF} Values

	V_{REF}
LVCMOS	$\frac{V_{CC} - V_{EE}}{2}$
LVTTL	1.5 V

Table 12. OPERATION TABLE

MR	Pa	PLa	Pb	PLb	SEL	CE	CLK	CLK_INT	TC_INT	TC
1	XXXXXXXX	x	XXXXXXXX	X	X	X	X	X	X	X
0	00000101	H	00000100	H	X	H	L	H	H	H
0	00000101	H	00000100	H	X	H	L	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	L	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	L	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X

X – Don't Care
H – HIGH
L – LOW

Table 12. OPERATION TABLE

MR	Pa	PLa	Pb	PLb	SEL	CE	CLK	CLK_INT	TC_INT	TC
0	XXXXXXXX	L	XXXXXXXX	L	H	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	H	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	L	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	L	L	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	L	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	L	L	L	X	X
0	00000010	H	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	00000001	H	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	H	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	L	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	L	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	L	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	L	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	L	H	H	H	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	L	L	X	X
0	XXXXXXXX	L	XXXXXXXX	L	X	H	H	H	X	X

X – Don’t Care
H – HIGH
L – LOW

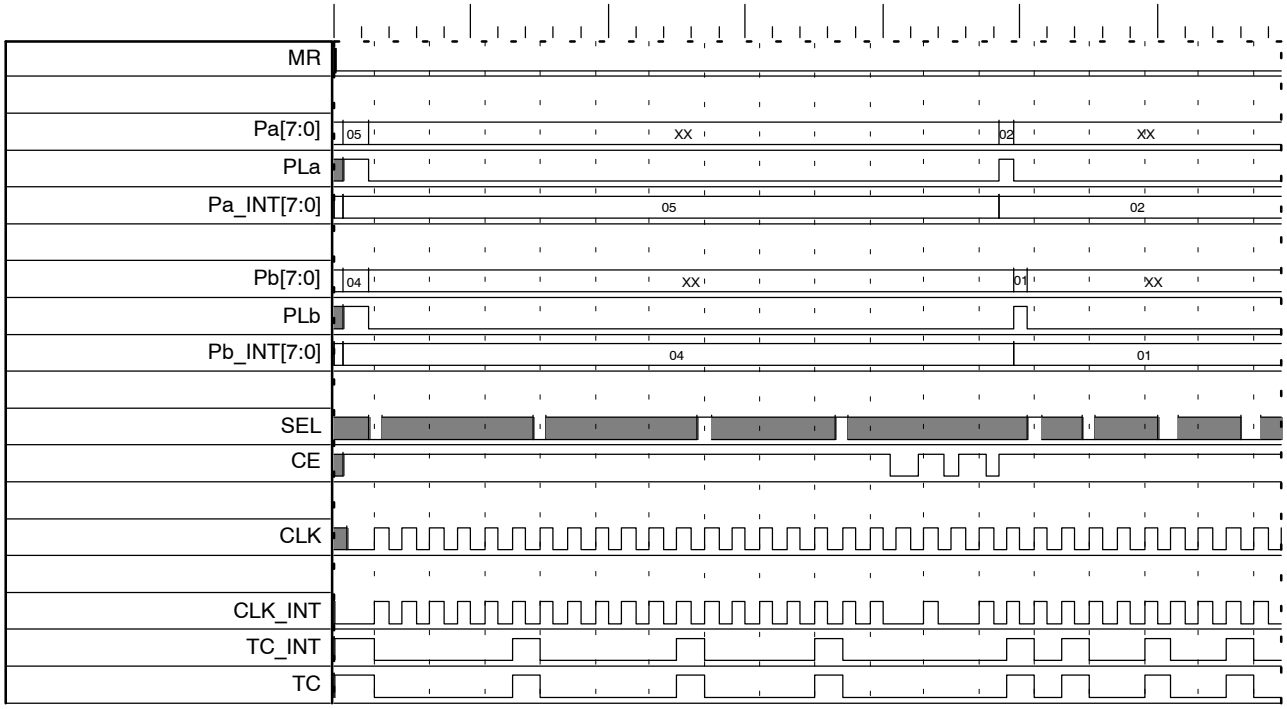


Figure 10. Device Timing Diagram for Table 12

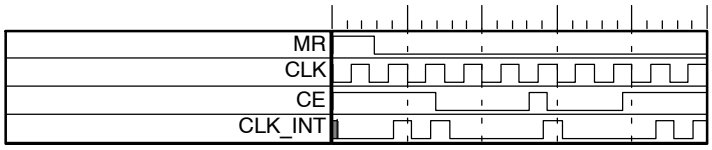


Figure 11. Timing Diagram for CE Input

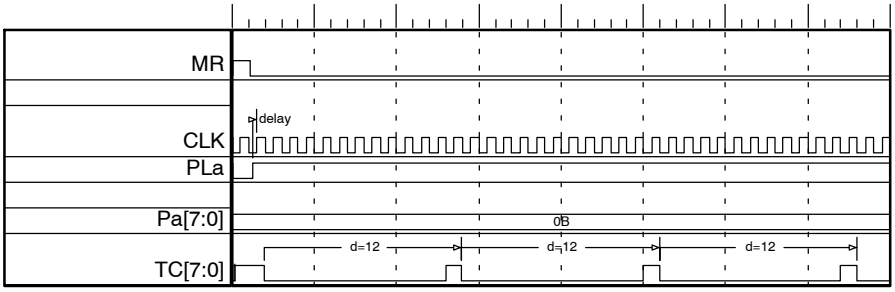


Figure 12. Timing Diagram for PLa / PLb Inputs (SEL is Low)

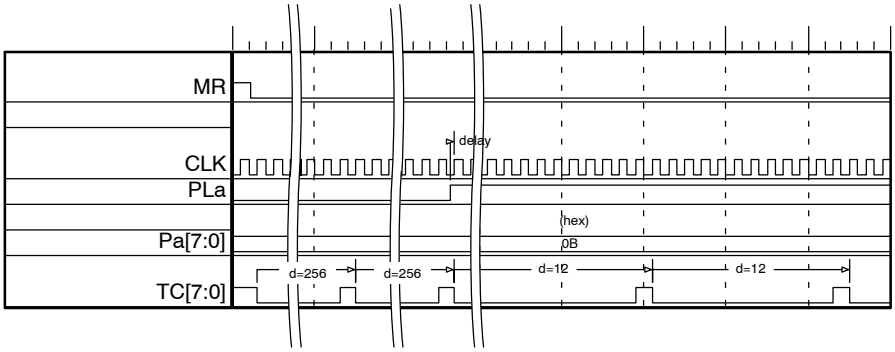


Figure 13. Timing Diagram for PLa / PLb Inputs (Before Critical Rising Edge of CLK) (SEL is Low)

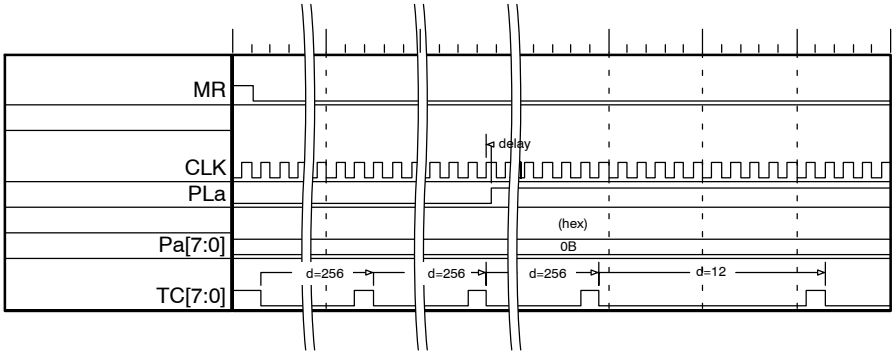


Figure 14. Timing Diagram for PLa / PLb Inputs (After Critical Rising Edge of CLK) (SEL is Low)

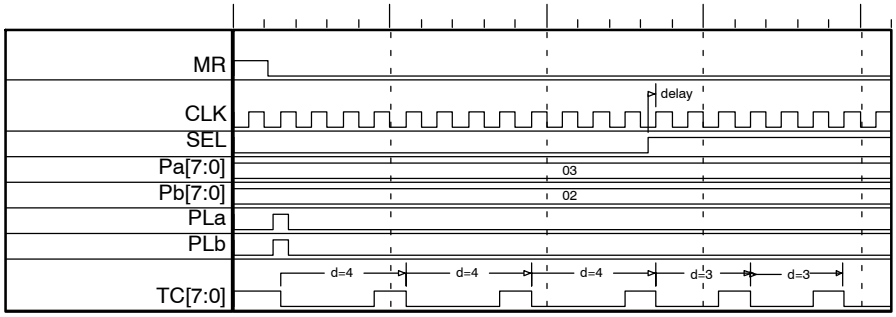


Figure 15. Timing Diagram for SEL Input (Before Critical Rising Edge of CLK)

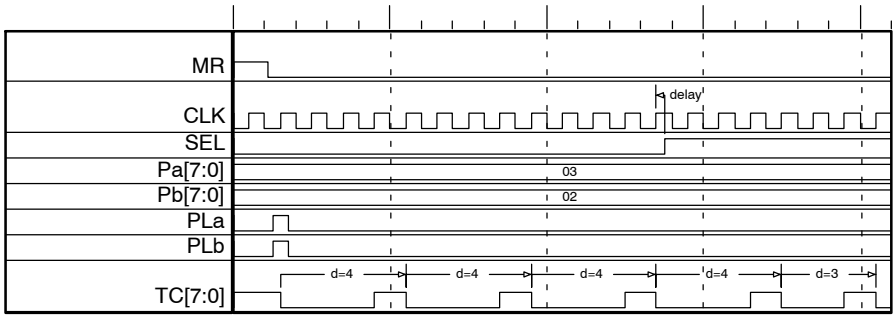


Figure 16. Timing Diagram for SEL Input (After Critical Rising Edge of CLK)

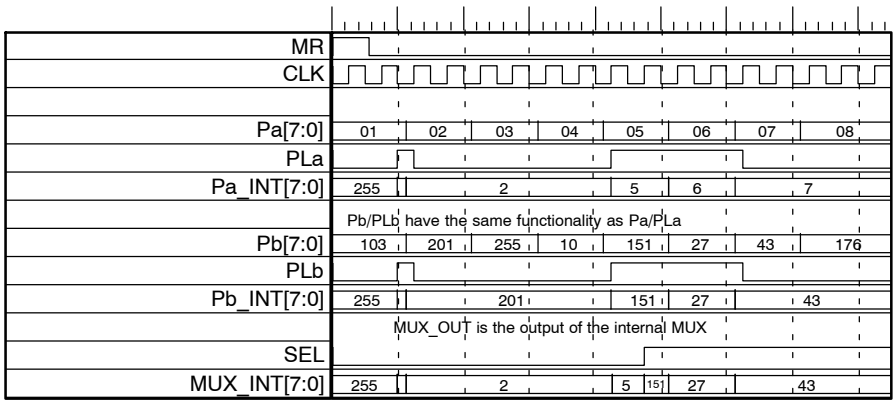


Figure 17. Timing Diagram Relating PLa, PLb, Pa(0:7), Pb(0:7)

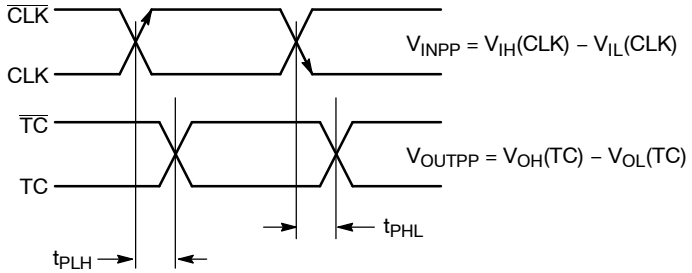


Figure 18. AC Reference Measurement

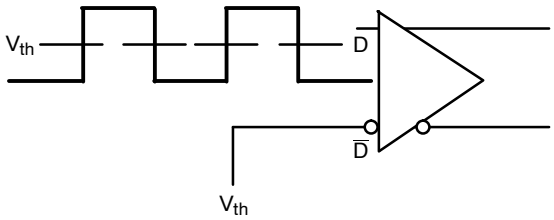


Figure 19. Differential Input Driven Single-Ended

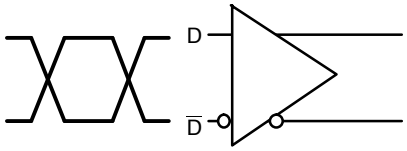


Figure 20. Differential Inputs Driven Differentially

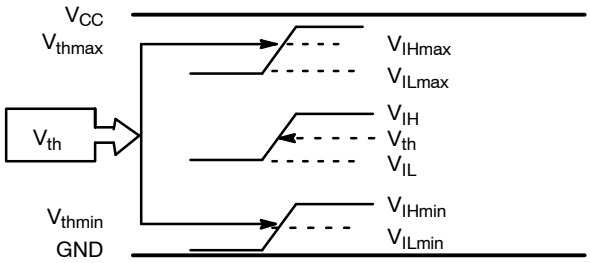


Figure 21. V_{th} Diagram

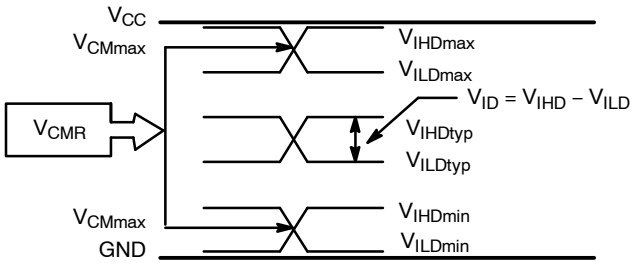


Figure 22. V_{CMR} Diagram

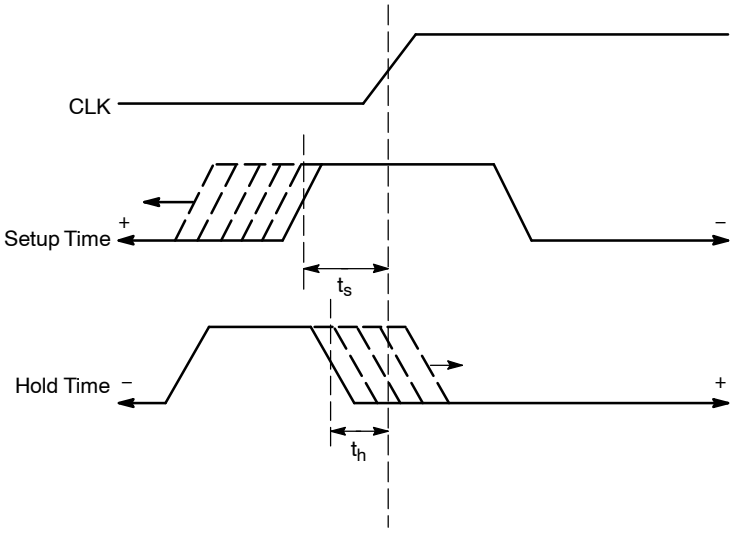


Figure 23. Setup and Hold Time

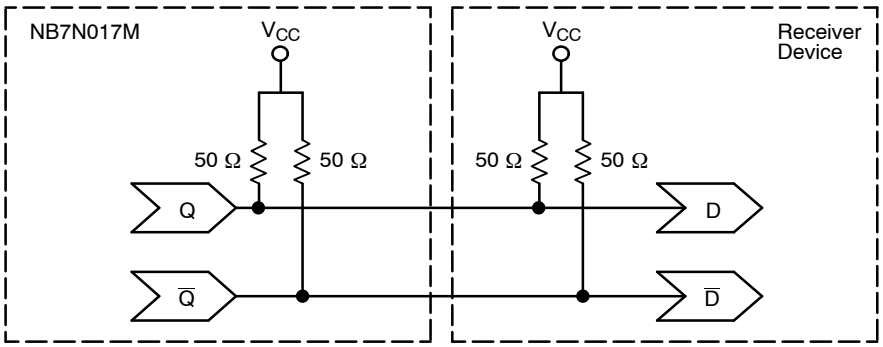
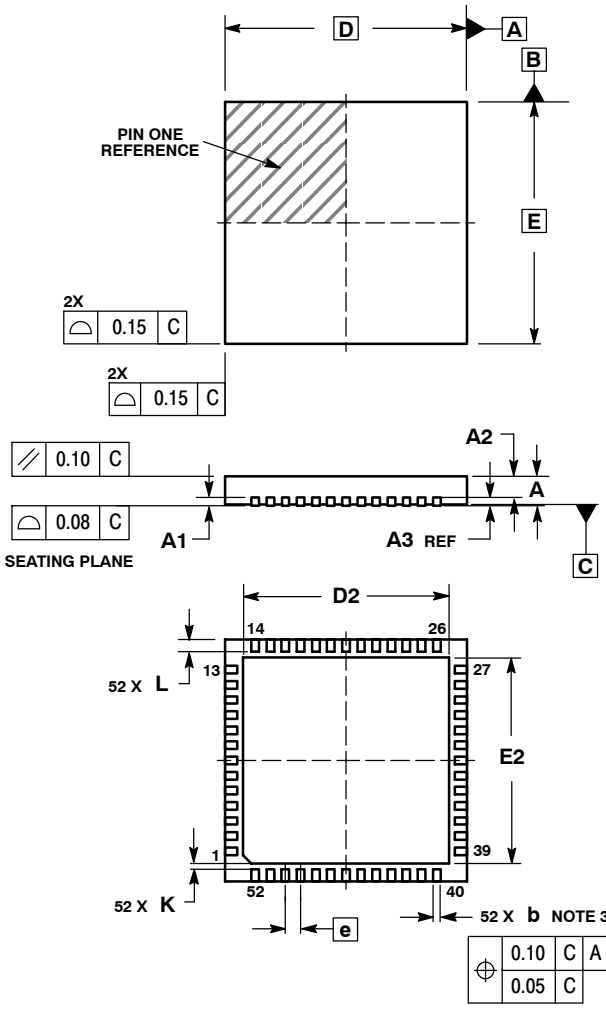


Figure 24. Typical Termination for 16 mA Output Drive and Device Evaluation

PACKAGE DIMENSIONS

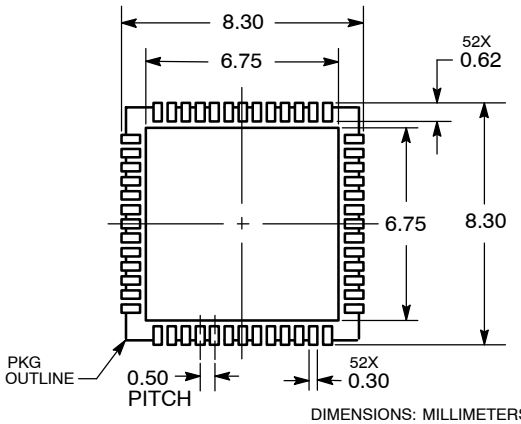
QFN−52 8x8, 0.5P
CASE 485M−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.18	0.30
D	8.00 BSC	
D2	6.50	6.80
E	8.00 BSC	
E2	6.50	6.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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