

TinyLogic UHS Inverter, Open Drain Output

NC7SZ05

Description

The NC7SZ05 is a single inverter with open drain output stage from ON Semiconductor's Ultra-High Speed series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} operating range. The inputs and output are high-impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V, independent of V_{CC} when in the high-impedance state.

Features

- Ultra-High Speed: $t_{PD} = 1.9$ ns (Typical) into 50 pF at 5 V V_{CC}
- Open Drain Output for OR Tied Applications
- High Output Drive: ± 24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Matches Performance of LCX Operated at 3.3 V V_{CC}
- Power Down High-Impedance Inputs / Outputs
- Over-Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise / EMI Reduction Circuitry Implemented
- Ultra-Small MicroPak™ Packages
- Space-Saving SC-74A and SC-88A Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

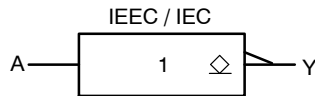


Figure 1. Logic Symbol



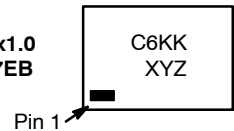
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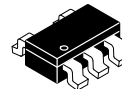
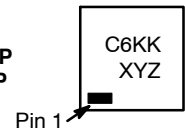
MARKING DIAGRAMS



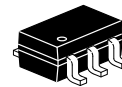
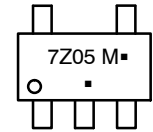
SIP6 1.45x1.0
CASE 127EB



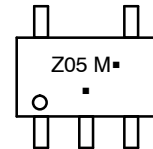
UDFN6
1.0X1.0, 0.35P
CASE 517DP



SC-74A
CASE 318BQ



SC-88A
CASE 419A-02



C6, 7Z05, Z05 = Specific Device Code
 KK = 2-Digit Lot Run Traceability Code
 XY = 2-Digit Date Code Format
 Z = Assembly Plant Code
 XX = Device Code
 M = Date Code*
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NC7SZ05

Pin Configurations

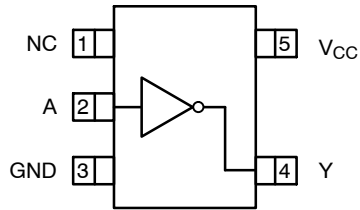


Figure 2. SC-88A and SC-74A (Top View)

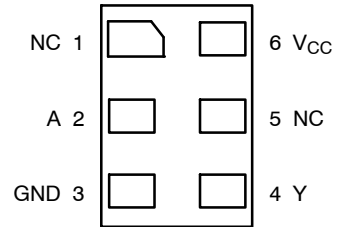


Figure 3. MicroPak (Top Through View)

PIN DEFINITIONS

| Pin # SC-88A / SC74-A | Pin # MicroPak | Name | Description |
|-----------------------|----------------|-----------------|----------------|
| 1 | 1, 5 | NC | No Connect |
| 2 | 2 | A | Input |
| 3 | 3 | GND | Ground |
| 4 | 4 | Y | Output |
| 5 | 6 | V _{CC} | Supply Voltage |

FUNCTION TABLE

| Inputs | Output |
|--------|--------|
| A | Y |
| L | *H |
| H | L |

H = HIGH Logic Level

L = LOW Logic Level

*H = High Impedance Output State, Open Drain

NC7SZ05

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Min | Max | Unit |
|-------------------------------------|---|------------------------|------|------|------|
| V _{CC} | Supply Voltage | | -0.5 | 6.5 | V |
| V _{IN} | DC Input Voltage | | -0.5 | 6.5 | V |
| V _{OUT} | DC Output Voltage | | -0.5 | 6.5 | V |
| I _{IK} | DC Input Diode Current | V _{IN} < 0 V | - | -50 | mA |
| I _{OK} | DC Output Diode Current | V _{OUT} < 0 V | - | -50 | mA |
| I _{OUT} | DC Output Current | | - | ±50 | mA |
| I _{CC} or I _{GND} | DC V _{CC} or Ground Current | | - | ±50 | mA |
| T _{STG} | Storage Temperature Range | | -65 | +150 | °C |
| T _J | Junction Temperature Under Bias | | - | +150 | °C |
| T _L | Junction Lead Temperature (Soldering, 10 Seconds) | | - | +260 | °C |
| P _D | Power Dissipation in Still Air | SC-74A | - | 390 | mW |
| | | SC-88A | - | 332 | |
| | | MicroPak-6 | - | 812 | |
| | | MicroPak2™-6 | - | 812 | |
| ESD | Human Body Model, JEDEC: JESD22-A114 | | - | 4000 | V |
| | Charge Device Model, JEDEC: JESD22-C101 | | - | 2000 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------------------|-------------------------------|--|------|------|------|
| V _{CC} | Supply Voltage Operating | | 1.65 | 5.50 | V |
| | Supply Voltage Data Retention | | 1.50 | 5.50 | |
| V _{IN} | Input Voltage | | 0 | 5.5 | V |
| V _{OUT} | Output Voltage | | 0 | 5.5 | V |
| T _A | Operating Temperature | | -40 | +85 | °C |
| t _r , t _f | Input Rise and Fall Times | V _{CC} at 1.8 V, 2.5 V ±0.2 V | 0 | 20 | ns/V |
| | | V _{CC} at 3.3 V ±0.3 V | 0 | 10 | |
| | | V _{CC} at 5.0 V ±0.5 V | 0 | 5 | |
| θ _{JA} | Thermal Resistance | SC-74A | - | 320 | °C/W |
| | | SC-88A | - | 377 | |
| | | MicroPak-6 | - | 154 | |
| | | MicroPak2-6 | - | 154 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

- Unused inputs must be held HIGH or LOW. They may not float.

NC7SZ05

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | | T _A = -40 to +85°C | | Unit |
|------------------|-----------------------------------|---------------------|---|------------------------|------|----------------------|-------------------------------|----------------------|------|
| | | | | Min | Typ | Max | Min | Max | |
| V _{IH} | HIGH Level Input Voltage | 1.65 to 1.95 | | 0.65 V _{CC} | - | - | 0.65 V _{CC} | - | V |
| | | 2.30 to 5.50 | | 0.70 V _{CC} | - | - | 0.70 V _{CC} | - | |
| V _{IL} | LOW Level Input Voltage | 1.65 to 1.95 | | - | - | 0.35 V _{CC} | - | 0.35 V _{CC} | V |
| | | 2.30 to 5.50 | | - | - | 0.30 V _{CC} | - | 0.30 V _{CC} | |
| I _{LKG} | HIGH Level Output Leakage Current | 1.65 to 5.50 | V _{IN} = V _{IH} or V _{IL} , V _{OUT} = V _{CC} or GND | - | - | ±5 | - | ±10 | µA |
| V _{OL} | LOW Level Output Voltage | 1.65 | V _{IN} = V _{IH} or V _{IL} , I _{OL} = 100 µA | - | 0.00 | 0.10 | - | 0.10 | V |
| | | 1.80 | | - | 0.00 | 0.10 | - | 0.10 | |
| | | 2.30 | | - | 0.00 | 0.10 | - | 0.10 | |
| | | 3.00 | | - | 0.00 | 0.10 | - | 0.10 | |
| | | 4.50 | | - | 0.00 | 0.10 | - | 0.10 | |
| | | 1.65 | I _{OL} = 4 mA | - | 0.80 | 0.24 | - | 0.24 | |
| | | 2.30 | I _{OL} = 8 mA | - | 0.10 | 0.30 | - | 0.30 | |
| | | 3.00 | I _{OL} = 16 mA | - | 0.15 | 0.40 | - | 0.40 | |
| | | 3.00 | I _{OL} = 24 mA | - | 0.22 | 0.55 | - | 0.55 | |
| | | 4.50 | I _{OL} = 32 mA | - | 0.22 | 0.55 | - | 0.55 | |
| I _{IN} | Input Leakage Current | 1.65 to 5.5 | 0 ≤ V _{IN} ≤ 5.5 V | - | - | ±1 | - | ±10 | µA |
| I _{OFF} | Power Off Leakage Current | 0 | V _{IN} or V _{OUT} = 5.5 V | - | - | 1 | - | 10 | µA |
| I _{CC} | Quiescent Supply Current | 1.65 to 5.50 | V _{IN} = 5.5 V, GND | - | - | 2 | - | 20 | µA |

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | | T _A = -40 to +85°C | | Unit |
|------------------|--|---------------------|--|------------------------|-----|------|-------------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | |
| t _{PZL} | Propagation Delay (Figure 4, 5) | 1.65 | C _L = 50 pF, R _U = 500 Ω, R _D = 500 Ω, V _{IN} = 2 · V _{CC} | - | 5.5 | 12.9 | - | 13.4 | ns |
| | | 1.80 | | - | 4.6 | 10.5 | - | 11.0 | |
| | | 2.50 ±0.20 | | - | 3.0 | 7.0 | - | 7.5 | |
| | | 3.30 ±0.30 | | - | 2.4 | 5.0 | - | 5.2 | |
| | | 5.00 ±0.50 | | - | 1.9 | 4.3 | - | 4.5 | |
| t _{PLZ} | | 1.65 | C _L = 50 pF, R _U = 500 Ω, R _D = 500 Ω, V _{IN} = 2 · V _{CC} | - | 5.0 | 12.9 | - | 13.4 | ns |
| | | 1.80 | | - | 4.1 | 10.5 | - | 11.0 | |
| | | 2.50 ±0.20 | | - | 2.5 | 7.0 | - | 7.5 | |
| | | 3.30 ±0.30 | | - | 2.1 | 5.0 | - | 5.2 | |
| | | 5.00 ±0.50 | | - | 1.2 | 4.3 | - | 4.5 | |
| C _{IN} | Input Capacitance | 0.00 | | - | 4.0 | - | - | - | pF |
| C _{OUT} | Output Capacitance | 0.00 | | - | 6.0 | - | - | - | pF |
| C _{PD} | Power Dissipation Capacitance (Note 2) (Figure 6) | 3.30 | | - | 3.6 | - | - | - | pF |
| | | 5.00 | | - | 6.5 | - | - | - | |

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression:
I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CC}static).

NC7SZ05

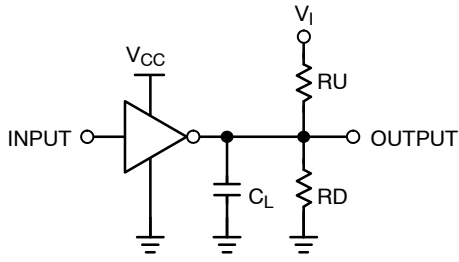


Figure 4. AC Test Circuit

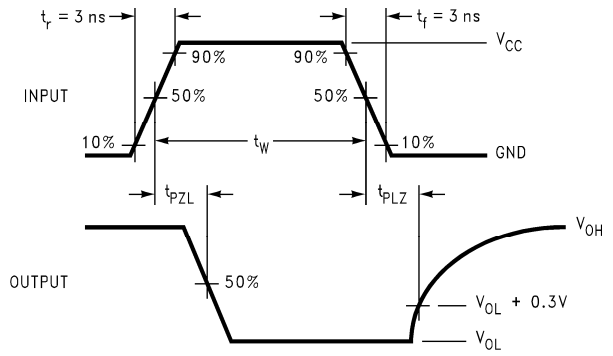
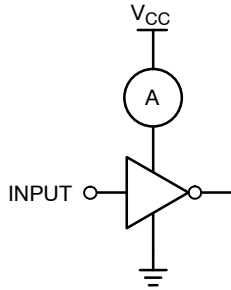


Figure 5. AC Waveforms



NOTE:
3. Input = AC Waveform; $t_r = t_f = 1.8$ ns;
PRR = 10 MHz; Duty Cycle = 50%.

Figure 6. Test Circuit

DEVICE ORDERING INFORMATION

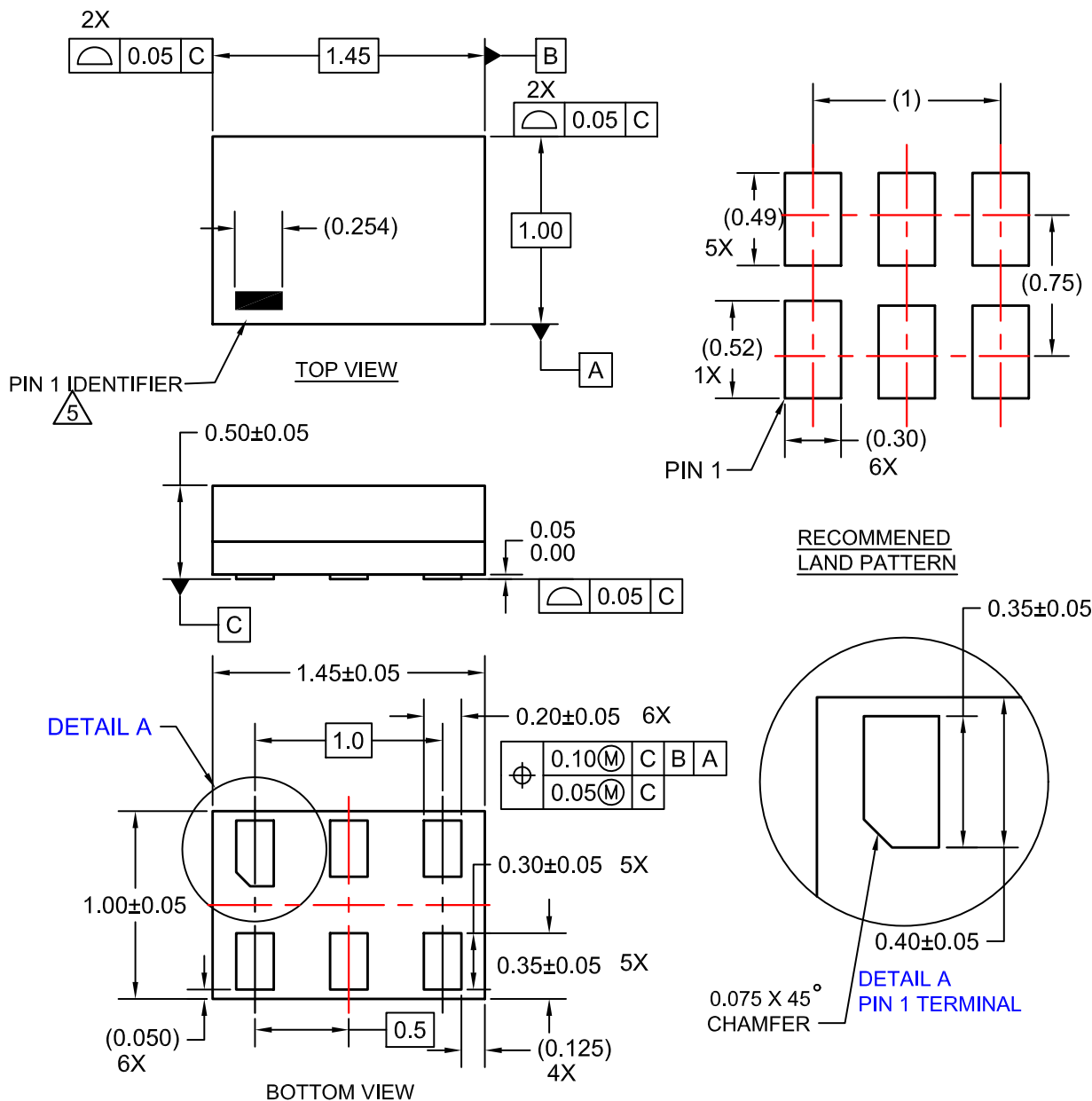
| Device | Top Mark | Packages | Shipping† |
|------------|----------|---|--------------------|
| NC7SZ05M5X | 7Z05 | 5-Lead SC-74A, 1.6mm | 3000 / Tape & Reel |
| NC7SZ05P5X | Z05 | 5-Lead SC70, EIAJ SC-88A, 1.25 mm Wide | 3000 / Tape & Reel |
| NC7SZ05L6X | C6 | 6-Lead MicroPak, 1.00 mm Wide | 5000 / Tape & Reel |
| NC7SZ05FHX | C6 | 6-Lead, MicroPak2, 1 x 1 mm Body, 0.35 mm Pitch | 5000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

SC-74A CASE 318BQ ISSUE B

DATE 18 JAN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.90 | 1.10 |
| A1 | 0.01 | 0.10 |
| b | 0.25 | 0.50 |
| c | 0.10 | 0.26 |
| D | 2.85 | 3.15 |
| E | 2.50 | 3.00 |
| E1 | 1.35 | 1.65 |
| e | 0.95 BSC | |
| L | 0.20 | 0.60 |
| M | 0° | 10° |

RECOMMENDED SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE L

DATE 17 JAN 2013



SOLDER FOOTPRINT



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

- | | | | | |
|--|--|--|--|--|
| <p>STYLE 1: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR</p> | <p>STYLE 2: PIN 1. ANODE 2. EMITTER 3. BASE 4. COLLECTOR 5. CATHODE</p> | <p>STYLE 3: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. CATHODE 1</p> | <p>STYLE 4: PIN 1. SOURCE 1 2. DRAIN 1/2 3. SOURCE 1 4. GATE 1 5. GATE 2</p> | <p>STYLE 5: PIN 1. CATHODE 2. COMMON ANODE 3. CATHODE 2 4. CATHODE 3 5. CATHODE 4</p> |
| <p>STYLE 6: PIN 1. EMITTER 2 2. BASE 2 3. EMITTER 1 4. COLLECTOR 5. COLLECTOR 2/BASE 1</p> | <p>STYLE 7: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR</p> | <p>STYLE 8: PIN 1. CATHODE 2. COLLECTOR 3. N/C 4. BASE 5. EMITTER</p> | <p>STYLE 9: PIN 1. ANODE 2. CATHODE 3. ANODE 4. ANODE 5. ANODE</p> | <p>Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.</p> |

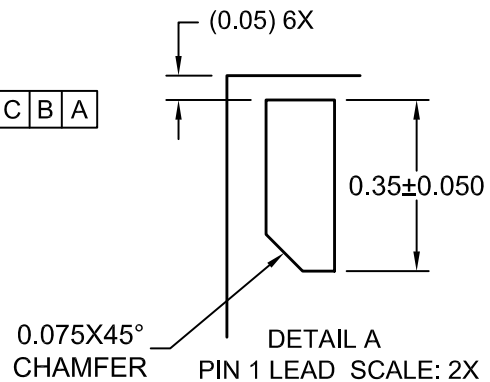
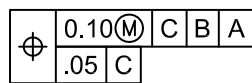
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UDFN6 1.0X1.0, 0.35P
CASE 517DP
ISSUE O

DATE 31 AUG 2016



- NOTES:
- A. COMPLIES TO JEDEC MO-252 STANDARD
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009

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