

TinyLogic UHS D-Type, Flip-Flop with Preset and Clear

NC7SZ74

Description

The NC7SZ74 is a single, D-type, CMOS flip-flop with preset and clear from onsemi ultra high-speed series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive, while maintaining low static power dissipation over a very broad V_{CC} operating range of 1.65 V to 5.5 V V_{CC} . The inputs and outputs are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V, independent of V_{CC} operating voltage.

The signal level applied to the D input is transferred to the Q output during the positive-going transition of the CLK pulse.

Features

- Ultra-High Speed: t_{PD} 2.6 ns (Typical) into 50 pF at 5 V V_{CC}
- High Output Drive: ± 24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Power Down High-Impedance Inputs/Outputs
- Over-Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise/EMI Reduction Circuitry

CONNECTION DIAGRAM

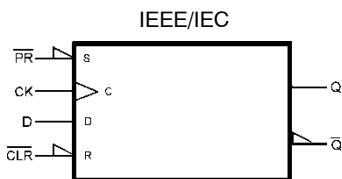
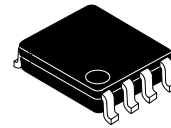
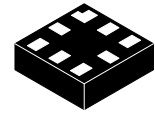


Figure 1. Logic Symbol

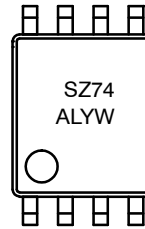


US8
CASE 846AN



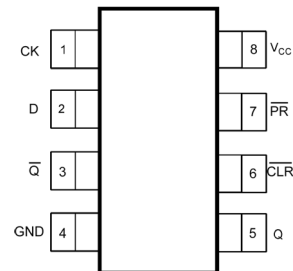
UQFN8
1.6X1.6, 0.5P
CASE 523AY

MARKING DIAGRAMS

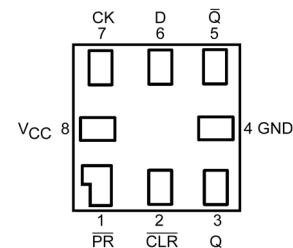


- SZ74, N9 = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Wee
KK = 2-Digit Lot Run Traceability Code
XY = 2-Digit Date Code Format
Z = Assembly Plant Code

PIN CONFIGURATIONS



USB (Top View)



MicroPak™ (Top Through View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

NC7SZ74

PIN DEFINITIONS

Pin # US8	Pin # MicroPak	Name	Description
1	7	CK	Clock Pulse Input
2	6	D	Data Input
3	5	\bar{Q}	Flip-Flop Output
4	4	GND	Ground
5	3	Q	Flip-Flop Output
6	2	\bar{CLR}	Direct Clear Input
7	1	\bar{PR}	Direct Preset Input
8	8	V _{CC}	Supply Voltage

FUNCTION TABLE

Inputs				Output		Function
CLR	PR	D	CK	Q	\bar{Q}	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	
H	H	L	↑	L	H	
H	H	H	↑	H	L	
H	H	X	↓	Q _n	\bar{Q}_n	No Change

H = HIGH Logic Level

Q_n = No change in data

X = Immaterial

↓ = Falling Edge

L = LOW Logic Level

Z = High Impedance

↑ = Rising Edge

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	-0.5	6.5	V
V _{IN}	DC Input Voltage	-0.5	6.5	V
V _{OUT}	DC Output Voltage	-0.5	6.5	V
I _{IK}	DC Input Diode Current	-	-50	mA
I _{OK}	DC Output Diode Current	-	-50	mA
I _{OUT}	DC Output Source/Sink Current	-	±50	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	-	±50	mA
T _{STG}	Storage Temperature Range	-65	+150	°C
T _J	Junction Temperature Under Bias	-	+150	°C
T _L	Junction Lead Temperature (Soldering, 10 Seconds)	-	+260	°C
P _D	Power Dissipation in Still Air	-	500 539	mW
ESD	Human Body Model: JEDEC:JESD22-A114	-	4000	V
	Charge Device Model: JEDEC:JESD22-C101	-	2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NC7SZ74

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.50	5.50	
V _{IN}	Input Voltage		0	5.5	V
V _{OUT}	Output Voltage	Active State	0	V _{CC}	V
		3-State	0	5.5	
t _r , t _f	Input Rise and Fall Times	V _{CC} = 1.8 V, 2.5 V ±0.2 V	0	20	ns/V
		V _{CC} = 3.3 V ±0.3 V	0	10	
		V _{CC} = 5.0 V ±0.5 V	0	5	
T _A	Operating Temperature		-40	+85	°C
θ _{JA}	Thermal Resistance	US8		250	°C/W
		MicroPak-8		232	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NOTE: Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC}	Conditions	T _A = +25°C			T _A = -40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	HIGH Level Control Input Voltage	1.65 to 1.95		0.65 V _{CC}			0.65 V _{CC}		V
		2.30 to 5.50		0.70 V _{CC}			0.70 V _{CC}		
V _{IL}	LOW Level Control Input Voltage	1.65 to 1.95				0.35 V _{CC}		0.35 V _{CC}	V
		2.30 to 5.50				0.30 V _{CC}		0.30 V _{CC}	
V _{OH}	HIGH Level Output Voltage	1.65	V _{IN} = V _{IH} , I _{OH} = -100 μA	1.55	1.65		1.55		V
		2.30		2.20	2.30		2.20		
		3.00		2.90	3.00		2.90		
		4.50		4.40	4.50		4.40		
		1.65	I _{OH} = -4 mA	1.29	1.52		1.29		
		2.30		1.90	2.15		1.90		
		3.00		2.40	2.80		2.40		
		3.00		2.30	2.68		2.30		
4.50	I _{OH} = -32 mA	3.80	4.20		3.80				
V _{OL}	LOW Level Control Output Voltage	1.65	V _{IN} = V _{IH} , I _{OL} = 100 μA			0.10		0.10	V
		2.30				0.10		0.10	
		3.00				0.10		0.10	
		4.50				0.10		0.10	
		1.65	I _{OL} = 4 mA		0.10	0.24		0.24	
		2.30		0.10	0.30		0.30		
		3.00		0.15	0.40		0.40		
		3.00		0.22	0.55		0.55		
		4.50		0.22	0.55		0.55		
		4.50		I _{OL} = 32 mA		0.22	0.55		
I _{IN}	Input Leakage Current	1.65 to 5.5	0 ≤ V _{IN} ≤ 5.5 V			±0.1		±1.0	μA
I _{OFF}	Power Off Leakage Current	0	V _{IN} or V _{OUT} = 5.5 V			1		10	μA
I _{CC}	Quiescent Supply Current	1.65 to 5.50	V _{IN} = 5.5 V, GND			1		10	μA

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AC ELECTRICAL CHARACTERISTICS

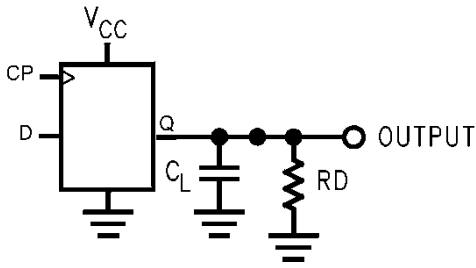
Symbol	Parameter	V _{CC}	Conditions	T _A = +25°C			T _A = -40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
f _{MAX}	Maximum Clock Frequency	1.80 ±0.15	C _L = 15 pF, R _D = 1 MΩ, S ₁ = Open	75			75		ns	Figure 4 Figure 8
		2.50 ±0.20		150			150			
		3.30 ±0.30		200			200			
		5.00 ±0.50		250			250			
		3.30 ±0.50	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	175			175			
		5.00 ±0.50		200			200			
t _{PLH} , t _{PHL}	Propagation Delay CK to Q, \bar{Q}	1.80 ±0.15	C _L = 15 pF, R _D = 1 MΩ, S ₁ = Open		6.5	12.5		13.0	ns	Figure 4 Figure 6
		2.50 ±0.20			3.8	7.5		8.0		
		3.30 ±0.30			2.8	6.5		7.0		
		5.00 ±0.50			2.2	4.5		5.0		
		3.30 ±0.30	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open		3.4	7.0		7.5		
		5.00 ±0.50			2.6	5.0		5.5		
t _{PLH} , t _{PHL}	Propagation Delay CLR, \bar{PR} to Q, \bar{Q}	1.80 ±0.15	C _L = 15 pF, R _L = 1 MΩ, S ₁ = Open		6.5	14.0		14.5	ns	Figure 4 Figure 6
		2.50 ±0.20			3.8	9.0		9.5		
		3.30 ±0.30			2.8	6.5		7.0		
		5.00 ±0.50			2.2	5.0		5.5		
		3.30 ±0.30	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open		3.4	7.0		7.5		
		5.00 ±0.50			2.6	5.0		5.5		
t _S	Setup Time CK to D	1.80 ±0.15	C _L = 15 pF, R _L = 1 MΩ, S ₁ = Open	6.5			6.5		ns	Figure 4 Figure 7
		2.50 ±0.20		3.5			3.5			
		3.30 ±0.30		2.0			2.0			
		5.00 ±0.50		1.5			1.5			
		3.30 ±0.30	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	2.0			2.0			
		5.00 ±0.50		1.5			1.5			
t _H	Hold Time, CK to D	1.80 ±0.15	C _L = 15 pF, R _L = 1 MΩ, S ₁ = Open	0.5			0.5		ns	Figure 4 Figure 7
		2.50 ±0.20		0.5			0.5			
		3.30 ±0.30		0.5			0.5			
		5.00 ±0.50		0.5			0.5			
		3.30 ±0.30	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	0.5			0.5			
		5.00 ±0.50		0.5			0.5			
t _W	Pulse Width, CK, PR, CLR	1.80 ±0.15	C _L = 15 pF, R _L = 1 MΩ, S ₁ = Open	6.0			6.0		ns	Figure 4 Figure 8
		2.50 ±0.20		4.0			4.0			
		3.30 ±0.30		3.0			3.0			
		5.00 ±0.50		2.0			2.0			
		3.30 ±0.30	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	3.0			3.0			
		5.00 ±0.50		2.0			2.0			
t _{REC}	Recover Time CLR, PR to CK	1.80 ±0.15	C _L = 15 pF, R _L = 1 MΩ, S ₁ = Open	8.0			8.0		ns	Figure 7
		2.50 ±0.20		4.5			4.5			
		3.30 ±0.30		3.0			3.0			
		5.00 ±0.50		3.0			3.0			
		3.30 ±0.30	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	3.0			3.0			
		5.00 ±0.50		3.0			3.0			

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AC ELECTRICAL CHARACTERISTICS (continued)

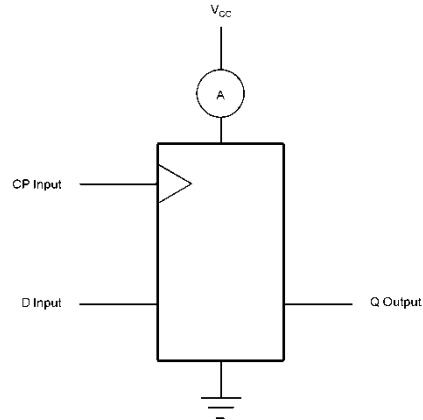
Symbol	Parameter	V _{CC}	Conditions	T _A = +25°C			T _A = -40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
C _{IN}	Input Capacitance	0			3				pF	
C _{OUT}	Output Capacitance	0			4				pF	
C _{PD}	Power Dissipation Capacitance (Note 1)	3.30			10				pF	
		5.00			12					

1. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CCstatic}).



2. C_L includes load and stray capacitance.
Input PRR = 1.0 MHz t_w = 500 ns.

Figure 2. AC Test Circuit



3. CP input = AC Waveforms t_r = t_f = 2.5 ns.
4. CP input PRR = 10 MHz; Duty Cycle = 50%.
5. D input PRR = 5 MHz; Duty Cycle = 50%.

Figure 3. AC Test Circuit

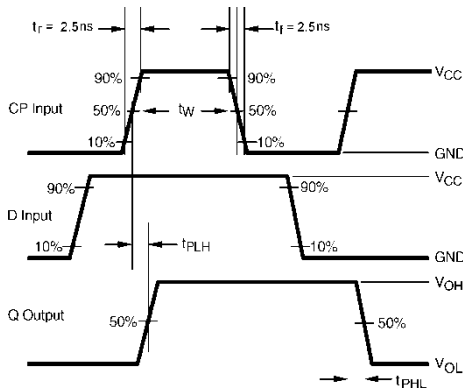


Figure 4. AC Waveforms

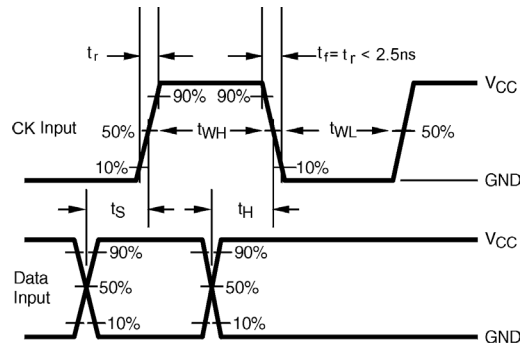


Figure 5. AC Waveforms

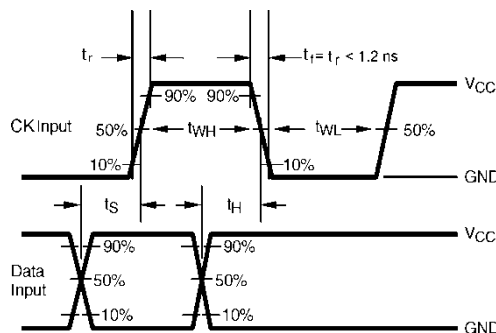


Figure 6. AC Waveforms

NC7SZ74

ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method†
NC7SZ74K8X	SZ74	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3000 Units on Tape & Reel
NC7SZ74L8X	N9	8-Lead MicroPak, 1.6 mm Wide	5000 Units on Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

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UQFN8 1.6X1.6, 0.5P
CASE 523AY
ISSUE O

DATE 31 AUG 2016



**RECOMMENDED
LAND PATTERN**



SIDE VIEW



BOTTOM VIEW

NOTES:

- A. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.



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US8
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